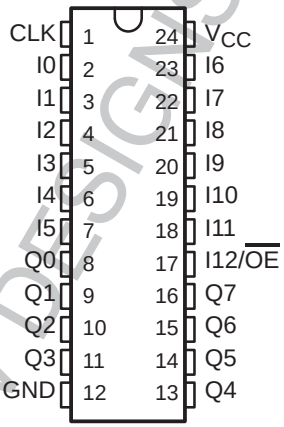
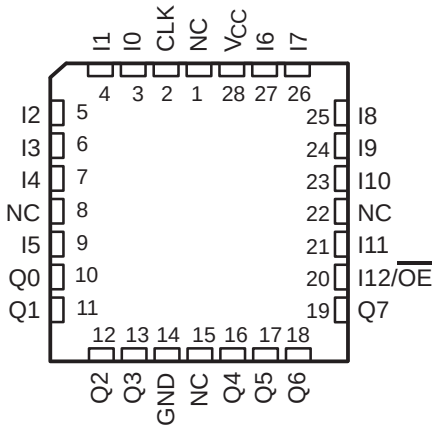
- **58-MHz Max Clock Rate**
- **Two Transition Complement Array Terms**
- **16-Bit Internal State Registers**
- **8-Bit Output Registers**
- **Outputs Programmable for Registered or Combinational Operation**
- **Ideal for Waveform Generation and High-Performance State Machine Applications**
- **Programmable Output Enable**
- **Programmable Clock Polarity**

JT OR NT PACKAGE
(TOP VIEW)



FK OR FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TIBPLS506AC is a TTL field-programmable state machine of the Mealy type. This state machine (logic sequencer) contains 97 product terms (AND terms) and 48 sum terms (OR terms). The product and sum terms are used to control the 16-bit internal state registers and the 8-bit output registers.

The outputs of the internal state registers (P0–P15) are fed back and combined with the 13 inputs (I0–I12) to form the AND array. In addition, two sum terms are complemented and fed back to the AND array, which allows any product term to be summed, complemented, and used as input to the AND array.

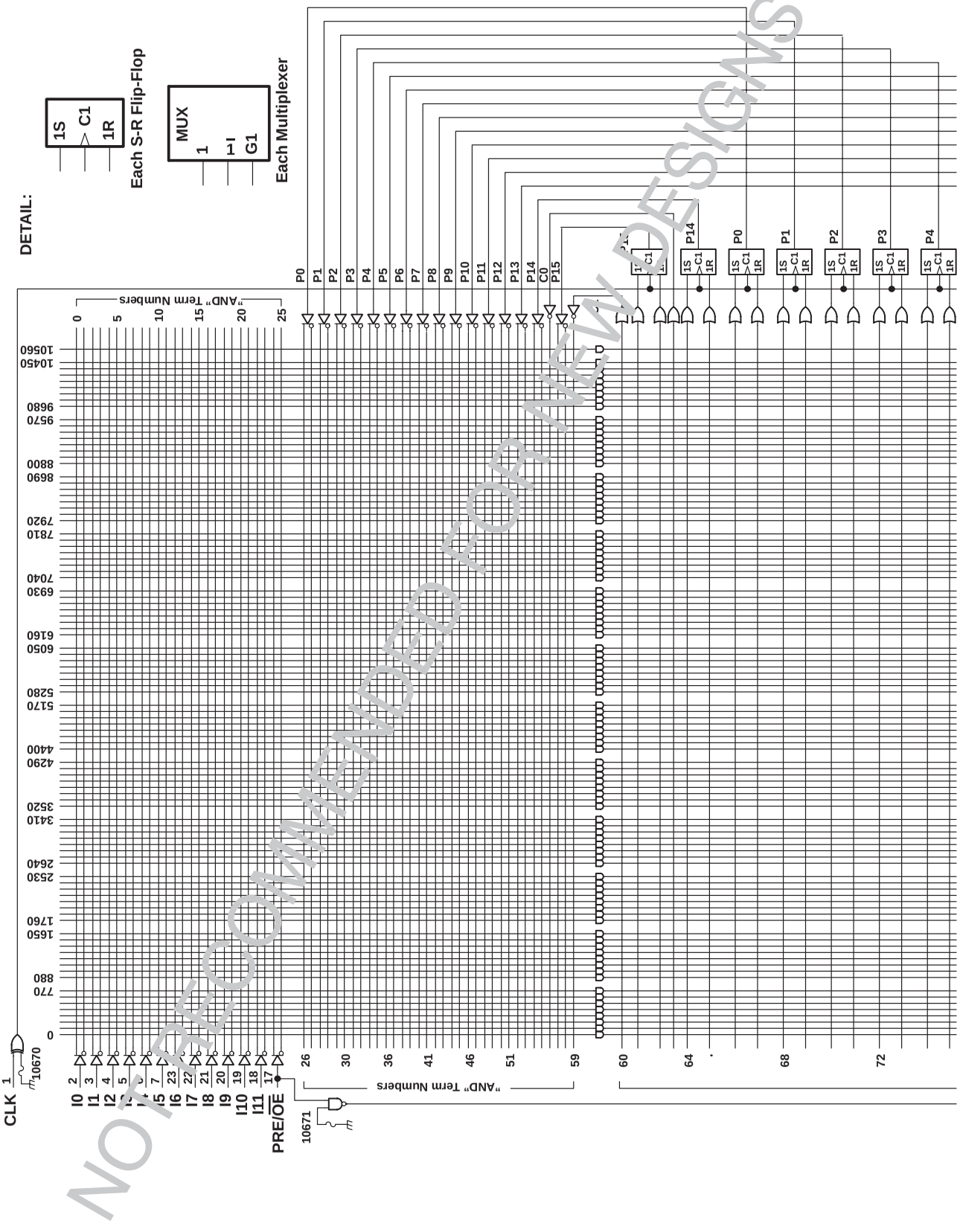
The eight output cells can be individually programmed for registered or combinational operation. Nonregistered operation is selected by blowing the output multiplexer fuse. Registered output operation is selected by leaving the output multiplexer fuse intact.

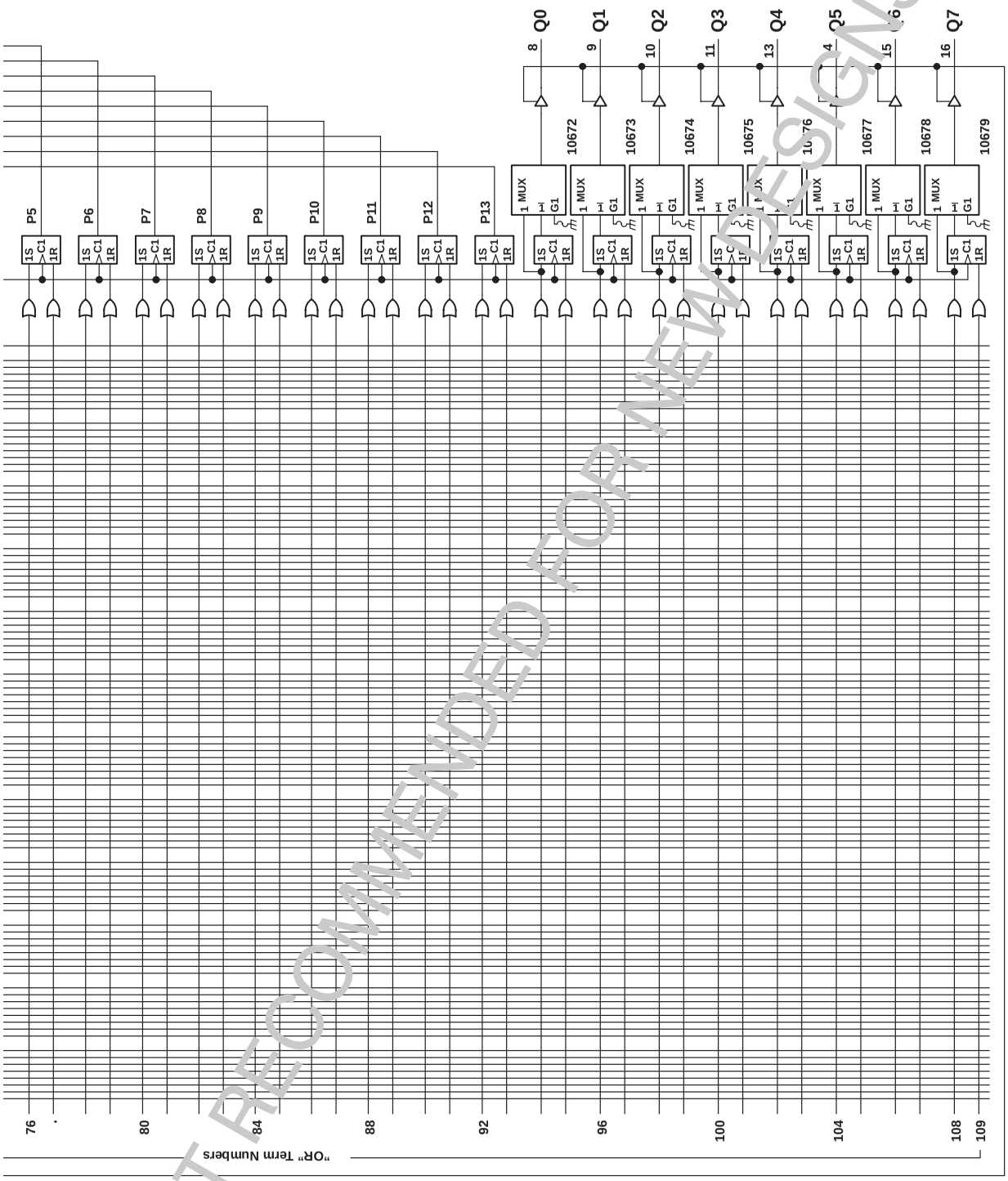
Pin 17 can be programmed to function as an input and/or an output enable. Blowing the output enable fuse lets pin 17 function as an output enable but does not disconnect pin 17 from the input array. When the output enable fuse is intact, pin 17 functions only as an input with the outputs being permanently enabled.

The state and output registers are synchronously clocked by the fuse programmable clock input. The clock polarity fuse selects either postive- or negative-edge triggering. Negative-edge triggering is selected by blowing the clock polarity fuse. Leaving this fuse intact selects positive-edge triggering. After power-up, the device must be initialized to the desired state. When the output multiplexer fuse is left intact, registered operation is selected.

The TIBPLS506AC is characterized for operation from 0°C to 75°C.

logic diagram (positive logic)





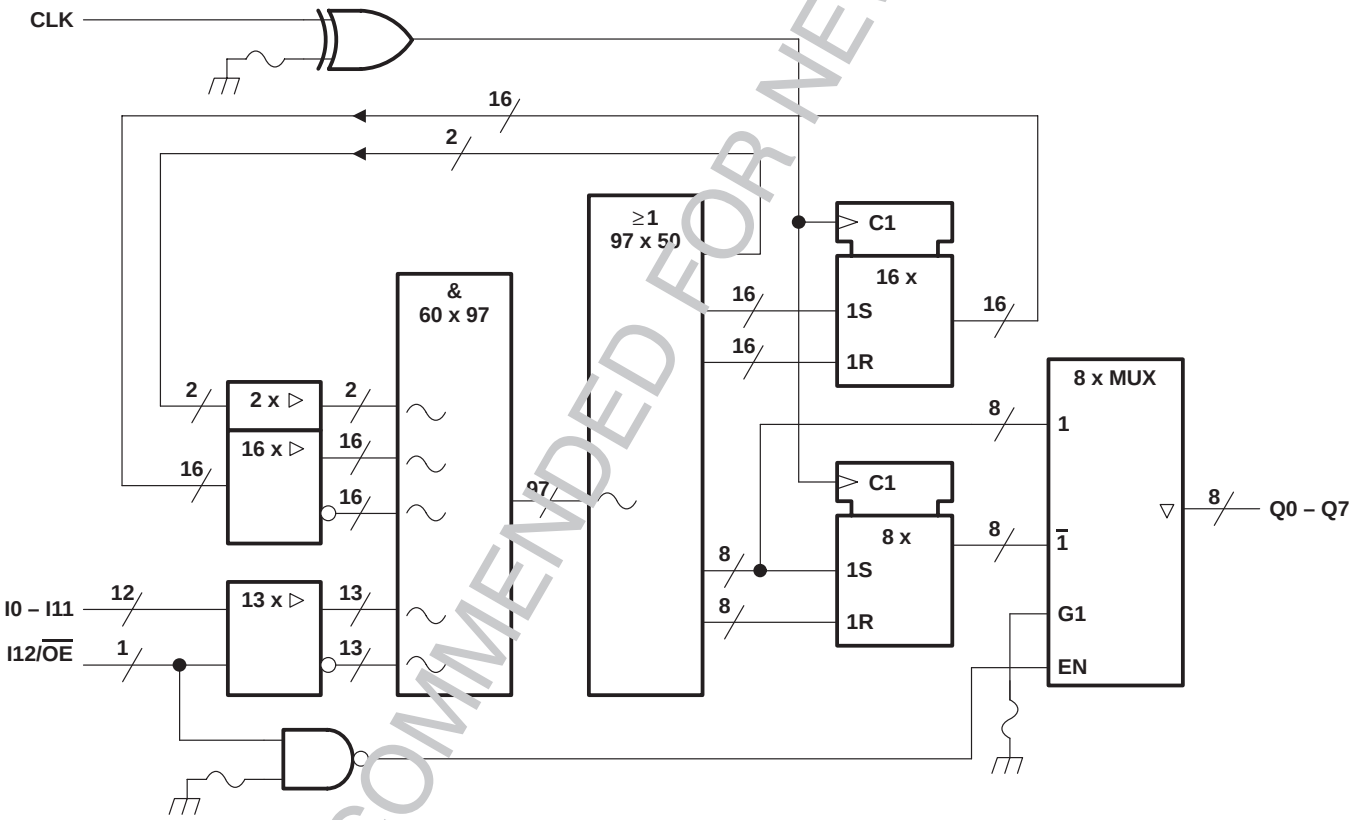
All inputs to AND gates, exclusive-OR gates, and multiplexers with a blown link assume the logic-1 state.
All OR gate inputs with a blown link assume the logic-0 state.

S-R FUNCTION TABLE (see Note 1)

CLK POLARITY FUSE	CLK	S	R	STATE REGISTER
INTACT	↑	L	L	Q_0
INTACT	↑	L	H	L
INTACT	↑	H	L	H
INTACT	↑	H	H	INDETERMINATE
BLOWN	↓	L	L	Q_0
BLOWN	↓	L	H	L
BLOWN	↓	H	L	H
BLOWN	↓	H	H	INDETERMINATE

NOTE 1: Q_0 is the state of the S-R registers before the active clock edge.

functional block diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 2) . . . . . 7 V
Input voltage (see Note 2) . . . . . 5.5 V
Voltage applied to disabled output (see Note 2) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . –65°C to 150°C

NOTE 2: These ratings apply except when programming pins during a programming cycle or during diagnostic testing.

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage			4.75	5	5.25	V
V_{IH}	High-level input voltage, V_{CC} = 5.25 V			2		5.5	V
V_{IL}	Low-level input voltage, V_{CC} = 4.75 V					0.8	V
I_{OH}	High-level output current					–3.2	mA
I_{OL}	Low-level output current					16	mA
t_w	Pulse duration	Clock high		6			ns
		Clock low		6			
t_{su}	Setup time before CLK active transition†	Input or feedback to S/R↑ inputs	Without C-array	12			ns
		Input or feedback to S/R↓ inputs‡		20			
		Input or feedback to S/R inputs	With C-array	25			
t_h	Hold time after CLK	Input or feedback to S/R inputs		0			ns
T_A	Operating free-air temperature			0	25	75	°C

† The active edge of CLK is determined by the programmed state of CLK polarity fuse.
‡ See the OR term loading section and Figure 3.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP§	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = –18 mA				–1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = –3.2 mA		2.4	3		V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 16 mA			0.37	0.5	V
I_{OZH}	V_{CC} = 5.25 V,	V_O = 2.7 V				20	µA
I_{OZL}	V_{CC} = 5.25 V,	V_O = 0.4 V				–20	µA
I_I	V_{CC} = 5.25 V,	V_I = 5.5 V				0.1	mA
I_{IH}	V_{CC} = 5.25 V,	V_I = 2.7 V				20	µA
I_{IL}	V_{CC} = 5.25 V,	V_I = 0.4 V				–0.25	mA
I_O¶	V_{CC} = 5.25 V,	V_O = 0.5 V		–30		–130	mA
I_{CC}	V_{CC} = 5.25 V,	See Note 3,	Outputs open		156	210	mA
C_i	f = 1 MHz,	V_I = 2 V			7		pF
C_o	f = 1 MHz,	V_O = 2 V			11		pF
C_{clk}	f = 1 MHz,	V_{CLK} = 2 V			14		pF

§ All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶ This parameter approximates I_{OS}. The condition V_O = 0.5 V takes tester noise into account. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
NOTE 3: When the clock is programmed for negitive edge, then V_I = 4.75 V. When the clock is programmed for positive edge, then V_I = 0.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}‡	Without C-array		R1 = 300 Ω, R2 = 390 Ω, See Figure 5	58	65		MHz
	With C-array			33	45		
	External feedback without C-array			45	60		
	External feedback with C-array			28.5	40		
t_{pd}	CLK	Q (nonregistered)		6		25	ns
		Q (registered)		3		10	
	I or Feedback	Q (nonregistered)		6		20	ns
t_{en}	$\overline{OE}$↓	Q		1	6	10	ns
t_{dis}	$\overline{OE}$↑	Q		1	6	10	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ See the f_{max} calculations section.

f_{max} calculations

The following is a brief description of how the different operating frequencies can be achieved when using the TIBPLS506A.

f_{max} without C-(complementary) array = $\frac{1}{t_{su} + t_{pd} \text{ CLK to Q}}$ where setup time t_{su} before CLK at the S/R register inputs = 12 ns and propagation delay time t_{pd} CLK to Q for the internal S/R registers = 5ns (difference in t_{pd} from CLK and feedback, 25 to 20).

Thus: f_{max} for this condition = $\frac{1}{(12 + 5) \text{ ns}} = \frac{1}{17 \text{ ns}}$ = 58 MHz.

f_{max} with the C-array = $\frac{1}{t_{su} + t_{pd} \text{ CLK to Q}}$ where t_{su} setup time before CLK at the S/R register inputs = 25 ns and propagation delay time t_{pd} CLK to Q for the internal S/R registers = 5 ns (difference in t_{pd} from CLK and feedback, 25 to 20)

Thus: f_{max} for this condition = $\frac{1}{(25 + 5) \text{ ns}} = \frac{1}{30 \text{ ns}}$ = 33 MHz.

f_{max} external feedback without the C-array = $\frac{1}{t_{su} + t_{pd} \text{ CLK to Q}}$ where setup time t_{su} before CLK at the S/R register inputs = 12 ns and propagation delay time t_{pd} CLK to Q for the internal S/R registers = 10 ns

Thus: f_{max} for this condition = $\frac{1}{(12 + 10) \text{ ns}} = \frac{1}{22 \text{ ns}}$ = 45 MHz.

f_{max} external feedback with the C-array = $\frac{1}{t_{su} + t_{pd} \text{ CLK to Q}}$ where setup time t_{su} before CLK at the S/R register inputs = 25 ns and propagation delay time t_{pd} CLK to Q for the internal S/R registers = 10 ns.

Thus: f_{max} for this condition = $\frac{1}{(25 + 10) \text{ ns}} = \frac{1}{35 \text{ ns}}$ = 28.5 MHz.

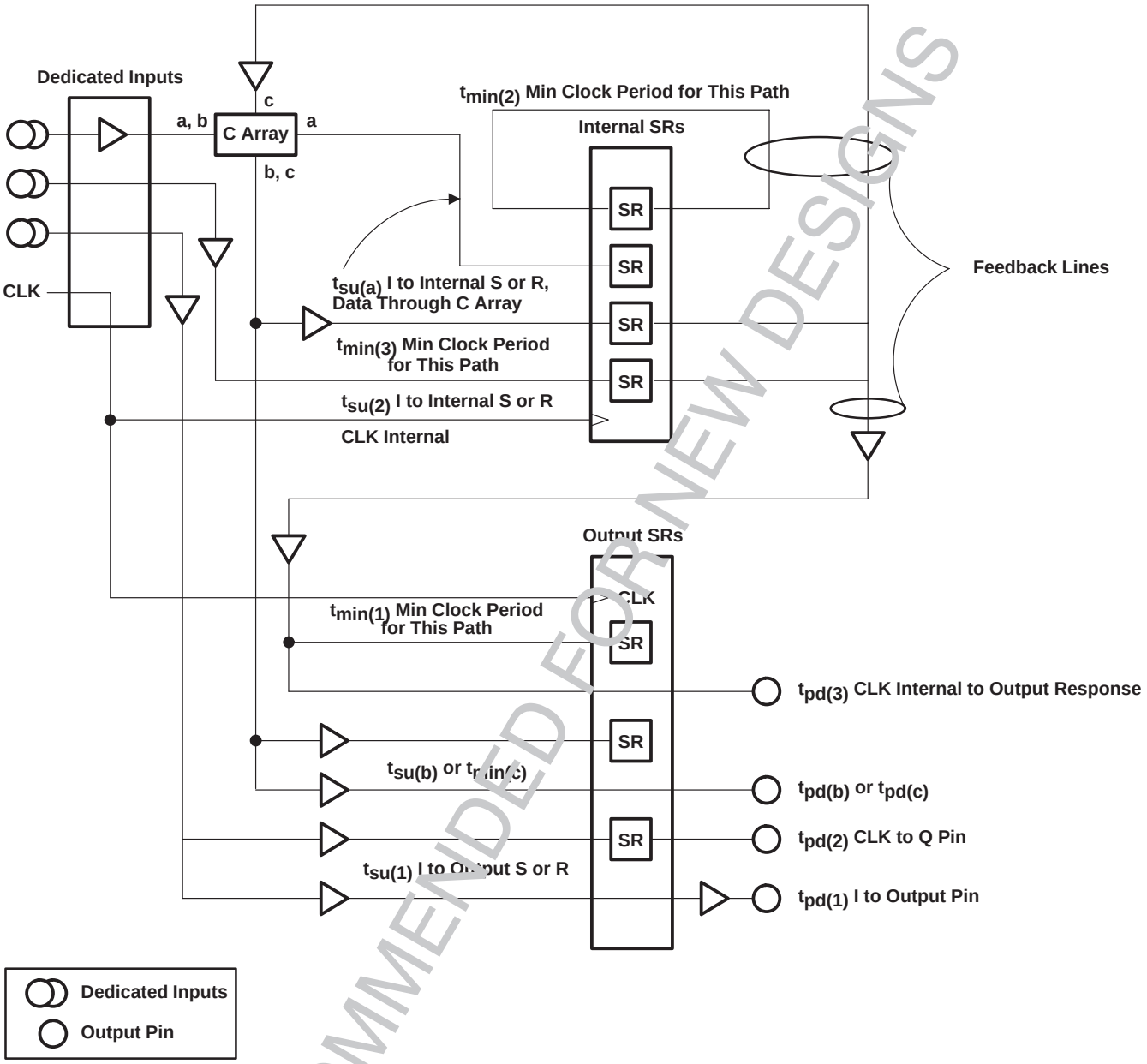


Figure 1. Timing Model

glossary — timing model

$t_{pd(1)}$ — Maximum time interval from the time a signal edge is received at any input pin to the time any logically affected combinational output pin delivers a response.

$t_{pd(2)}$ — Maximum time interval from a positive edge on the clock input pin to data delivery on the output pin corresponding to any output SR register.

$t_{pd(3)}$ — Maximum time interval from the positive edge on the clock input pin to the response on any logically affected combinational configured output (at the pin), where data origin is any internal SR register.

$t_{pd(b)}$ — Maximum time interval from the time a signal edge is received at any input pin to the time any logically affected combinational output pin delivers a response, where data passes through a C-array once before reaching the affected output.

$t_{pd(c)}$ — Maximum time interval from the positive edge on the clock input pin to the response on any logically affected combinational configured output (at the pin), where data origin is any internal SR register and data passes once through a C-array before reaching an affected output.

$t_{su(1)}$ — Minimum time interval that must be allowed between the data edge on any dedicated input and the active clock edge on the clock input pin when data affects the S or R line of any output SR register.

$t_{su(2)}$ — Minimum time interval that must be allowed between the data edge on any dedicated input and the active clock edge on the clock input pin when data affects the S or R line of any internal SR register.

$t_{su(a)}$ — Minimum time interval that must be allowed between the data edge on any dedicated input and the active clock edge on the clock input pin when data passes once through a C-array before reaching an affected S or R line on any internal SR register.

$t_{su(b)}$ — Minimum time interval that must be allowed between the data edge on any dedicated input and the active clock edge on the clock input pin when data passes once through a C-array before reaching an affected S or R line on any output SR register.

$t_{min(1)}$ — Minimum clock period (or 1/[maximum frequency]) that the device will accommodate when using feedback from any internal SR register or counter bit to feed the S or R line of any output SR register.

$t_{min(2)}$ — Minimum clock period (or 1/[maximum frequency]) that the device will accommodate when using feedback from any internal SR register to feed the S or R line of any internal SR register.

$t_{min(3)}$ — Minimum clock period (or 1/[maximum frequency]) that the device will accommodate when using feedback from any internal SR register to feed the S or R line of any internal SR register and data passes once through a C-array before reaching an affected S or R line on any internal SR register.

$t_{min(c)}$ — Minimum clock period (or 1/[maximum frequency]) that the device will accommodate when using feedback from any internal SR register to feed the S or R line of any output SR register and data passes once through a C-array before reaching an affected S or R line on any output SR register.

PARAMETER VALUES FOR TIMING MODEL

$t_{pd(1)}$ = 20 ns	$t_{su(1)}$ = 12 ns†	$t_{min(1)}$ = 20 ns
$t_{pd(2)}$ = 10 ns	$t_{su(2)}$ = 12 ns†	$t_{min(2)}$ = 20 ns
$t_{pd(3)}$ = 25 ns	$t_{su(a)}$ = 25 ns	$t_{min(3)}$ = 25 ns
	$t_{su(b)}$ = 25 ns	$t_{min(c)}$ = 25 ns

INTERNAL NODE NUMBERS

Q0-Q7	RESET 25-32	P0-P15	SET 33-48
C0	65		RESET 49-64
C1	66		

† Use tsu = 20 ns for applications where the setup time for S/R↓ inputs are required.

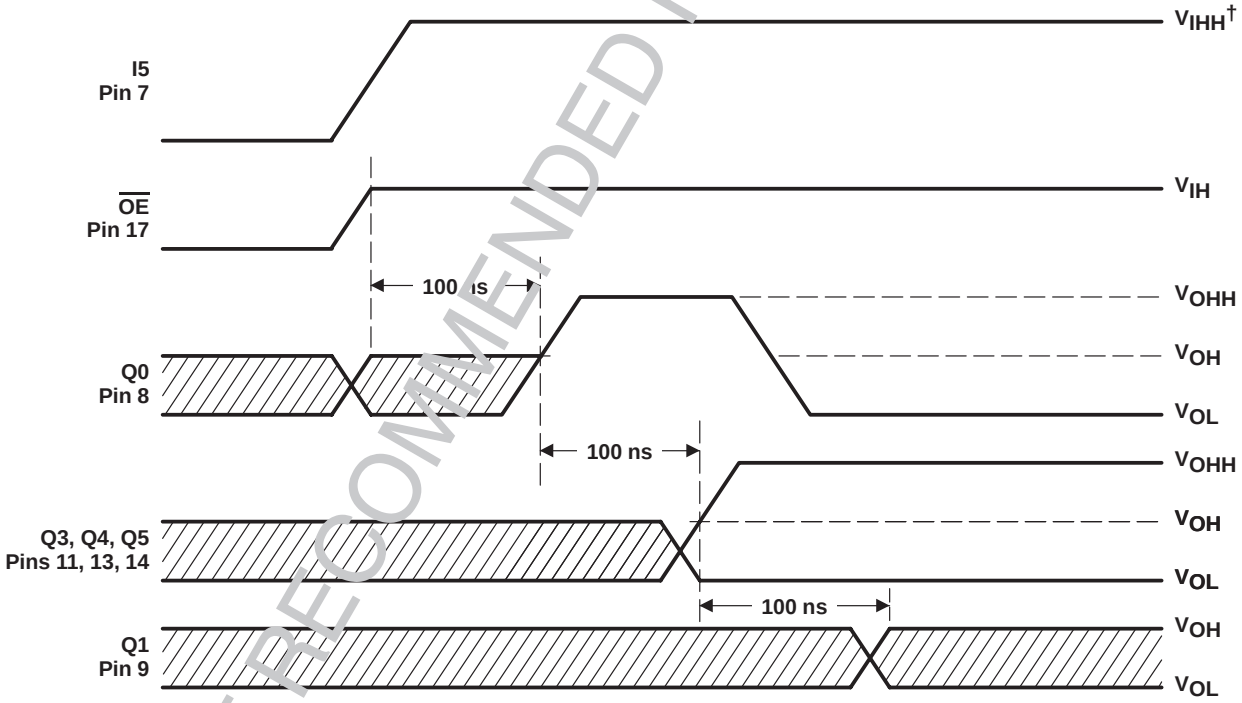
diagnostics

A diagnostic mode is provided with these devices that allows the user to inspect the contents of the state registers. The step-by-step procedures required to use the diagnostics follow.

Step 1. Disable all outputs by taking pin 17 ($\overline{OE}$) high (see Note 4).
Step 2. Take pin 8 (Q0) to V_{IHH} to enable the diagnostics test sequence.
Step 3. Apply appropriate levels of voltage to pins 11 (Q3), 13 (Q4), and 14 (Q5) to select the desired state register (see Table 1).

The voltage level monitored on pin 9 will indicate the state of the selected state register.

NOTE 4: If pin 17 is being used as an input to the array, then pin 7 (I5) must be taken to V_{IHH} before pin 17 is taken high.



† V_{IHH} = 10.25 V min, 10.5 V nom, 10.75 V max

Figure 2. Diagnostics Waveforms

Table 1. Addressing State Registers During Diagnostics†

REGISTER BINARY ADDRESS			BURIED REGISTER
PIN 11	PIN13	PIN 14	SELECTED
L	L	L	C1
L	L	H	P15
L	L	HH	C0
L	H	L	P14
L	H	H	P0
L	H	HH	P1
L	HH	L	P2
L	HH	H	P3
L	HH	HH	P4
H	L	L	P5
H	L	H	P6
H	L	HH	P7
H	H	L	P8
H	H	H	P9
H	H	HH	P10
H	HH	L	P11
H	HH	H	P12
H	HH	HH	P13

† V_{IHH} = 10.25 V min, 10.5 V nom, 10.75 V max

programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers that are capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

OR term loading

As shown in Figure 3 and by the f_{max} calculations, f_{max} is affected by the number of terms connected to each OR array line. Theoretically, f_{max} is calculated as:

$$f_{max} = \frac{1}{t_{su} + t_{pd}\ \text{CLK to Q}}$$

Since the setup time (input or feedback to S/R↓) varies with the number of terms connected to each OR array line, (due to capacitance loading) f_{max}will also vary. Figure 3 illustrates the relationship between the number of terms connected per OR line and the setup time.

Use Figure 3 to determine the worst-case setup time for a particular application. Identify the OR array line with the maximum number of terms connected. Count the number of terms and use the graph to determine the setup time.

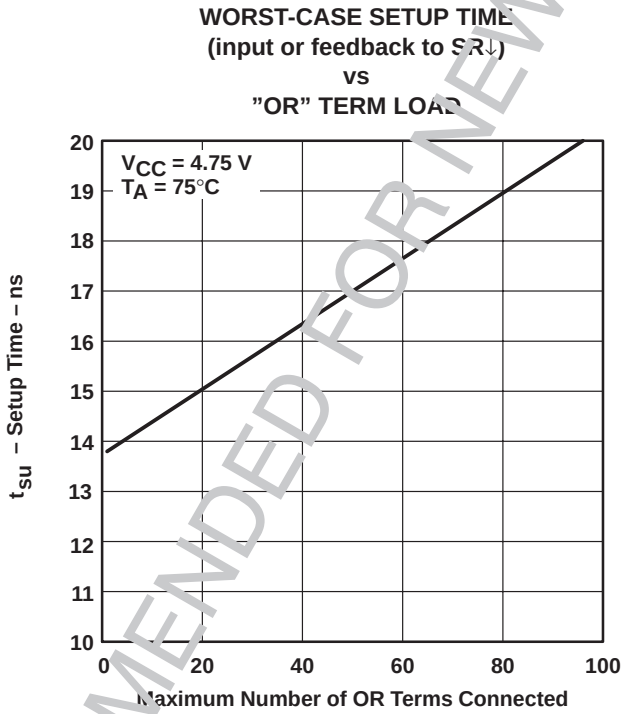


Figure 3

f_{max} with external feedback

The configuration shown is a typical state-machine design with feedback signals sent off-chip. This external feedback could go back to the device inputs or to a second device in a multi-chip state machine. The slowest path defining the clock period is the sum of the clock-to-output delay time and the setup time for the input or feedback signals (t_{su} + t_{pd} CLK to Q).

Thus: f_{max} with external feedback = $\frac{1}{t_{su} + t_{pd} \text{ CLK to Q}}$

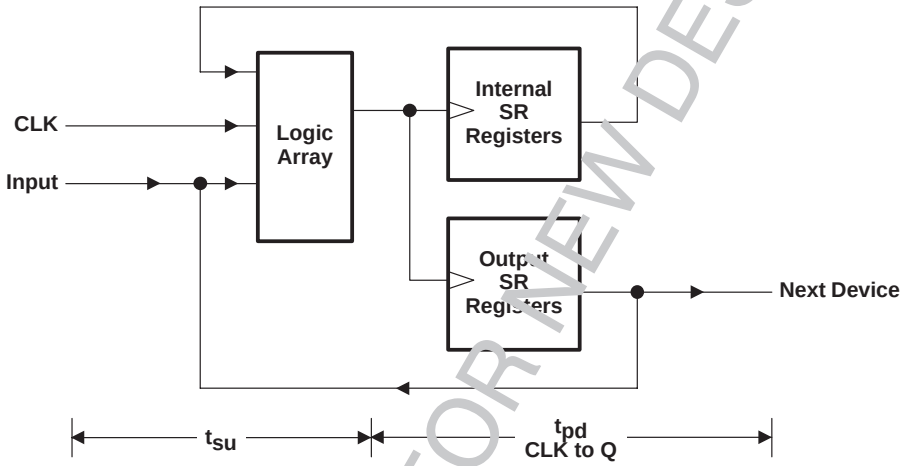
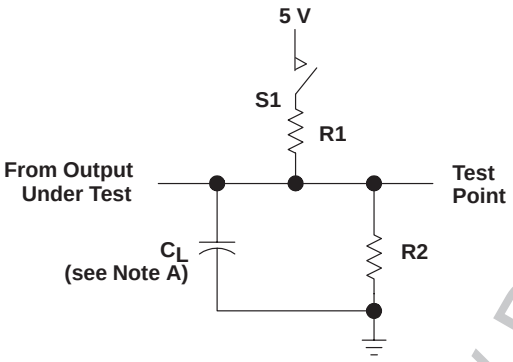
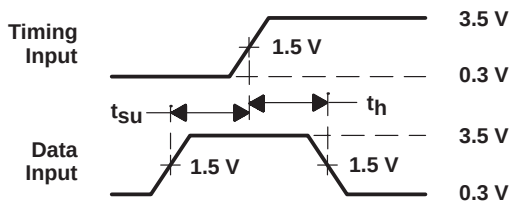


Figure 4

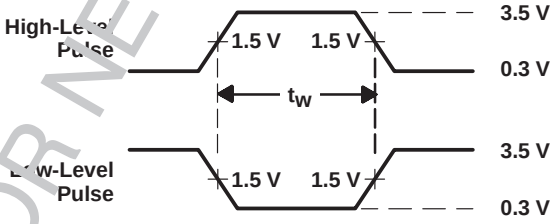
PARAMETER MEASUREMENT INFORMATION



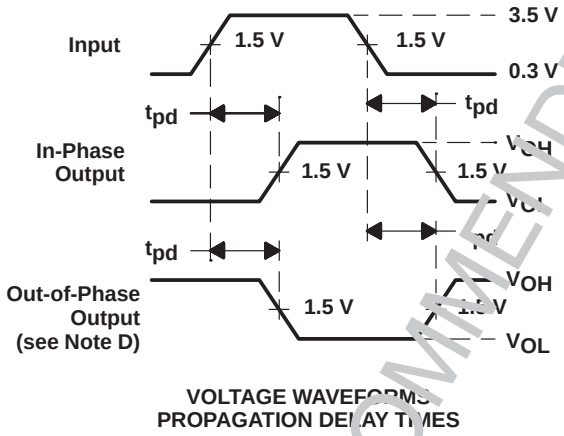
LOAD CIRCUIT FOR 3-STATE OUTPUTS



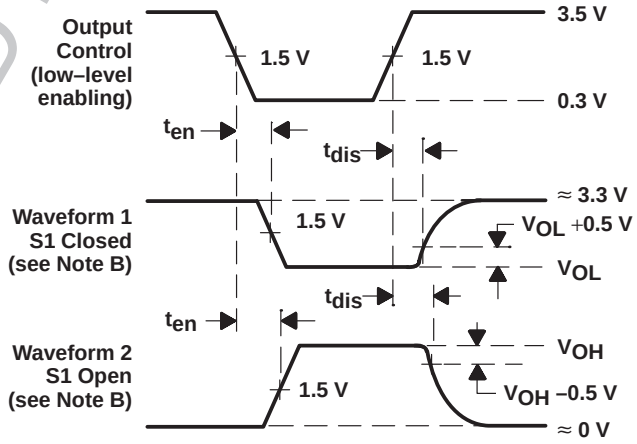
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f \leq 2$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

Figure 5. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

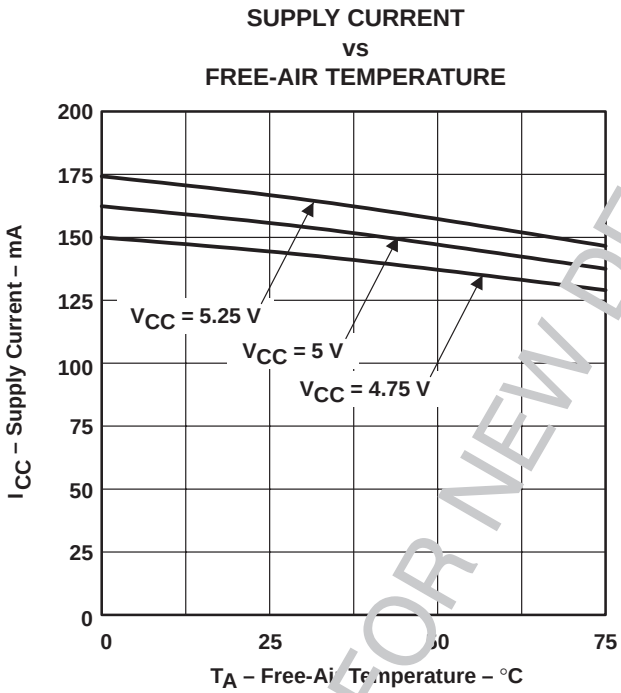


Figure 6

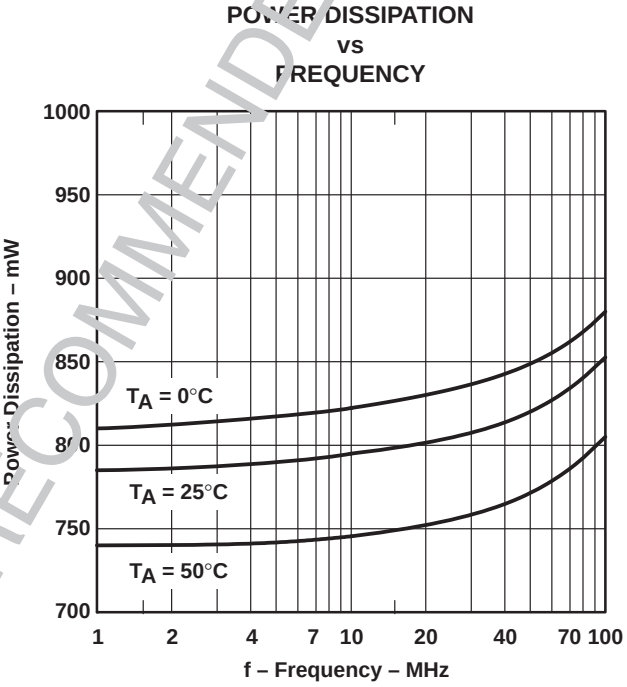


Figure 7

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME vs SUPPLY VOLTAGE

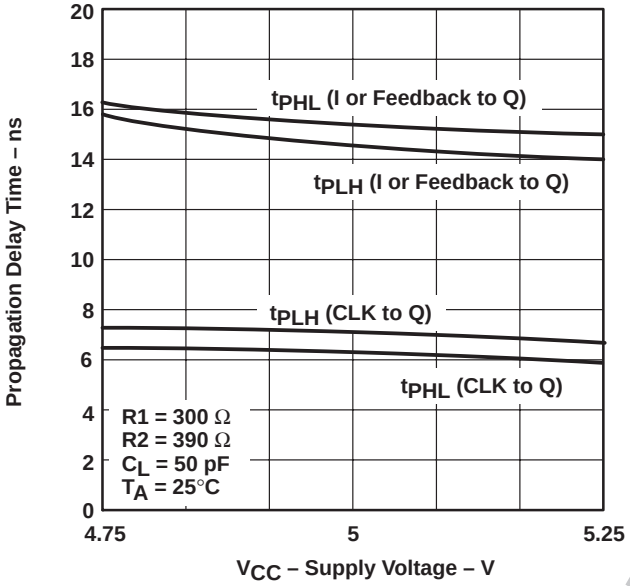


Figure 8

PROPAGATION DELAY TIME vs LOAD CAPACITANCE

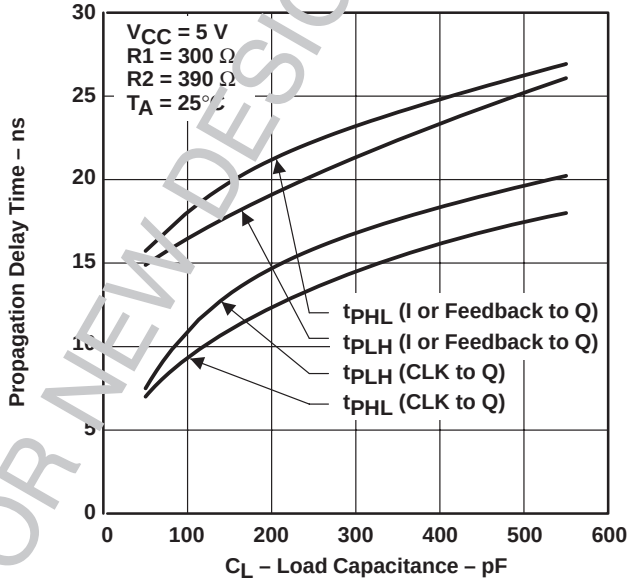


Figure 9

PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

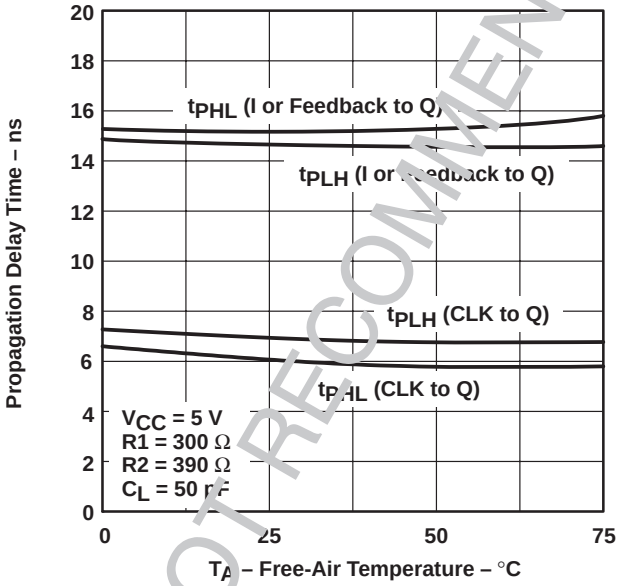


Figure 10

PROPAGATION DELAY TIME vs NUMBER OF OUTPUTS SWITCHING

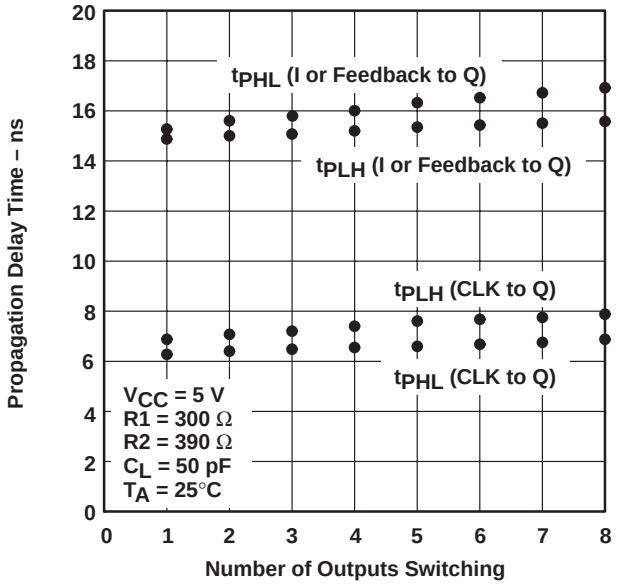


Figure 11

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