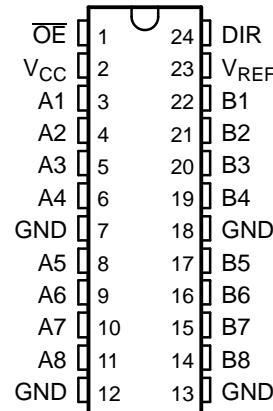


FEATURES

- **TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **LVTTL Interfaces Are 5-V Tolerant**
- **Medium-Drive GTLP Outputs (50 mA)**
- **LVTTL Outputs (-24 mA/24 mA)**
- **GTLP Rise and Fall Times Designed for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Bus Hold on A-Port Data Inputs**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

**DGV, DW, OR PW PACKAGE
(TOP VIEW)**



DESCRIPTION/ORDERING INFORMATION

The SN74GTLPH306 is a medium-drive, 8-bit bus transceiver that provides LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard LVTTL or TTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC™ circuitry, and TI-OPC™ circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The medium drive allows incident-wave switching in heavily loaded backplanes with equivalent load impedance down to $19\ \Omega$.

GTLP is the Texas Instruments (TI™) derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification of the SN74GTLPH306 is given only at the preferred higher-noise-margin GTLP, but the user has the flexibility of using this device at either GTL ($V_{TT} = 1.2$ V and $V_{REF} = 0.8$ V) or GTLP ($V_{TT} = 1.5$ V and $V_{REF} = 1$ V) signal levels.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels, but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs. V_{REF} is the B-port differential input reference voltage.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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DESCRIPTION/ORDERING INFORMATION (CONTINUED)

This GTLP device features TI-OPC circuitry, which actively limits overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

Active bus-hold circuitry holds unused or undriven LVTTL data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable (\overline{OE}) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube	SN74GTLPH306DW	GTLPH306
		Tape and reel	SN74GTLPH306DWR	
	TSSOP – PW	Tape and reel	SN74GTLPH306PWR	GH306
	TVSOP – DGV	Tape and reel	SN74GTLPH306DGVR	GH306

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTIONAL DESCRIPTION

The SN74GTLPH306 is an 8-bit bus transceiver and is designed for asynchronous communication between data buses. The device transmits data from the A port to the B port or from the B port to the A port, depending on the logic level at the direction-control (DIR) input. \overline{OE} can be used to disable the device so the buses are effectively isolated. Data polarity is noninverting.

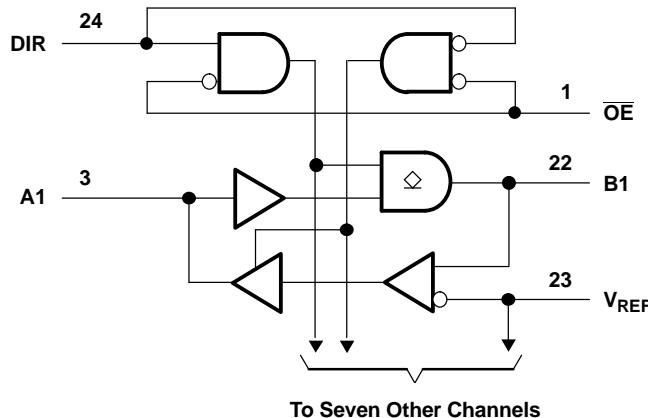
For A-to-B data flow, when \overline{OE} is low and DIR is high, the B outputs take on the logic value of the A inputs. When \overline{OE} is high, the outputs are in the high-impedance state.

The data flow for B to A is similar to A to B, except \overline{OE} and DIR are low.

FUNCTION TABLE

INPUTS		OUTPUT	MODE
\overline{OE}	DIR		
H	X	Z	Isolation
L	L	B data to A port	True transparent
L	H	A data to B port	

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	4.6	V
V_I	Input voltage range ⁽²⁾	A port and control inputs	-0.5	7
		B port and V_{REF}	-0.5	4.6
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	A port	-0.5	7
		B port	-0.5	4.6
I_O	Current into any output in the low state	A port	48	mA
		B port	100	mA
I_O	Current into any A port output in the high state ⁽³⁾		48	mA
	Continuous current through each V_{CC} or GND		± 100	mA
I_{IK}	Input clamp current	$V_I < 0$	-50	mA
I_{OK}	Output clamp current	$V_O < 0$	-50	mA
θ_{JA}	Package thermal impedance ⁽⁴⁾	DGV package	86	°C/W
		DW package	46	
		PW package	88	
T_{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) This current flows only when the output is in the high state and $V_O > V_{CC}$.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

SN74GTLPH306
8-BIT LVTTL-TO-GTLP BUS TRANSCEIVER

SCES284E—OCTOBER 1999—REVISED APRIL 2005



Recommended Operating Conditions⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V_I	Input voltage	B port			V_{TT}	V
		Except B port		V_{CC}	5.5	
V_{IH}	High-level input voltage	B port		$V_{REF} + 0.05$		V
		Except B port		2		
V_{IL}	Low-level input voltage	B port			$V_{REF} - 0.05$	V
		Except B port			0.8	
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A port			-24	mA
I_{OL}	Low-level output current	A port			24	mA
		B port			50	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate			20		$\mu s/V$
T_A	Operating free-air temperature			-40	85	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
- (2) Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS $V_{CC} = 3.3$ V first, I/O second, and $V_{CC} = 3.3$ V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable, but generally, GND is connected first.
- (3) V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc recommended I_{OL} ratings are not exceeded.
- (4) V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT} . TI-OPC circuitry is enabled in the A-to-B direction and is activated when $V_{TT} > 0.7$ V above V_{REF} . If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current drain.

Electrical Characteristics

over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IK}		$V_{CC} = 3.15 \text{ V}$,	$I_I = -18 \text{ mA}$			-1.2	V
V_{OH}	A port	$V_{CC} = 3.15 \text{ V to } 3.45 \text{ V}$,	$I_{OH} = -100 \mu\text{A}$	$V_{CC} - 0.2$			V
		$V_{CC} = 3.15 \text{ V}$	$I_{OH} = -12 \text{ mA}$	2.4			
V_{OL}	A port	$V_{CC} = 3.15 \text{ V to } 3.45 \text{ V}$,	$I_{OL} = 100 \mu\text{A}$		0.2		V
		$V_{CC} = 3.15 \text{ V}$	$I_{OL} = 12 \text{ mA}$		0.4		
	B port		$I_{OL} = 24 \text{ mA}$		0.5		
		$V_{CC} = 3.15 \text{ V}$	$I_{OL} = 40 \text{ mA}$		0.4		
$I_I^{(2)}$	A-port and control inputs	$V_{CC} = 3.45 \text{ V}$	$I_{OL} = 50 \text{ mA}$		0.55		μA
			$V_I = 0 \text{ or } V_{CC}$		± 5		
	B port		$V_I = 5.5 \text{ V}$		± 20		
$I_{BHL}^{(3)}$	A port	$V_{CC} = 3.15 \text{ V}$,	$V_I = 0.8 \text{ V}$	75			μA
$I_{BHH}^{(4)}$	A port	$V_{CC} = 3.15 \text{ V}$,	$V_I = 2 \text{ V}$	-75			μA
$I_{BHLO}^{(5)}$	A port	$V_{CC} = 3.45 \text{ V}$,	$V_I = 0 \text{ to } V_{CC}$	500			μA
$I_{BHHO}^{(6)}$	A port	$V_{CC} = 3.45 \text{ V}$,	$V_I = 0 \text{ to } V_{CC}$	-500			μA
I_{CC}	A or B port	$V_{CC} = 3.45 \text{ V}$, $I_O = 0$, V_I (A-port or control input) = V_{CC} or GND, V_I (B port) = V_{TT} or GND	Outputs high		20		mA
			Outputs low		20		
			Outputs disabled		20		
$\Delta I_{CC}^{(7)}$		$V_{CC} = 3.45 \text{ V}$, One A-port or control input at $V_{CC} - 0.6 \text{ V}$, Other A-port or control inputs at V_{CC} or GND			1.5		mA
C_i	Control inputs	$V_I = 3.15 \text{ V or } 0$		4.5	5		pF
C_{io}	A port	$V_O = 3.15 \text{ V or } 0$		7.5	9		pF
	B port	$V_O = 1.5 \text{ V or } 0$		7.5	9		

- (1) All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.
- (2) For I/O ports, the parameter I_I includes the off-state output leakage current.
- (3) The bus-hold circuit can sink at least the minimum low sustaining current at $V_{IL\text{max}}$. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to $V_{IL\text{max}}$.
- (4) The bus-hold circuit can source at least the minimum high sustaining current at $V_{IH\text{min}}$. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to $V_{IH\text{min}}$.
- (5) An external driver must source at least I_{BHLO} to switch this node from low to high.
- (6) An external driver must sink at least I_{BHHO} to switch this node from high to low.
- (7) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

Hot-Insertion Specifications for A Port

over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	$V_{CC} = 0$,	V_I or $V_O = 0 \text{ to } 5.5 \text{ V}$			10	μA
I_{OZPU}	$V_{CC} = 0 \text{ to } 1.5 \text{ V}$,	$V_O = 0.5 \text{ V to } 3 \text{ V}$,	$\overline{OE} = 0$		± 30	μA
I_{OZPD}	$V_{CC} = 1.5 \text{ V to } 0$,	$V_O = 0.5 \text{ V to } 3 \text{ V}$,	$\overline{OE} = 0$		± 30	μA

Hot-Insertion Specifications for B Port

over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	$V_{CC} = 0$,	V_I or $V_O = 0 \text{ to } 1.5 \text{ V}$			10	μA
I_{OZPU}	$V_{CC} = 0 \text{ to } 1.5 \text{ V}$,	$V_O = 0.5 \text{ V to } 1.5 \text{ V}$,	$\overline{OE} = 0$		± 30	μA
I_{OZPD}	$V_{CC} = 1.5 \text{ V to } 0$,	$V_O = 0.5 \text{ V to } 1.5 \text{ V}$,	$\overline{OE} = 0$		± 30	μA

SN74GTLPH306
8-BIT LVTTL-TO-GTLP BUS TRANSCEIVER

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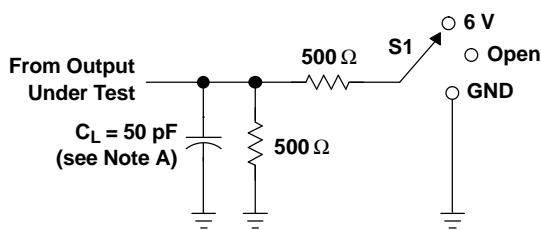
Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature,
 $V_{TT} = 1.5$ V and $V_{REF} = 1$ V for GTLP (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP ⁽¹⁾	MAX	UNIT	
t_{PLH}	A	B	1	7.5	ns		
t_{PHL}			1	7.5			
t_{en}	\overline{OE}	B	1	8	ns		
t_{dis}			1	8			
t_r	Rise time, B outputs (20% to 80%)			2.2	ns		
t_f	Fall time, B outputs (80% to 20%)			2.1	ns		
t_r	Rise time, A outputs (10% to 90%)			4.1	ns		
t_f	Fall time, A outputs (90% to 10%)			3.3	ns		
t_{PLH}	B	A	1	7	ns		
t_{PHL}			1	7			
t_{en}	\overline{OE}	A	1	8	ns		
t_{dis}			1	8			

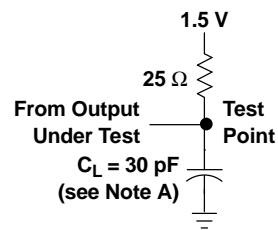
(1) All typical values are at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION

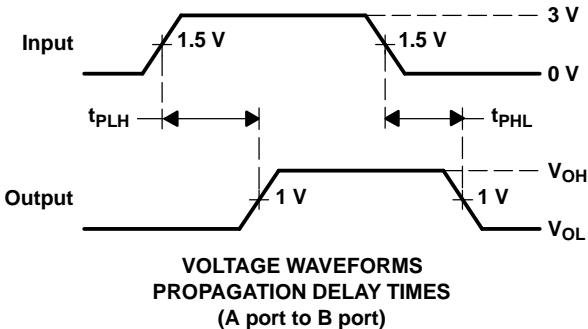


LOAD CIRCUIT FOR A OUTPUTS

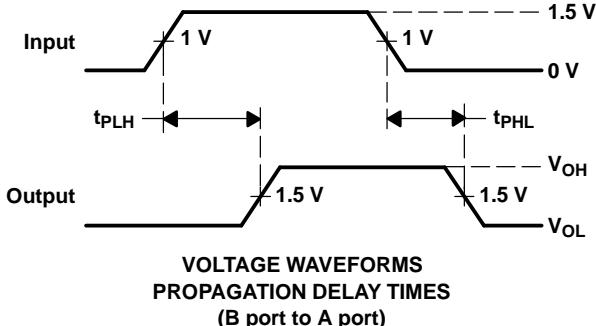
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



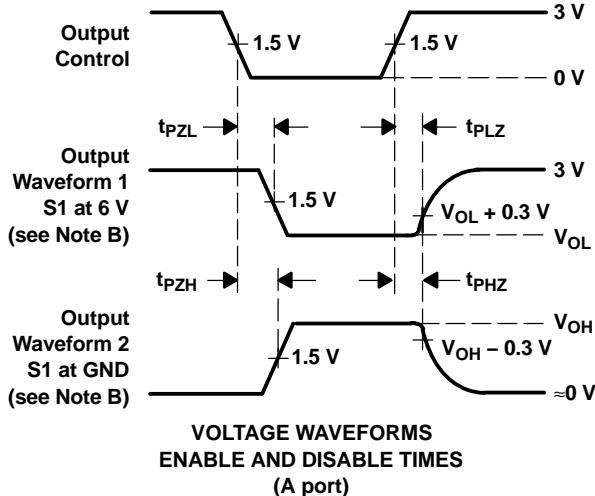
LOAD CIRCUIT FOR B OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)

NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: $PRR \approx 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \approx 2 \text{ ns}$, $t_f \approx 2 \text{ ns}$.
- The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

Distributed-Load Backplane Switching Characteristics

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 2. This backplane, or distributed load, can be approximated closely to a resistor inductance capacitance (RLC) circuit, as shown in Figure 3. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

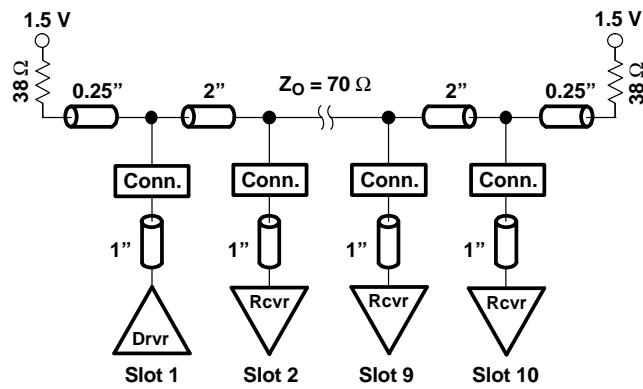


Figure 2. Medium-Drive Test Backplane

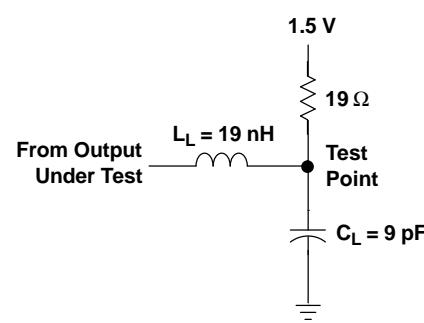


Figure 3. Medium-Drive RLC Network

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature,
 $V_{TT} = 1.5$ V and $V_{REF} = 1$ V for GTLP (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TYP ⁽¹⁾	UNIT	
t_{PLH}	A	B	3.6	ns	
t_{PHL}			4.1		
t_{en}	\overline{OE}	B	4.4	ns	
t_{dis}			4.6		
t_r	Rise time, B outputs (20% to 80%)			1.2 ns	
t_f	Fall time, B outputs (80% to 20%)			2.2 ns	

(1) All typical values are at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$. All values are derived from TI-SPICE models.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
74GTLPH306DGVR4	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
74GTLPH306DGVRG4	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74GTLPH306DGVR	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74GTLPH306DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74GTLPH306DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74GTLPH306DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74GTLPH306DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74GTLPH306DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74GTLPH306PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74GTLPH306PWE4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74GTLPH306PWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74GTLPH306PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74GTLPH306PWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74GTLPH306PWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

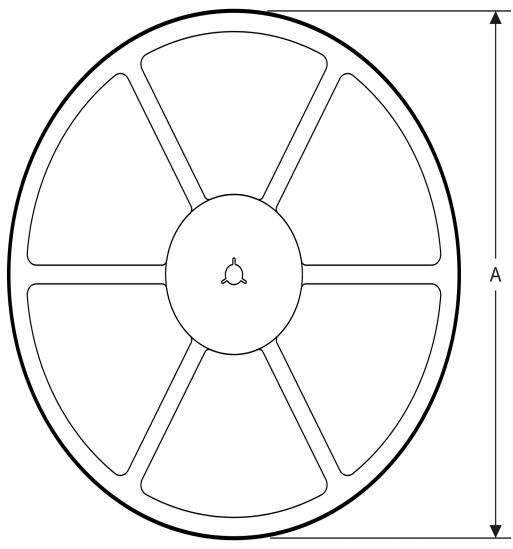
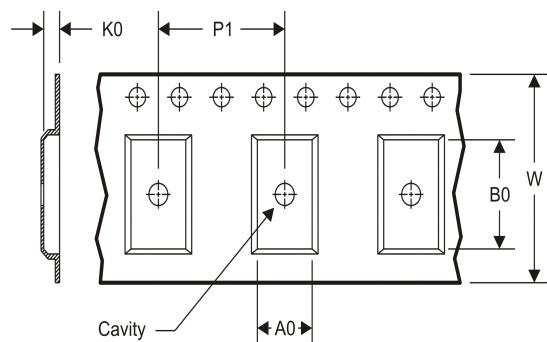
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

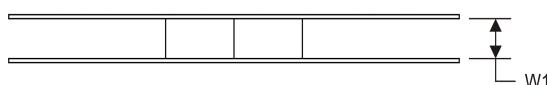
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers


TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74GTLPH306DGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74GTLPH306DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74GTLPH306PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74GTLPH306DGVR	TVSOP	DGV	24	2000	367.0	367.0	35.0
SN74GTLPH306DWR	SOIC	DW	24	2000	367.0	367.0	45.0
SN74GTLPH306PWR	TSSOP	PW	24	2000	367.0	367.0	38.0

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

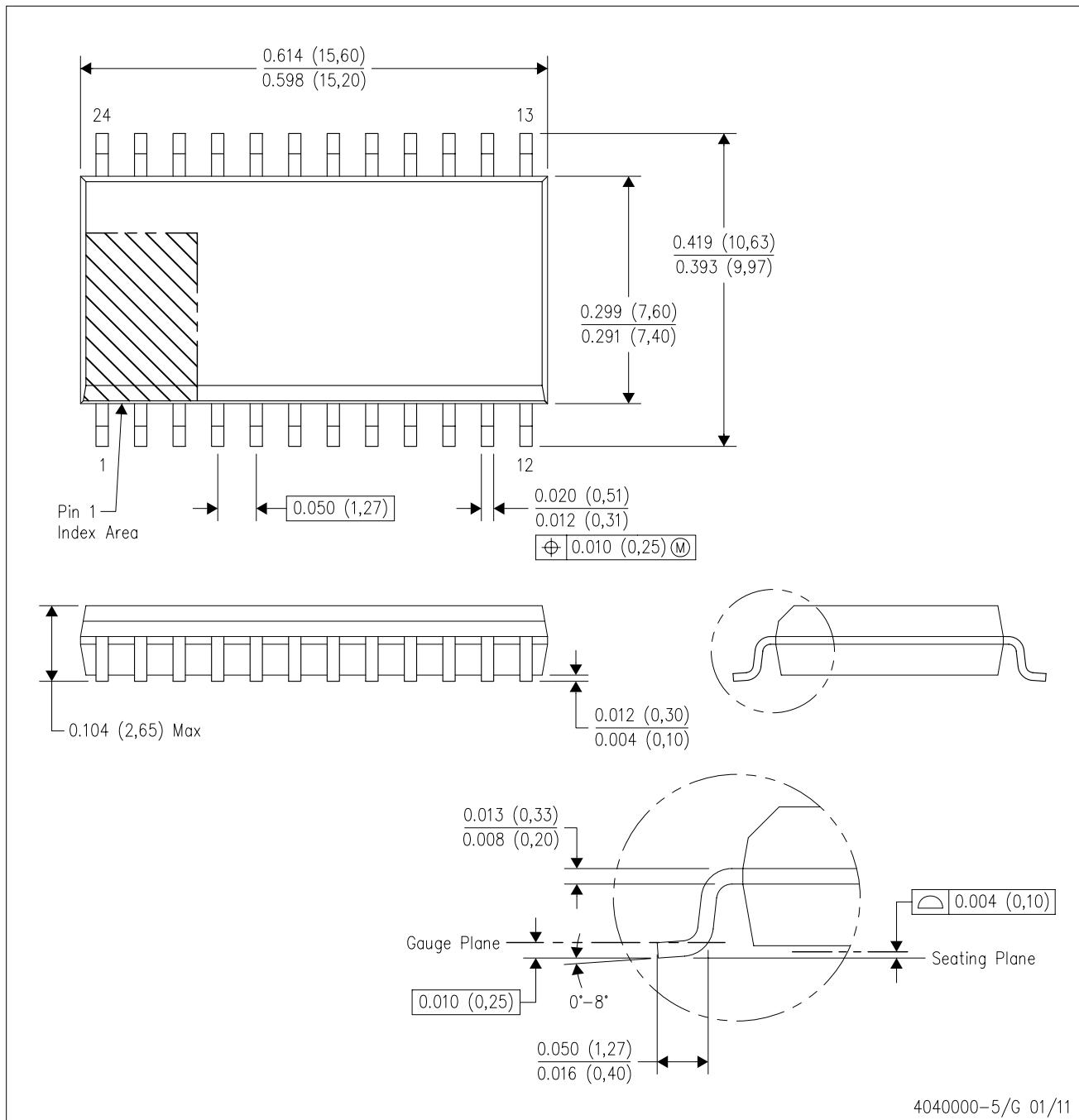
24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

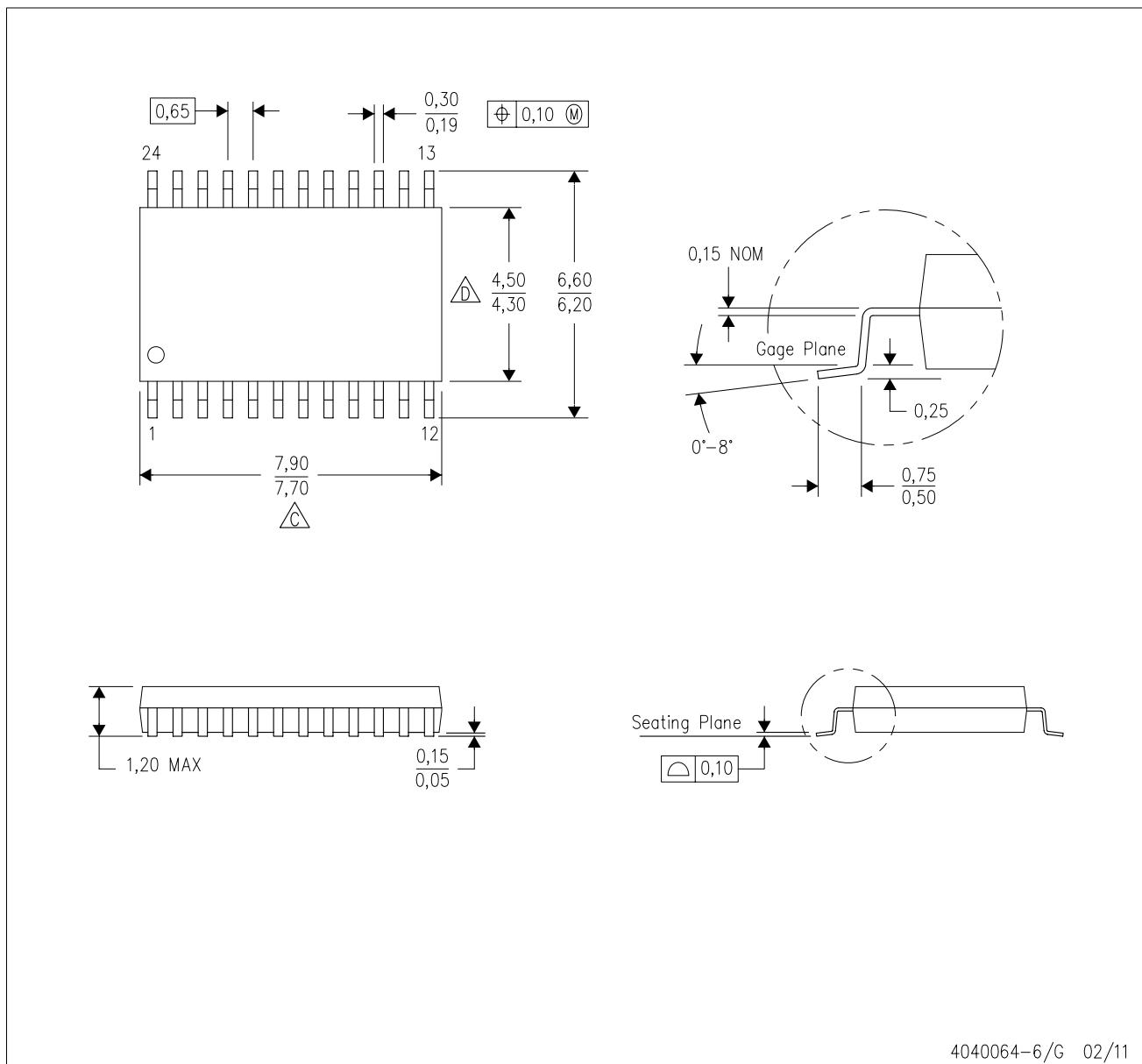


NOTES:

- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MS-013 variation AD.

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

 D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO-153

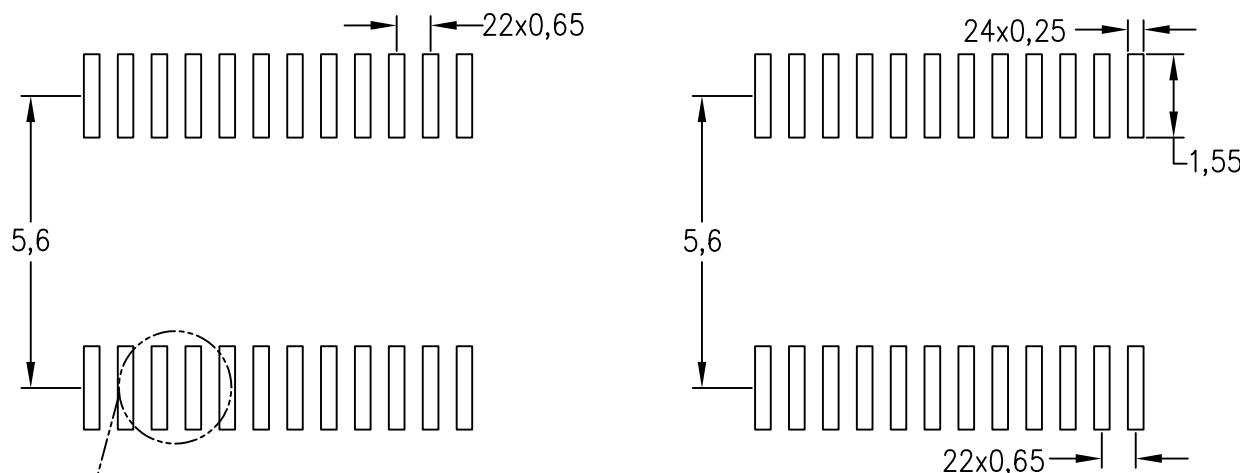
4040064-6/G 02/11

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

Example
Non Soldermask Defined PadExample
Solder Mask Opening
(See Note F)

Pad Geometry

1,6

All Around

4211284-4/E 07/12

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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