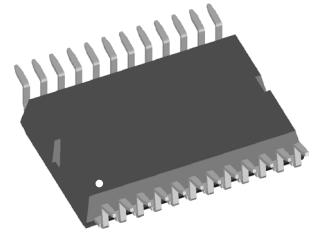
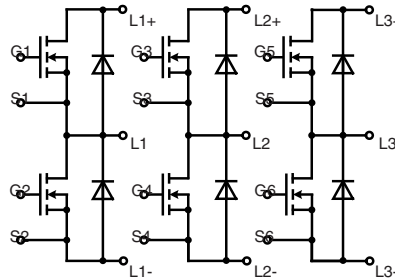


Three phase full Bridge with Trench MOSFETs in DCB isolated high current package

$V_{DSS} = 150 \text{ V}$
 $I_{D25} = 50 \text{ A}$
 $R_{DSon \text{ typ.}} = 19 \text{ m}\Omega$



MOSFETs					
Symbol	Conditions	Maximum Ratings			
V _{DSS}	T _{VJ} = 25°C to 150°C	150	V		
V _{GS}	continous	± 15	V		
	transient	± 20	V		
I _{D25}	T _C = 25°C	50	A		
I _{D90}	T _C = 90°C	38	A		
I _{D110}	T _C = 110°C	33	A		
I _{F25}	T _C = 25°C (diode)	150	A		
I _{F90}	T _C = 90°C (diode)	85	A		
I _{F110}	T _C = 110°C (diode)	65	A		
Symbol	Conditions	Characteristic Values			
(T _{VJ} = 25°C, unless otherwise specified)					
		min.	typ.	max.	
R _{DSon} ¹⁾	on chip level at V _{GS} = 10 V; I _D = 38 A	}	T _{VJ} = 25°C	19	mΩ
			T _{VJ} = 125°C	38	mΩ
V _{GS(th)}	V _{DS} = 20 V; I _D = 1 mA	2.5		4.5	V
I _{DSS}	V _{DS} = V _{DSS} ; V _{GS} = 0 V		T _{VJ} = 25°C	5	μA
			T _{VJ} = 125°C	0.5	mA
I _{GSS}	V _{GS} = ± 20 V; V _{DS} = 0 V			0.2	μA
Q _g	} V _{GS} = 10 V; V _{DS} = 75 V; I _D = 38 A		97		nC
Q _{gs}			29		nC
Q _{gd}			30		nC
C _{iss}	} V _{GS} = 10 V; V _{DS} = 25 V; f = 1 MHz		5800		pF
C _{oss}			490		pF
C _{rss}			85		pF
t _{d(on)}	} inductive load V _{GS} = 10 V; V _{DS} = 75 V I _D = 38 A; R _{G(on)} = 39 Ω; R _{G(off)} = 4.7 Ω T _J = 125°C		120		ns
t _r			50		ns
t _{d(off)}			100		ns
t _f			25		ns
E _{on}			0.25		mJ
E _{off}			0.05		mJ
E _{recoff}			0.02		mJ
R _{thJC}	with heat transfer paste (IXYS test setup)		1.3	1.0	K/W
R _{thJH}				1.6	K/W

¹⁾ $V_{DS} = I_D \cdot (R_{DS(on)} + 2R_{Pin \text{ to Chip}})$

IXYS reserves the right to change limits, test conditions and dimensions.

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Applications

AC drives

- in automobiles
 - electric power steering
 - starter generator
- in industrial vehicles
 - propulsion drives
 - fork lift drives
- in battery supplied equipment

Features

- MOSFETs in trench technology:
 - low R_{DSon}
 - optimized intrinsic reverse diode
- package:
 - high level of integration
 - high current capability
 - aux. terminals for MOSFET control
 - terminals for soldering or welding connections
 - isolated DCB ceramic base plate with optimized heat transfer
- Space and weight savings

Source-Drain Diode

Symbol	Conditions	Characteristic Values		
		min.	typ.	max.
V_{SD}	(diode) $I_F = 38\text{ A}$; $V_{GS} = 0\text{ V}$		0.85	1.0
t_{rr}	$I_F = 38\text{ A}$; $-di_F/dt = 900\text{ A}/\mu\text{s}$; $R_{G(on)} = 39\ \Omega$; $V_R = 75\text{ V}$; $T_{VJ} = 125^\circ\text{C}$		65	ns
Q_{RM}			1.6	μC
I_{RM}			40	A

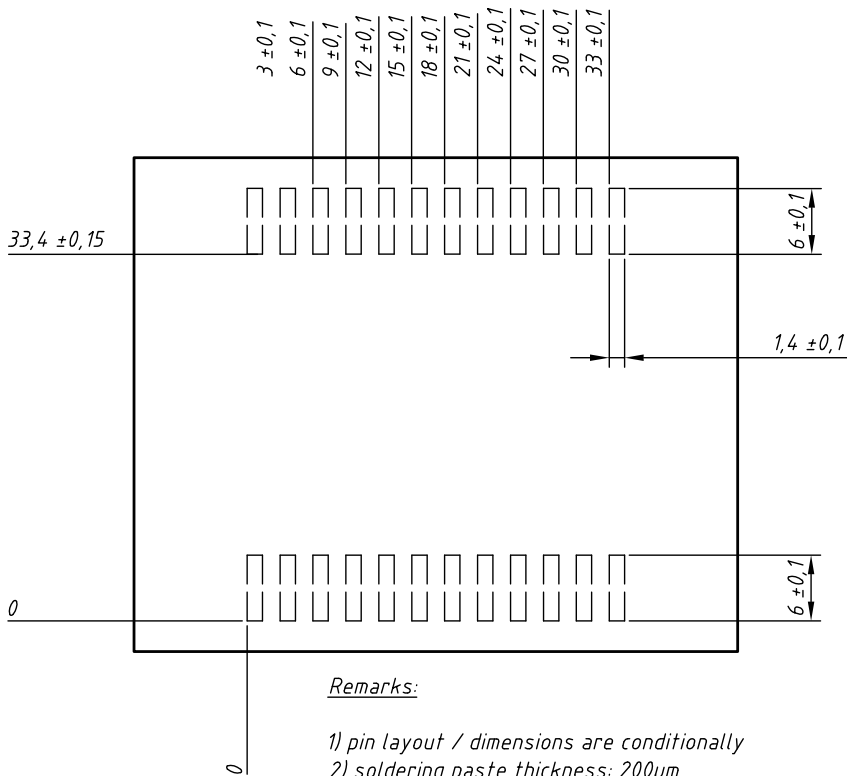
Component

Symbol	Conditions	Maximum Ratings		
I_{RMS}	per pin in main current paths (L+, L-, N-, L1, L2, L3) may be additionally limited by external connections 2 pins for output L1, L2, L3		75	A
T_J			-55...+175	$^\circ\text{C}$
T_{stg}			-55...+125	$^\circ\text{C}$
V_{ISOL}	$I_{ISOL} \leq 1\text{ mA}$, 50/60 Hz, $f = 1\text{ minute}$		1000	V~
F_c	mounting force with clip		50 - 250	N

Symbol	Conditions	Characteristic Values		
		min.	typ.	max.
$R_{pin\text{ to chip}}^{1)}$	L+ to L1/L2/L3 or L- to L1/L2/L3		0.9	$\text{m}\Omega$
C_P	coupling capacity between shorted pins and back side metallization		160	pF
Weight			13	g

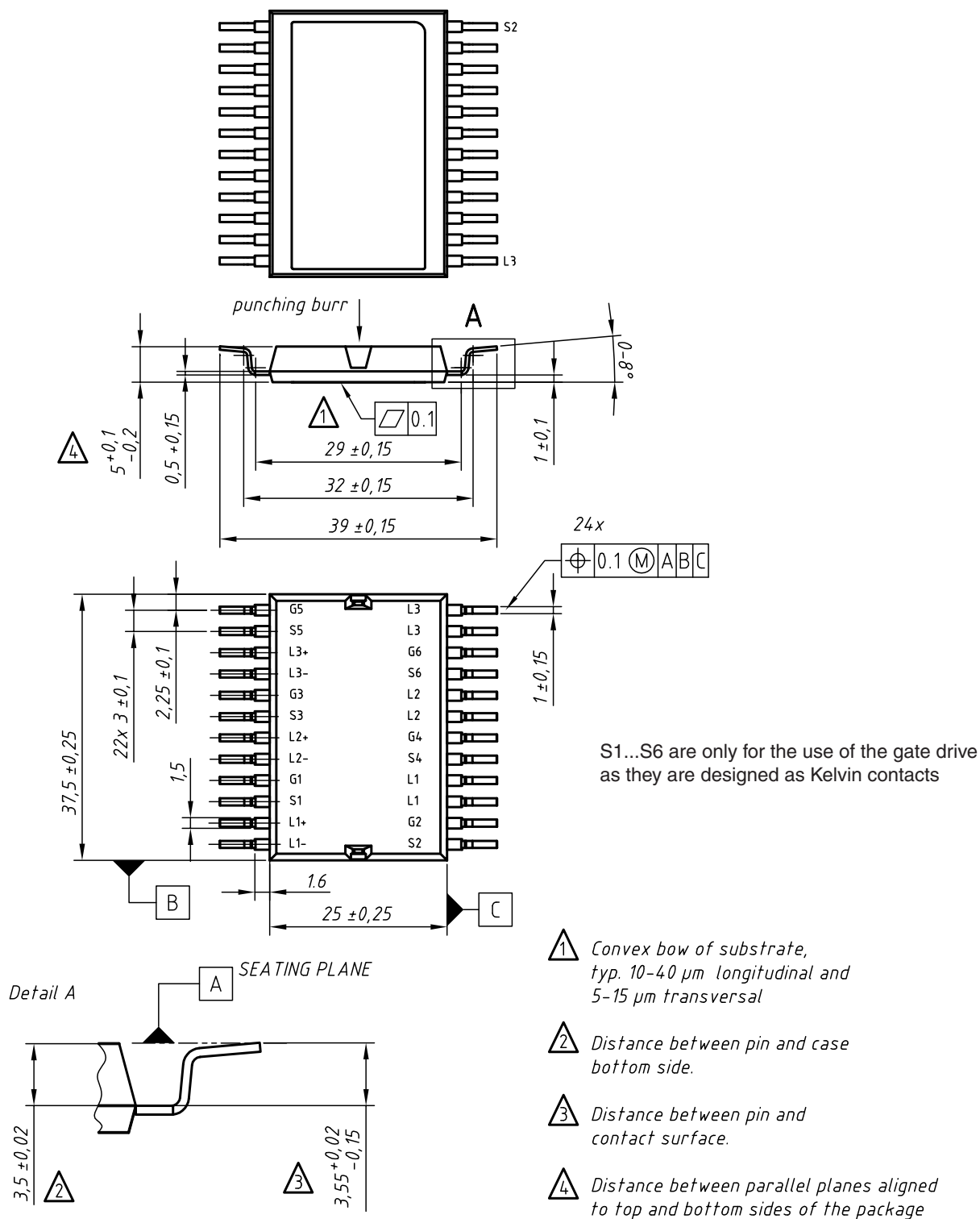
$$^1) V_{DS} = I_D \cdot (R_{DS(on)} + 2R_{Pin\text{ to Chip}})$$

Recommended printed circuit board lay-out



IXYS reserves the right to change limits, test conditions and dimensions.

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contact pin:

- galv. tin plating, per pin side: Sn 10...25 µm, undercoating Ni 0,2...1 µm
- stamping edges may be free of tin
- punching burr: ≤ 0,05mm

Leads	Ordering	Part Name & Packing Unit Marking	Part Marking	Delivering Mode	Base Qty.	Ordering Code
SMD	Standard	GMM 3x60-015X2 - SMD	GMM 3x60-015X2	Tube	13	518037

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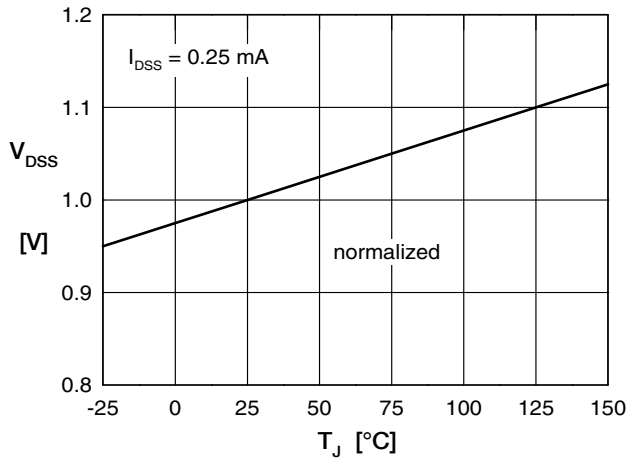


Fig.1 Drain source breakdown voltage V_{DSS} vs. junction temperature T_{J}

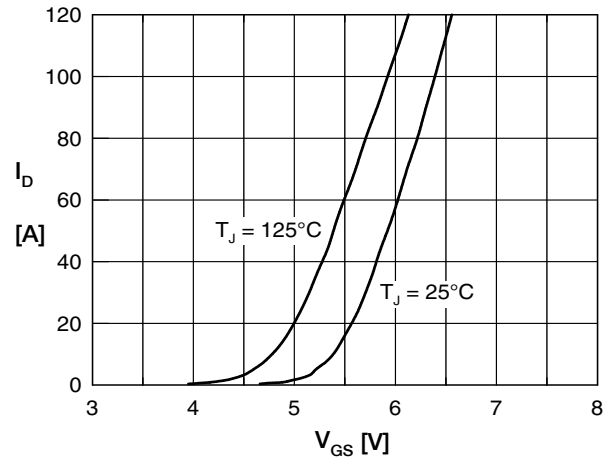


Fig. 2 Typ. transfer characteristics

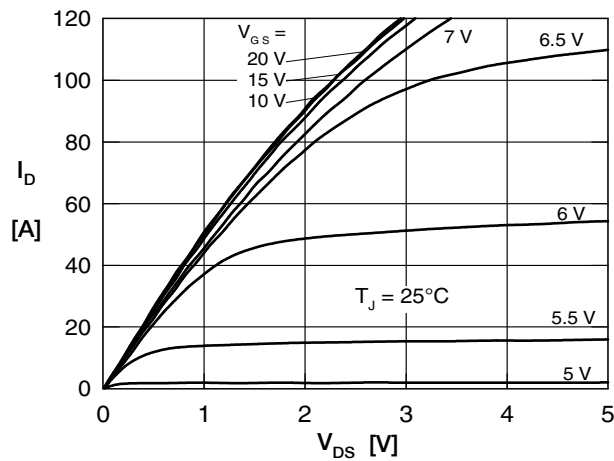


Fig. 3 Typ. output characteristics

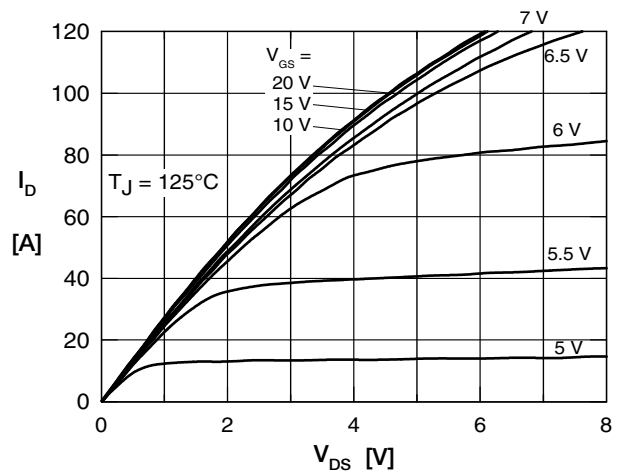


Fig. 4 Typ. output characteristics

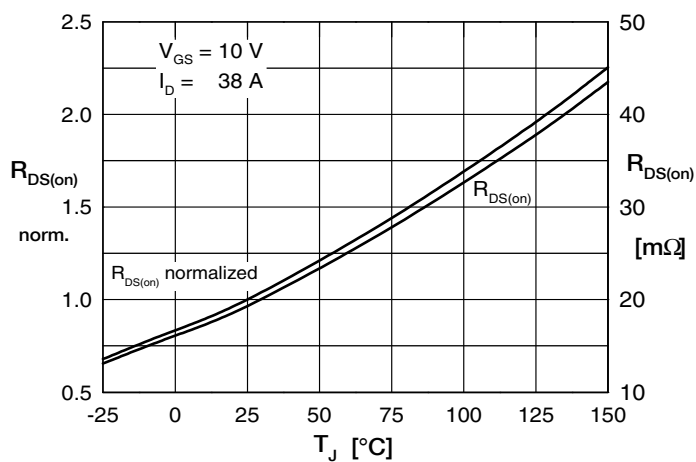


Fig.5 Drain source on-state resistance $R_{DS(on)}$ versus junction temperature T_{J}

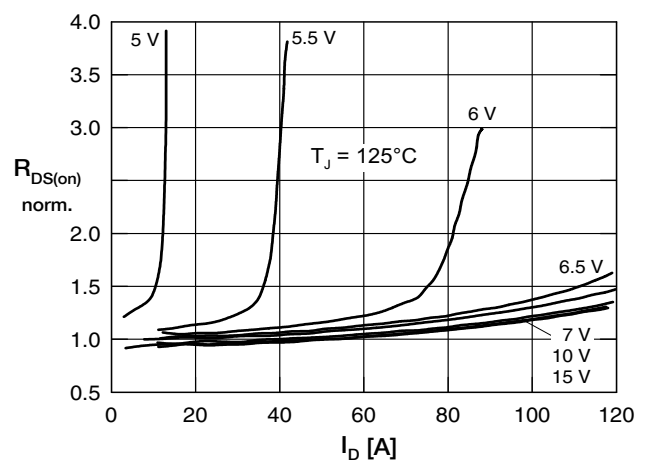


Fig. 6 Drain source on-state resistance $R_{DS(on)}$ versus I_D

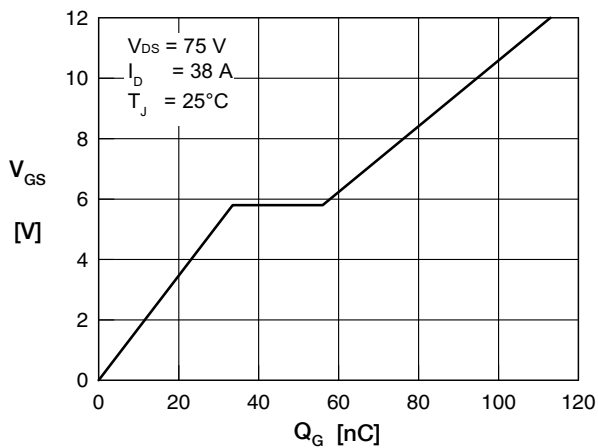


Fig. 7 Typical turn on gate charge

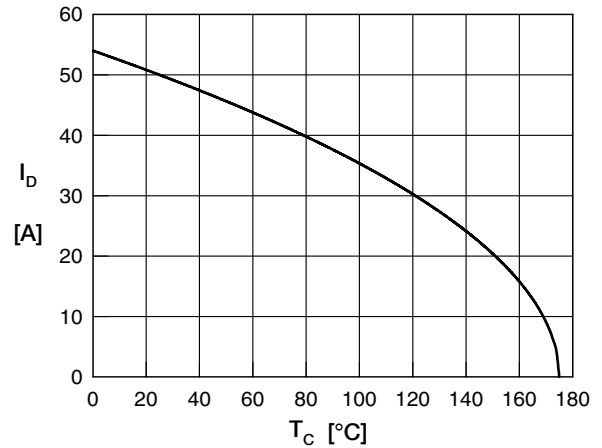


Fig. 8 Drain current I_D vs. case temperature T_C

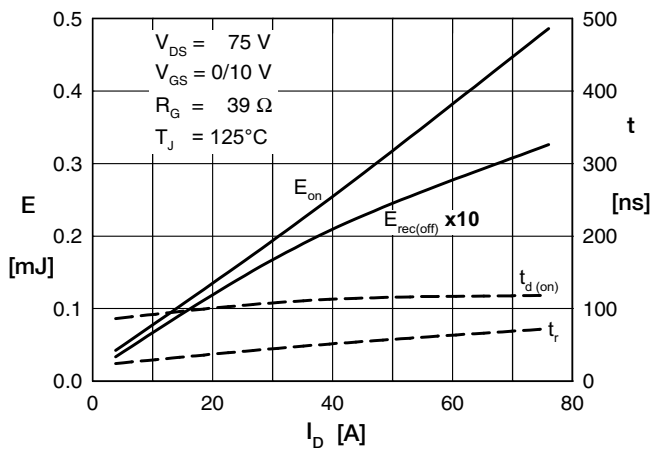


Fig. 9 Typ. turn-on energy and switching times versus drain current, inductive switching

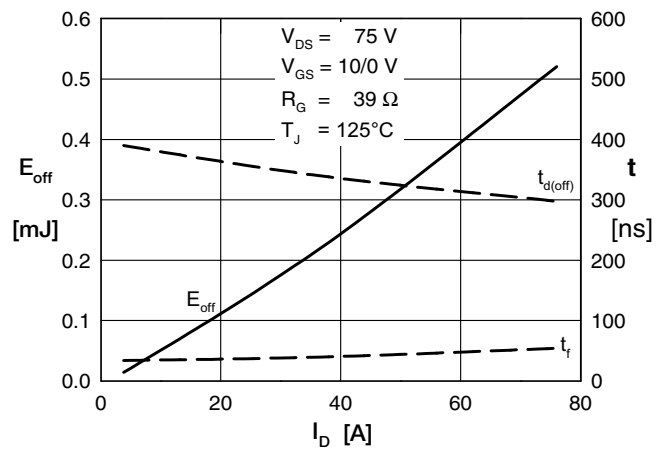


Fig. 10 Typ. turn-off energy and switching times versus drain-current, inductive switching

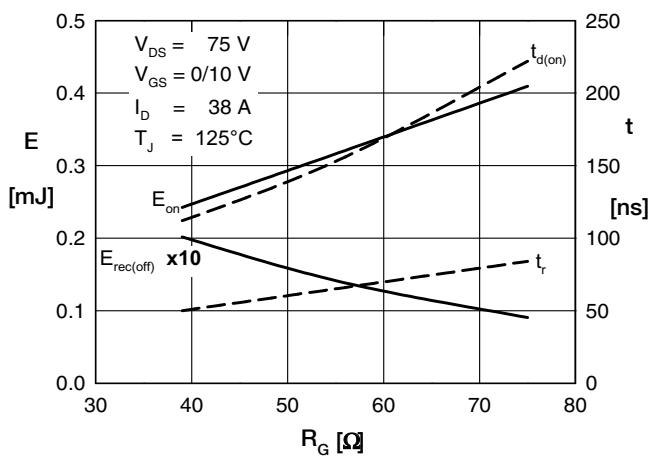


Fig. 11 Typ. turn-on energy and switching times versus gate resistor, inductive switching

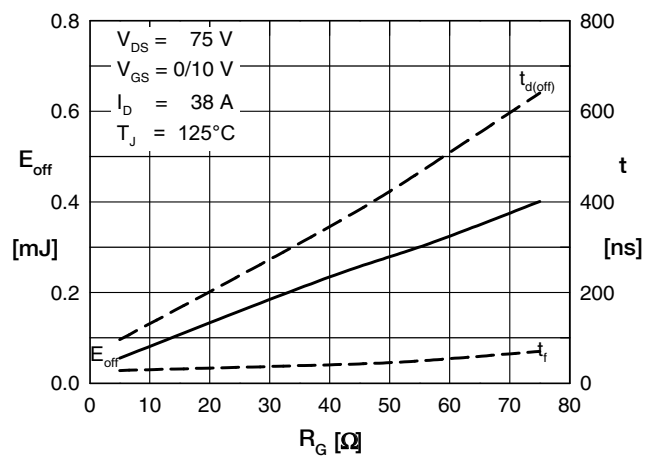


Fig. 12 Typ. turn-off energy and switching times versus gate resistor, inductive switching

