Audio Codec with Advanced Accessory Detect

General Description

The DA7219 is an ultra low-power audio codec with Advanced Accessory Detection (AAD), which supports sample rates up to 96 kHz at 24-bit resolution. It contains a mono microphone to analog to digital converter (ADC) path, and a stereo digital to analog converter (DAC) to headphone (HP) path.

AAD supports the detection and identification of 3-pole (headphone) and 4-pole (headset) jacks, and allows the automatic pin order switching of MIC/GND on CTIA or OMTP headsets. It also supports automatic multiple button detection.

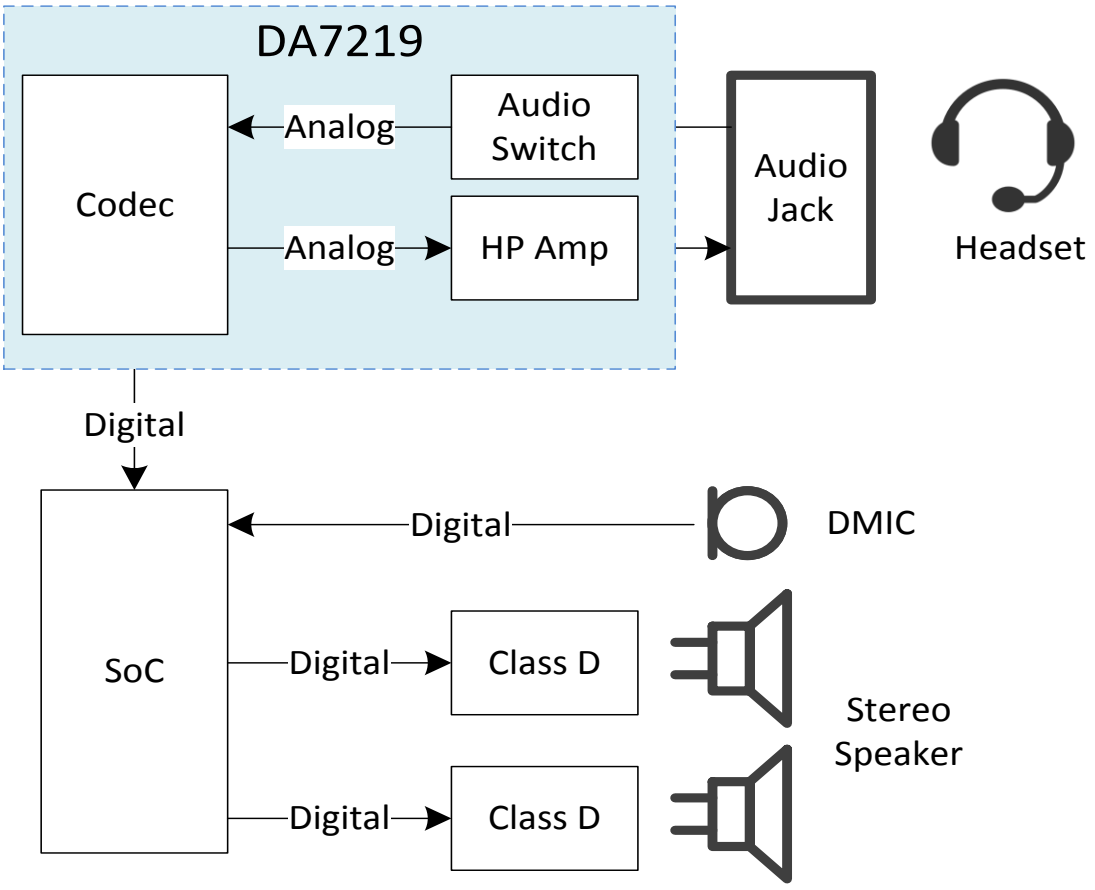
Key Features

- Android Wired Headset v1.1 compliant
- High performance mono microphone to ADC record path with 90 dB SNR
  - ADC digital filters with Audio and Voice mode high-pass characteristics
  - Low-noise microphone bias regulator with programmable output
- High performance stereo DAC to headphone playback path with 100 dB SNR
  - DAC digital filters with Audio and Voice mode high-pass cutoff and 5-band equalizer
- Advanced Accessory Detect supports
  - 3-pole and 4-pole jack detection
  - MIC/GND polarity switching
  - Multiple button detection
  - Headphone impedance testing
- Microphone input with automatic level control
- Digital sidetone path with gain
- Digital tone generator
- System controller for simplified pop-free start-up and shut-down
- Mixed sample rates of 24 kHz ADC, 48 kHz DAC supported from a single digital interface
- Sample rates of up to 96 kHz at 24-bit resolution
- Shut-down mode for very low current consumption during standby
- Phase locked loop with WCLK tracking to generate system clock
- 4-wire digital audio interface with support for I^2S, TDM and other audio formats
- 2-wire I^2C compatible interface with support for High Speed mode up to 3.4 MHz
- 4.5 mm x 1.6 mm WLCSP RouteEasy™ package for low cost PCB manufacture

Applications

- Chromebooks
- Portable audio applications
- Tablets and eBooks
- All digital distributed systems
- Headphone accessories
- Remote controllers
- Gaming controllers

System Diagram



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1 Terms and Definitions

AAD	Advanced Accessory Detect
ADC	Analog to Digital Converter
ALC	Automatic Level Control
CMRR	Common Mode Rejection Ratio
CTIA	Cellular Telecommunications Industry Association, (now known as 'The Wireless Association')
DAC	Digital to Analog Converter
DAI	Digital Audio Interface
DMIC	Digital Microphone
DTMF	Dual Tone Multi Frequency
EQ	Equalizer
FS	Sample Rate
HP	Headphones
HPF	High-Pass Filter
I^2C	Inter-Integrated Circuit Interface
I^2S	Inter-Integrated Circuit Sound
LDO	Low Dropout Regulator
MCLK	Master Clock
OMTP	Open Mobile Terminals Platform
PC	Program Counter
PGA	Programmable Gain Amplifier
PLL	Phase Locked Loop
PSRR	Power Supply Rejection Ratio
SC	System Controller
SDM	Sigma Delta Modulator
SNR	Signal to Noise Ratio
SRM	Sample Rate Matching
SWG	Sine Wave Generator
TDM	Time Division Multiplexing
THD+N	Total Harmonic Distortion plus Noise
VCO	Voltage-Controlled Oscillator
WCLK	Word Clock

1.1 Terminology

Crosstalk (dB)

The level difference between the active path output and the idle path measured signal level, at the test signal frequency. The active path is configured and supplied with an input signal capable of driving a full scale output, with the signal measured at the output of the specified idle path.

Mute Attenuation

The difference in level between the full scale output signal and the output with mute applied.

Channel Separation (dB) [left-to-right and right-to-left]

The difference in level between the active channel (driven to maximum full scale output) and the signal level measured in the idle channel at the test signal frequency. The active channel is configured and supplied with an input signal capable of driving a full scale output, with the signal measured at the output of the associated idle channel.

PSRR

The ratio of a given power supply change relative to the output signal that results from it. PSRR is measured under quiescent signal path conditions.

SNR

The difference in level between the maximum full scale output signal and the output with no input signal applied.

THD+N

The level of the rms value of the sum of harmonic distortion products plus noise in the specified bandwidth relative to the amplitude of the measured output signal.

All performance measurements carried out with 20 kHz low pass filter, and where noted an A-weighted filter. Failure to use such a filter will result in higher THD and lower SNR readings than are found in the Electrical Characteristics. The low-pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.

2 References

[1] Android Wired Audio Headset Specification (v1.1)
(https://source.android.com/accessories/headset/specification.html)

3 Block Diagram

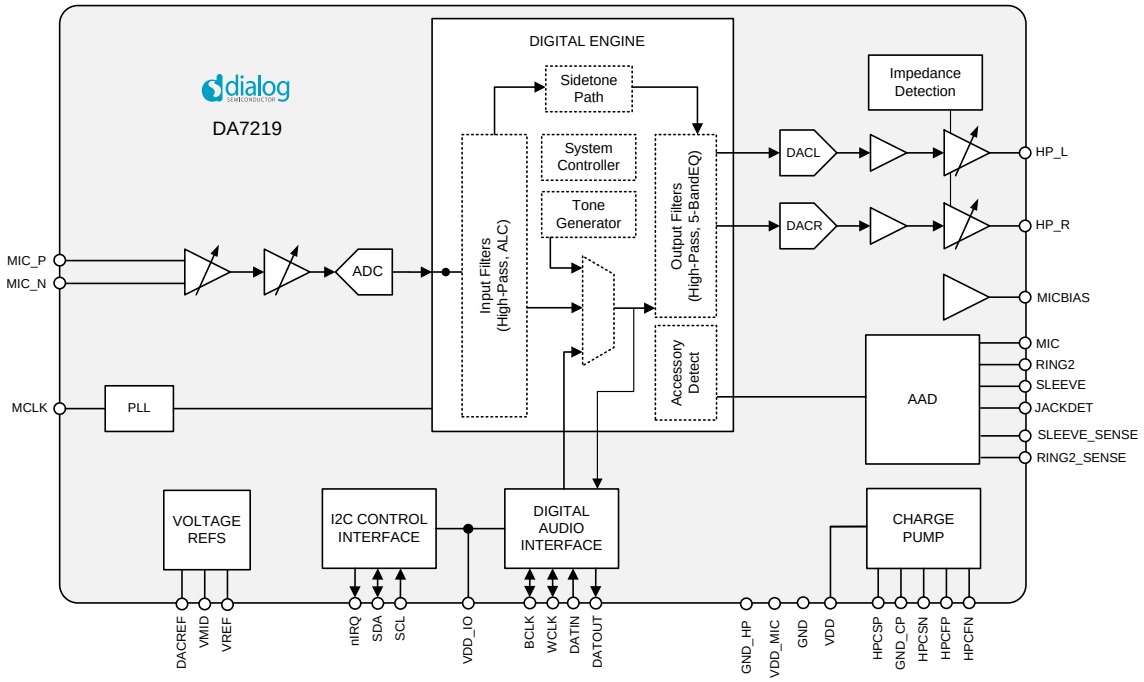

Figure 2: DA7219 Block Diagram

4 Ballout

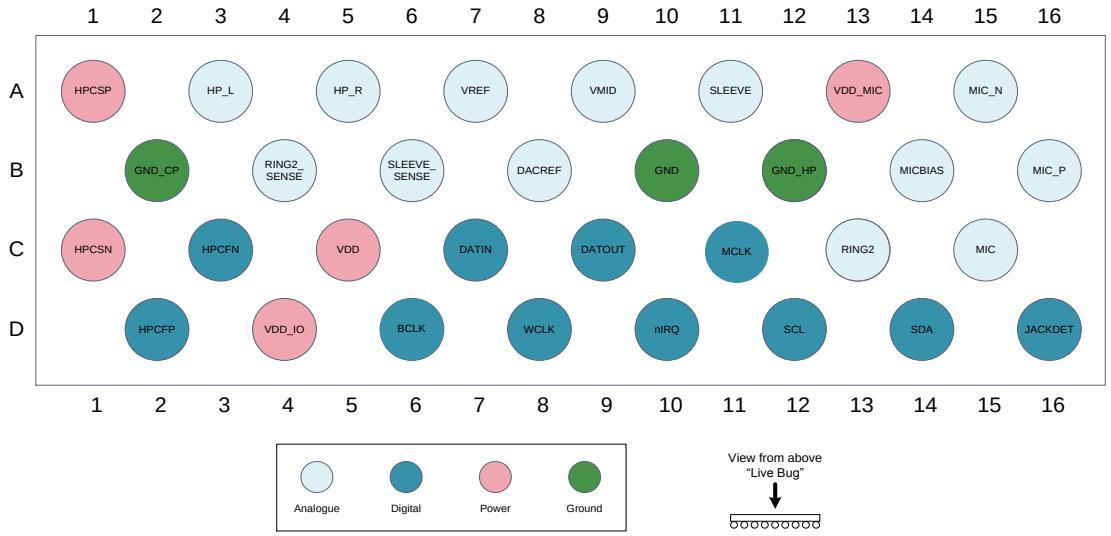

Figure 3: DA7219 Ballout Diagram

Table 1: Ball Description

Ball No.	Ball/Pin Name	Type (Table 2)	Description
Microphone Inputs			
B16	MIC_P	AI	Differential analog microphone 1 input (Pos)
A15	MIC_N	AI	Differential analog microphone 1 input (Neg)
B14	MICBIAS	AO	Microphone bias output
Accessory Detect			
D16	JACKDET	DI	Jack Detect Input from socket
A11	SLEEVE	AIO	Socket Sleeve (configured as MIC or GND)
C13	RING2	AIO	Socket Ring 2 (configured as GND or MIC)
B6	SLEEVE_SENSE	AIO	Socket Sleeve (Sense)
B4	RING2_SENSE	AIO	Socket Ring 2 (Sense)
C15	MIC	AIO	Microphone DC input
Headphone Outputs			
A3	HP_L	AO	Single-ended headphone output (Left)
A5	HP_R	AO	Single-ended headphone output (Right)
Charge Pump			
A1	HPCSP	AIO	Charge pump reservoir capacitor (Positive)
C1	HPCSN	AIO	Charge pump reservoir capacitor (Negative)
D2	HPCFP	AIO	Charge pump flying capacitor (Positive)
C3	HPCFN	AIO	Charge pump flying capacitor (Negative)
Digital Interface			
D14	SDA	DIOD	I^2C bidirectional data
D12	SCL	DI	I^2C clock

Ball No.	Ball/Pin Name	Type (Table 2)	Description
D10	nIRQ	DIOD	Interrupt output (open drain active low)
C7	DATIN	DIO	DAI data input to DA7219
C9	DATOUT	DIO	DAI data output from DA7219
D6	BCLK	DIO	DAI bit clock
D8	WCLK	DIO	DAI word clock
C11	MCLK	DI	Master clock input
References			
B8	DACREF	AIO	DAC reference decoupling capacitor
A9	VMID	AIO	Mid-rail reference decoupling capacitor
A7	VREF	AIO	Bandgap reference decoupling capacitor
Supplies			
C5	VDD	AI	Main analog and digital supply
A13	VDD_MIC	AI	Supply for MICBIAS LDO
D4	VDD_IO	AI	Supply for digital interfaces
Grounds			
B2	GND_CP	AI	Ground
B10	GND	AI	Ground
B12	GND_HP	AI	Ground

Table 2: Ball/Pin Type Definition

Ball/Pin Type	Description	Ball/Pin Type	Description
DI	Digital Input	AI	Analog Input
DIO	Digital Input/Output	AO	Analog Output
DIOD	Digital Input/Output open Drain	AIO	Analog Input/Output

5 Pin Descriptions

5.1 Microphone Pins

5.1.1 MIC_P

MIC_P is the positive differential input for the analog microphone channel. It can be used as a single-ended input if MIC_N is grounded (see

Figure 7).

5.1.2 MIC_N

MIC_N is the negative differential input for the analog microphone channel. It should be grounded when using a single-ended analog microphone configuration.

5.1.3 MICBIAS

MICBIAS is the internally generated microphone supply. This must be decoupled with a 1 µF capacitor.

5.2 Accessory Detect Pins

5.2.1 JACKDET

JACKDET is used to signal to the device when the Jack is fully inserted into the 3.5 mm jack (or alternative) socket.

The JACKDET pin is designed to be pulled either HIGH or LOW on the insertion of the jack. If using an HPLDET type headset socket additional external circuitry is required.

If not required it should be left unconnected.

5.2.2 SLEEVE

Sleeve is tested during the sense stage and then configured as either the headset microphone input or the headset ground connection.

5.2.3 RING2

RING2 is tested during the sense stage and then configured as either the headset microphone input or the headset ground connection.

5.2.4 SLEEVE_SENSE

SLEEVE sense line to guarantee accuracy over distance, cables and connectors.

5.2.5 RING2_SENSE

RING2 sense line to guarantee accuracy over distance, cables and connectors.

5.2.6 MIC

MIC is the DC input for the analog accessory detect.

5.3 Interface Input Pins

5.3.1 MCLK

MCLK is the master clock input pin. It is used as the main system clock either directly or via the PLL.

5.3.2 SCL

SCL is the Control Interface (I^2C) clock input and is used in conjunction with SDA to control the device.

5.3.3 DATIN

DATIN is the data input pin which forms part of the Digital Audio Interface (DAI). It is used to present audio playback data to the device.

5.4 Interface Output Pins

5.4.1 nIRQ

nIRQ is the open drain active-low interrupt output to alert the host to either an accessory or a level detect event.

5.4.2 DATOUT

DATOUT is the data output pin which forms part of the DAI. It is used to present audio record data to the host.

5.5 Interface Bidirectional Pins

5.5.1 SDA

SDA is the Control Interface (I^2C) data input/output and is used in conjunction with SCL to control the device.

5.5.2 BCLK

BCLK is the bit clock input/output pin which forms part of the DAI. It is used to clock audio data bits into or out from the device or both.

5.5.3 WCLK

WCLK is the word clock input/output pin which forms part of the DAI. It is used to indicate whether the data bits belong to the left or right audio channel.

5.6 Headphone Output Pins

5.6.1 HP_L

HP_L is the left-channel single-ended headphone output. It is ground-centered so the headphone speaker can be connected directly between HP_L and ground.

5.6.2 HP_R

HP_R is the right-channel single-ended headphone output. It is ground-centered so the headphone speaker can be connected directly between HP_R and ground.

5.7 Charge Pump Pins

5.7.1 HPCSP

HPCSP is the positive output from the headphone charge pump. It should be connected to GND_CP via a reservoir capacitor.

5.7.2 HPCSN

HPCSN is the negative output from the headphone charge pump. It must be connected to GND_CP via a reservoir capacitor.

5.7.3 HPCFP

HPCFP is one of the flying capacitor connections required by the headphone charge pump. It must be connected to HPCFN via a capacitor.

5.7.4 HPCFN

HPCFN is one of the flying capacitor connections required by the headphone charge pump. It must be connected to HPCFP via a capacitor.

5.8 References

5.8.1 VMID

VMID is the mid-rail reference decoupling capacitor connection.

5.8.2 DACREF

DACREF is the DAC reference decoupling capacitor connection.

5.8.3 VREF

VREF is the bandgap reference decoupling capacitor connection.

5.9 Supply Pins

5.9.1 VDD

VDD is main analog supply pin. It supplies all the analog circuits except the MICBIAS output and the HPAMP outputs.

5.9.2 VDD_IO

VDD_IO is the supply pin for the digital input/output signals. VDD_IO must be greater than or equal to VDD during device operation.

5.9.3 VDD_MIC

VDD_MIC is the supply pin for the MICBIAS. VDD_MIC must be greater than or equal to VDD during device operation.

5.10 Ground Pins

5.10.1 GND

GND is the main analog ground pin. It is the ground connection for all analog circuits with the exception of the charge pump.

5.10.2 GND_CP

GND_CP is the ground pin for the charge pump and the digital engine.

5.10.3 GND_HP

GND_HP is the ground point for the headset. When a headset is connected this pin is automatically connected internally to either RING2 or SLEEVE.

6 Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings

Parameter	Description	Conditions (Note 1)	Min	Max	Unit
T_{STG}	Storage temperature		–65	+165	°C
T_a	Operating temperature		–40	+85	°C
V_{DD_LIM}	Main supply voltage		–0.3	+2.75	V
V_{VDD_IO}	Digital IO supply voltage		–0.3	+5.5	V
V_{DD_MIC}	Microphone bias supply voltage		–0.3	+5.5	V
V_{DDIO}	Digital IO pins: SDA, SCL, BCLK, WCLK, DATIN, DATOUT, MCLK		–0.3	V_{DD_IO} + 0.3	V
$V_{JACKDET}$	Accessory detect pins: JACKDET		–0.3	V_{DD} + 0.3	V
V_{ACCDET}	Accessory detect pins: RING2, SLEEVE, MIC, RING2_SENSE, SLEEVE_SENSE		–0.3	V_{DD_MIC} + 0.3	V
V_{MIC_P}, V_{MIC_N}	Analog input pins MIC_P and MIC_N		–0.3	V_{DD} + 0.3	V
V_{ESD_HBM}	ESD susceptibility	Human body model (HBM)	2000		V
V_{ESD_CDM}	ESD susceptibility	Charged device model (CDM)	500		V

Note 1 Stresses beyond those listed under ‘Absolute Maximum Ratings’ may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_a	Operating temperature		–25		85	°C
V_{DD}	Main supply voltage		1.7		2.5	V
V_{DD_IO}	Digital IO supply voltage	(Note 1)	VDD		3.6	V
V_{DD_MIC}	Microphone bias supply voltage	(Note 1)	VDD		3.6	V

Note 1 V_{DD_IO} and V_{DD_MIC} must be greater than or equal to V_{DD}.

8 Electrical Characteristics

Unless otherwise stated, test conditions are as follows: V_{DD} = V_{DD_IO} = 1.8 V, V_{DD_MIC} = 3.3 V, MCLK = 12.288 MHz, SR = 48 kHz, PLL = Bypass mode, T_a = 25 ºC.

Table 5: Power Consumption

Description	Conditions	Min	Typ	Max	Unit
DEEP SLEEP mode			4	10	µA
SLEEP mode	AAD on without button detection		185		µA
Digital playback to headphone, no load	DAC to HP_L/R, quiescent		3.4		mW
Digital playback to headphone, with load	DAC to HP_L/R, 16 Ω load, 0.1 mW at 0 dBFS		7.5		mW
Microphone stereo record	MIC P/N to ADCL/R		2.75		mW
Microphone stereo record and digital playback to headphone, no load	MIC P/N to ADCL/R and DACL/R to HP_L/R, quiescent		4.8		mW
Microphone stereo record and digital playback to headphone, with load	MIC P/N to ADCL/R and DACL/R to HP_L/R, 16 Ω load, 0.1 mW at 0 dBFS		8.9		mW

Table 6: Microphone Bias

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{MICBIAS}$	Output voltage	No load, V_{DD_MIC} > $V_{MICBIAS}$ + 200 mV Level programmable using micbias1_level	1.6		2.9	V
I_{BIAS}	Output current	Output voltage droop < 50 mV		2		mA
PSRR	Power supply rejection ratio	20 Hz to 2 kHz 2 kHz to 20 kHz	70 50			dB
V_{NO}	Output voltage noise	$V_{MICBIAS}$ ≤ 2.2 V		5		μV_{RMS}

Table 7: Microphone Amplifier

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Full-scale input signal	0 dB, singled-ended 0 dB gain, differential		0.8*V_{DD} 1.6*V_{DD}		V_{PP}
	Input resistance		12	15	18	kΩ
	Programmable gain		−6		36	dB
	Gain step size			6		dB
	Absolute gain accuracy	0 dB @ 1 kHz	-1.0		1.0	dB
	Gain step error	20 Hz to 20 kHz	-0.1		0.1	dB
VNI	Input noise level	Inputs connected to GND, 24 dB gain, input-referred, A-weighted		5		μV_{RMS}
	Amplitude ripple	20 Hz to 20 kHz	-0.5		0.5	dB
PSRR	Power supply rejection ratio	20 Hz to 2 kHz 2 kHz to 20 kHz	90 70			dB

Parameter	Description	Conditions	Min	Typ	Max	Unit
CMRR	Common mode rejection ratio			70		dB

Table 8: Input Mix Amplifier (mixinamp)

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Programmable gain		−4.5		+18	dB
	Gain step size			1.5		dB
	Absolute gain accuracy	0 dB @ 1 kHz	-1.0		+1.0	dB
	Gain step error	20 Hz to 20 kHz	-0.1		+0.1	dB
	Amplitude ripple	20 Hz to 20 kHz	-0.5		+0.5	dB

Table 9: Mono Analog to Digital Converter (adc_mono)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{MAX}	Full-scale input signal	0 dBFS digital output level		1.6*V_{DD}		V_{PP}
SNR	Signal to noise ratio	A-weighted		90		dB
THD+N	Total harmonic distortion plus noise	-1 dBFS analog input level		-85		dB
PSRR	Power supply rejection ratio	20 Hz to 2 kHz 2 kHz to 20 kHz	70 50			dB

Table 10: Stereo Digital to Analog Converter (dac_stereo)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{MAX}	Full-scale output signal	0 dBFS digital input level		1.6*V_{DD}		V_{PP}
SNR	Signal to Noise Ratio	A-weighted		100		dB
THD+N	Total harmonic distortion plus noise	-1 dBFS digital input level		-90		dB
PSRR	Power supply rejection ratio	20 Hz to 2 kHz 2 kHz to 20 kHz	70 50			dB

Table 11: Stereo Headphone Amplifier (audio_hpamp_stereo)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{MAX}	Full-scale output signal	No load		1.6*V_{DD}		V_{PP}
	DC output offset	−30 dB gain		250		µV
	Maximum output power per channel	V_{DD} = 1.8 V, THD < 0.1%, R_{LOAD} = 16 Ω, 1 kHz		30		mW_{RMS}
	Maximum output power per channel	V_{DD} = 2.5 V, THD < 0.1%, R_{LOAD} = 16 Ω, 1 kHz		70		mW_{RMS}
	Load resistance		13	16		Ω
	Load capacitance				500	pF
	Load inductance				400	µH
Frequency Response	20 Hz to 20 kHz		-0.5		+0.5	dB
SNR	Signal to Noise Ratio	V_{DD} = 1.8 V, 0 dB gain		98		dB

Parameter	Description	Conditions	Min	Typ	Max	Unit
		V_{DD} = 2.5 V, 0 dB gain		100		dB
V_{NO}	Output noise level	20 Hz to 20 kHz, <20 dB gain			2.5	μV_{RMS}
THD+N	Total harmonic distortion plus noise	V_{DD} = 1.8 V, R_{LOAD} = 16 Ω, -5 dBFS, 1 kHz		−85		dB
	Channel separation	V_{DD} = 1.8 V, R_{LOAD} = 32 Ω, 1 kHz		90		dB
	Programmable gain		−57		6	dB
	Gain step size			1.0		dB
	Absolute gain accuracy	0 dB @ 1 kHz	−0.8		0.8	dB
	Left/right gain mismatch	20 Hz to 20 kHz	−0.1		0.1	dB
	Gain step error	20 Hz to 20 kHz	−0.1		0.1	dB
	Amplitude ripple	20 Hz to 20 kHz	−0.5		0.5	dB
	Mute attenuation			−70		dB
PSRR	Power supply rejection ratio	20 Hz to 2 kHz 2 kHz to 20 kHz	70 50			dB

Table 12: Input Filters

Parameter	Description	Conditions	Min	Typ	Max	Unit
BPASS	Pass band				0.45*FS	Hz
	Pass band ripple	Voice mode Music mode			±0.3 ±0.1	dB
BSTOP	Stop band	FS ≤ 48 kHz FS = 88.2 kHz or 96 kHz	0.56*FS		7*FS 3.5*FS	Hz
	Stop band attenuation	Voice mode Music mode	70 55			dB
	Group delay	Voice mode Music mode FS = 88.2 kHz or 96 kHz		4.3/FS 18/FS 9/FS		s
	Digital gain		-83.25		12	dB
	Digital gain step size			0.75		dB

Table 13: DAC Filter

Parameter	Description	Conditions	Min	Typ	Max	Unit
BPASS	Pass band				0.45*FS	Hz
	Pass band ripple	Voice mode Music mode			±0.3 ±0.1	dB
BSTOP	Stop band	FS ≤ 48 kHz FS = 88.2 kHz or 96 kHz	0.56*FS		7*FS 3.5*FS	Hz
	Stop band attenuation	Voice mode Music mode	70 55			dB

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Group delay	Voice mode Music mode FS = 88.2 kHz or 96 kHz		4.3/FS 18/FS 9/FS		s
	Group delay variation	20 Hz to 20 kHz			1	µs
	Left/right channel group delay mismatch				2	µs
	Digital gain range		-71.25		18	dB
	Digital gain step size			0.75		dB

Table 14: Automatic Level Control (ALC)

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Attack rate	FS = 48 kHz	1.6		6500	dB/s
	Release rate	FS = 48 kHz	1.6		1675	dB/s
	Hold time	FS = 48 kHz	1.3		42300	ms
	Maximum threshold		−94.5		0	dBFS
	Minimum threshold		−94.5		0	dBFS
	Noise threshold		−94.5		0	dBFS
	Threshold step size			1.5		dB
	Maximum overall gain		0		90	dB
	Maximum overall attenuation		0		90	dB
	Maximum analog gain		0		36	dB
	Minimum analog gain		0		36	dB
	Gain step size			1.5		dB

Table 15: Advanced Accessory Detect (AAD)

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Ring2 ground switch resistance				50	mΩ
	Sleeve ground switch resistance				50	mΩ

Table 16: Reference Voltages

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{REF}	Bandgap voltage reference			1.2		V
DACREF	DAC reference			0.9*V_{DD}		V
V_{MID}	Mid-rail voltage reference			0.45*V_{DD}		V
	Charge pump positive voltage	VDD mode		1.8		V
		VDD/2 mode		0.9		V
	Charge pump negative voltage	VDD mode		-1.8		V
		VDD/2 mode		-0.9		V

Table 17: PLL Mode

Description	Conditions	Min	Typ	Max	Unit
MCLK input jitter	Absolute jitter (rms) Note 1			540	ps
MCLK input frequency	Normal mode	2		54	MHz
SRM tracking range	DAI slave mode WCLK frequency variation	-4		4	%
SRM tracking rate	DAI slave mode WCLK drift rate			54	ppm/s

Note 1 Jitter in the 100 Hz to 40 kHz band

Table 18: Bypass Mode

Description	Conditions	Min	Typ	Max	Unit
MCLK input jitter	Absolute jitter (rms) Note 1			540	ps
MCLK input frequency	F_S = 11.025, 22.05, 44.1, 88.2 kHz F_S = 8, 12, 16, 24, 32, 48, 96 kHz		11.2896 12.288		MHz

Note 1 Jitter in the 100 Hz to 40 kHz band

Table 19: Tone Generator

Description	Conditions	Min	Typ	Max	Unit
Single-tone frequency	F_S = 8, 12, 16, 24, 32, 48, 96 kHz F_S = 11.025, 22.05, 44.1, 88.2 kHz	1 1		12000 11025	Hz
Single-tone frequency step	F_S = 8, 12, 16, 24, 32, 48, 96 kHz F_S = 11.025, 22.05, 44.1, 88.2 kHz		0.18 0.17		Hz
Dual-tone modulation frequency A			697 770 852 941		Hz
Dual-tone modulation frequency B			1209 1336 1477 1633		Hz
Output programmable gain	Programmable via tone_gen_gain	-45		0	dBFS
On/off pulse duration		10		2000	ms
On/off pulse step size	10 ms to 200 ms duration 200 ms to 2000 ms duration		10 50		ms
On/off pulse repeat	Programmable Continuous		1, 2, 3, 4, 5, 6 ∞		Cycles

9 Digital Interfaces

Table 20: Digital I/O Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	SCL, SDA, MCLK, BCLK, WCLK, DATIN, DATOUT, AD Input HIGH voltage		0.7 * V_{DD_IO}			V
V_{IL}	SCL, SDA, MCLK, BCLK, WCLK, DATIN, DATOUT Input LOW voltage				0.3 * V_{DD_IO}	V
V_{OL}	SDA, nIRQ Output LOW voltage	I_{OUT} = 3 mA			0.24	V

10 Timing Characteristics

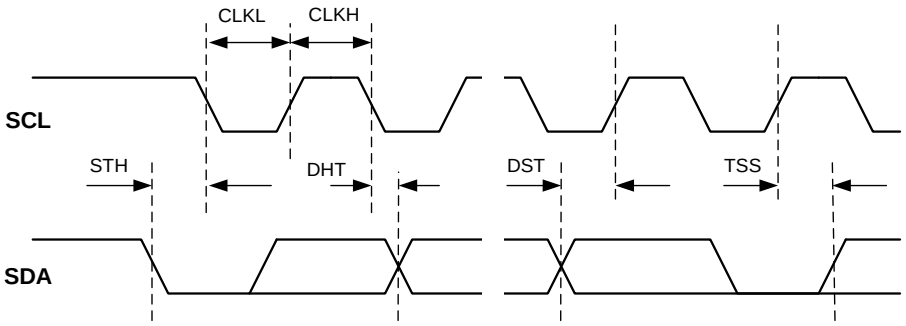

Figure 4: I²C Bus Timing

Table 21: I²C Control Bus (V_{DD_IO} = 1.8 V)

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Bus free time STOP to START		500			ns
	Bus line capacitive load				150	pF
Standard/Fast Mode						
	SCL clock frequency		0		1000	kHz
	Start condition setup time		260			ns
STH	Start condition hold time		260			ns
CLKL	SCL low time		500			ns
CLKH	SCL high time		260			ns
	SCL rise/fall time	Input requirement			1000	ns
	SDA rise/fall time	Input requirement			300	ns
DST	SDA setup time		50			ns
DHT	SDA hold time		0			ns
TSS	Stop condition setup time		260			ns
High-Speed Mode						
	SCL clock frequency		0		3400	kHz
	Start condition setup time		160			ns
STH	Start condition hold time		160			ns
CLKL	SCL low time		160			ns
CLKH	SCL high time		60			ns
	SCL rise/fall time	Input requirement			160	ns
	SDA rise/fall time	Input requirement			160	ns
DST	SDA setup time		10			ns
DHT	SDA hold time		0			ns
TSS	Stop condition setup time		160			ns

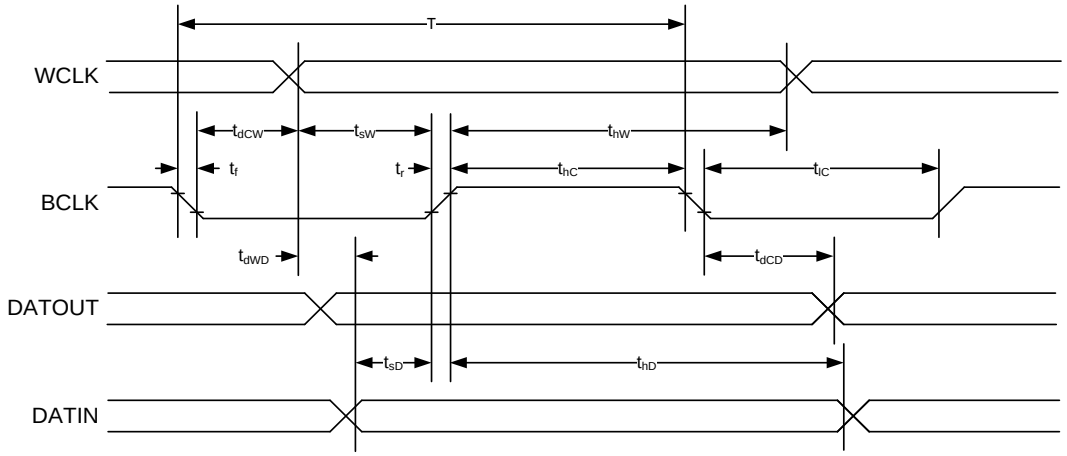

Figure 5: Digital Audio Interface Timing Diagram

NOTE
Diagram shown is valid for all modes except DSP. For DSP mode the BCLK signal is inverted

Table 22: Digital Audio Interface Timing (I^2S/DSP in Master/Slave Mode)

Parameter	Description	Conditions (V_{DD_IO} = 1.8 V)	Min	Typ	Max	Unit
	Input impedance	DC impedance > 10 MΩ	300 1.0		 2.5	Ω pF
T	BCLK period		75			ns
t_r	BCLK rise time				8	ns
t_f	BLCK fall time				8	ns
t_{hC}	BCLK high period		40 %		60 %	T
t_{lC}	BCLK low period		40 %		60 %	T
t_{dCW}	BCLK to WCLK delay		-30 %		+30 %	T
t_{dCD}	BCLK to DATOUT delay		-30 %		+30 %	T
t_{hW}	WCLK high time	DSP mode	100 %			T
		Non-DSP mode	Word length (Note 1)			T
t_{lW}	WCLK low time	DSP mode	100 %			T
		Non-DSP mode	Word length (Note 2)			T
t_{sW}	WCLK setup time	Slave mode	7			ns
t_{hW}	WCLK hold time	Slave mode	2			ns
t_{sD}	DATIN setup time		7			ns
t_{hD}	DATIN hold time		2			ns
t_{dWD}	DATOUT to WCLK delay		DATOUT is synchronized to BCLK			

Note 1 WCLK must be high for at least the word length number of BCLK periods

Note 2 WCLK must be low for at least the word length number of BCLK periods

11 Functional Description

DA7219 is a high-performance, low-power audio codec with in-built Advanced Accessory Detection (AAD). The AAD supports the detection of 3-pole (headphone or lineout) or 4-pole (headset) jacks, with automatic pin order switching of MIC/GND on CTIA and OMTP headsets.

The DA7219 contains a mono analog microphone-to-ADC path and a DAI for input and output. The DAC to headphone path has a ground-centered, single-ended stereo headphone output.

The digital core has an input filter with a high-pass filter (HPF), and automatic level control (ALC), while the output filter has an HPF, and a 5-band equalizer (EQ).

There is also a sidetone path with gain and a tone generator that supports Dual Tone Multi-Frequency (DTMF).

11.1 Device Operating Modes

The DA7219 codec has three operating modes:

11.1.1 DEEP SLEEP

There is no clocking in DEEP SLEEP mode and consequently no functionality available and no accessory detection is performed. The system will awake when system_active = 1.

11.1.2 SLEEP

In SLEEP mode and with micbias off, AAD performs jack detection and jack configuration detection. Any button press is detected, but identification of the button cannot be performed until micbias is on. No clocking is performed in SLEEP mode, and playback and record are not supported.

11.1.3 ON

AAD performs full-function accessory detection. Playback and record are supported.

All modes, their maximum current consumption, and functionality are listed in Table 23.

Table 23: System States, Configuration, and Current Consumption

Mode	Configuration						CODEC				Typical current consumption		Comments
	V_{DD} + V_{DD_IO}	V_{DD_MIC}	system_active	MCLK	PLL mode	AAD config	Internal ref osc	Internal PLL	Audio path	AAD	V_{DD} + V_{DD_IO}	V_{DD_MIC}	
OFF	OFF	OFF	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	None	None	N/A
DEEP SLEEP	ON	ON	0	N/A	N/A	N/A	OFF	OFF	OFF	OFF	<10 µA	0	Wake on system_active= 1.
SLEEP	ON	ON	1	OFF	OFF	AAD on without button detection	ON	OFF	OFF (playback/ record not supported)	Jack insertion, jack type and pin order	<200 µA	0	
						AAD on with button detection				As above plus button detection (without identification)	<500 µA	0	
						AAD on with button detection and identification				FULL DETECTION (as above but with button Identification)	<300 µA	Dependent on microphone	
ON	ON	ON	1	OFF	SRM - locks to WCLK if DAI is in slave mode	AAD on with button detection and identification	ON	ON	ON (Playback/ record)	FULL DETECTION	Dependent on use case		AAD uses clock on demand to save power
				ON (11.8 MHz or 12.288 MHz)	BYPASS		OFF	OFF					
				ON (Valid Freq 2 MHz to 54 MHz)	Normal - lock to MCLK		OFF	ON					

11.2 Input Paths

11.2.1 Microphone Input

The DA7219 analog input consists of one set of amplifiers and an ADC as shown in Figure 6.

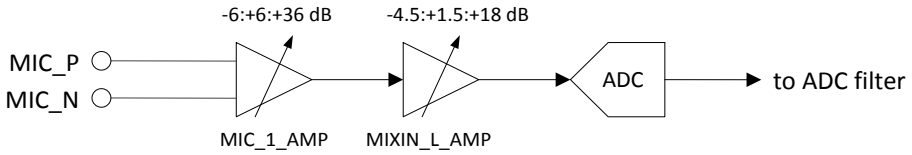

Figure 6: Analog Inputs Block Diagram

11.2.1.1 Microphone Bias

The device has a microphone bias output, which is a programmable voltage source that can be used to supply analog microphones.

The bias output can be independently programmed from 1.8 V to 2.9 V using micbias1_level.

The microphone bias level can only be changed while the associated micbias circuit is disabled (micbias1_en = 0).

Disable micbias prior to setting system_active= 0. Do not turn off the device with micbias disabled.

Table 24: Microphone Bias Settings

micbias1_level	Output Voltage (V) in Low Noise Mode
000	reserved
001	1.8
010	2.0
011	2.2
100	2.4
101	2.6
110	2.8
111	2.9

11.2.1.2 Microphone Amplifier

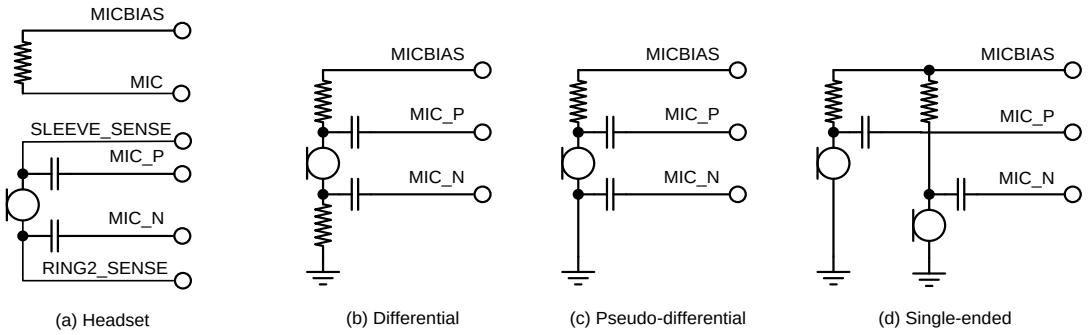

Figure 7: ECM Microphone Configurations

The microphone amplifier can be configured in:

- Headset mode, microphone amplifier is fully differential
- Fully Differential mode for improved common-mode noise rejection
- Pseudo-Differential mode
- Single-Ended mode (MIC_P or MIC_N)

All configurations are illustrated in Figure 7.

The configuration of the first microphone amplifier is specified using the MIC_1_CTRL register. It is enabled by setting the mic_1_amp_en bit, and is muted by setting the mic_1_amp_mute_en bit.

The gain of the amplifier can be set in the range of –6 dB to +36 dB in 6 dB steps using mic_1_amp_gain (see Table 25):

Table 25: First Microphone Amplifier Gain Settings

mic_1_amp_gain	Amplifier Gain (dB)
000	-6
001	0
010	6
011	12
100	18
101	24
110	30
111	36

11.2.1.3 Input Amplifiers

The input amplifier provides an additional gain stage between the microphone amplifier (see section 11.2.1 and Figure 6) and the ADC input. The input amplifier is enabled by setting mixin_l_amp_ramp_en = 1.

The gain can be set in the range of –4.5 dB to +18 dB in 1.5 dB steps using mixin_l_amp_gain.

Gain updates can be synchronized with signal zero-crossings by setting mixin_l_amp_zc_en = 1. If no zero-crossing is detected within the timeout period of approximately 100 ms, the update is applied unconditionally.

As an alternative to zero-cross synchronization, gain updates can be ramped through all intermediate values by setting mixin_l_amp_ramp_en = 1. This ramp setting overrides the settings of mixin_l_amp_zc_en.

The amplifier can be muted using mixin_l_amp_mute_en.

Table 26: Input Mixer Gain Settings

mixin_l_amp_gain	Amplifier gain (dB)
0000	-4.5
0001	-3.0
0010	-1.5
0011	0.0
0100	1.5
0101	3.0
0110	4.5
0111	6.0
1000	7.5
1001	9.0
1010	10.5
1011	12.0
1100	13.5
1101	15.0
1110	16.5
1111	18.0

11.2.2 Analog to Digital Converter

The DA7219 codec contains a high quality audio ADC. The ADC is clocked at a fixed rate of either 3.072 MHz or 2.8224 MHz, depending on the required input sample rate.

The DA7219 includes a low-power 24-bit high quality audio ADC that supports sampling rates from 8 kHz to 96 kHz. The sample rate is specified using the SR register.

The ADC can be enabled and disabled using adc_l_en.

The ADC channels offer a configurable digital gain from -83.25 dB to +12 dB in 0.75 dB steps after the digital conversion. Individual gain settings can be programmed via the adc_l_digital_gain_status control. The currently active gain settings are stored in the ADC_L_GAIN_STATUS register.

Muting, and the ramping of digital gain changes, can be controlled using the dedicated ADC_L_CTRL register. If the ramping is enabled using the control bit adc_l_ramp_en, the rate of the ramping is controlled using gain_ramp_rate in the GAIN_RAMP_CTRL register.

11.3 Digital Engine

DA7219 contains a digital engine that performs the signal processing and also provides overall system control, see Figure 8.

The input signals from the ADCs are passed to the input filter block which includes an HPF for DC offset removal and wind noise suppression, and an automatic level control.

The signals from the input filters are sent to the digital mixer where they can be combined with signals from the tone generator and the DAI, and routed to the output filters and the DAI. The output

filters contain an HPF for DC offset removal, and a fixed 5-band equalizer to adjust the sound of the output signals.

There is also a low latency sidetone path that can take one signal from the ADC and apply gain before passing the signal straight to the output filters. The filter paths are shown in more detail in Figure 9.

A system controller module is included to ensure correct sequencing of the events required to bring up and shut down signal paths without creating pops and clicks.

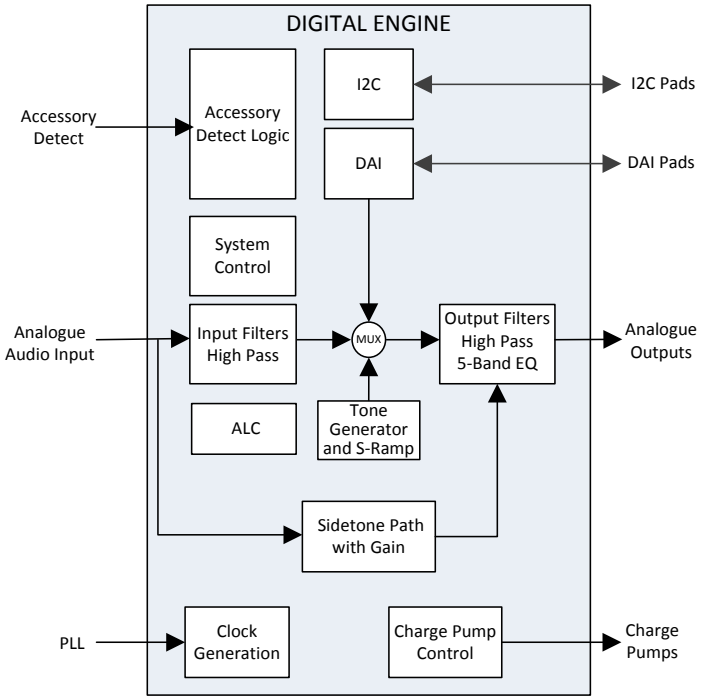

Figure 8: Digital Engine Block Diagram

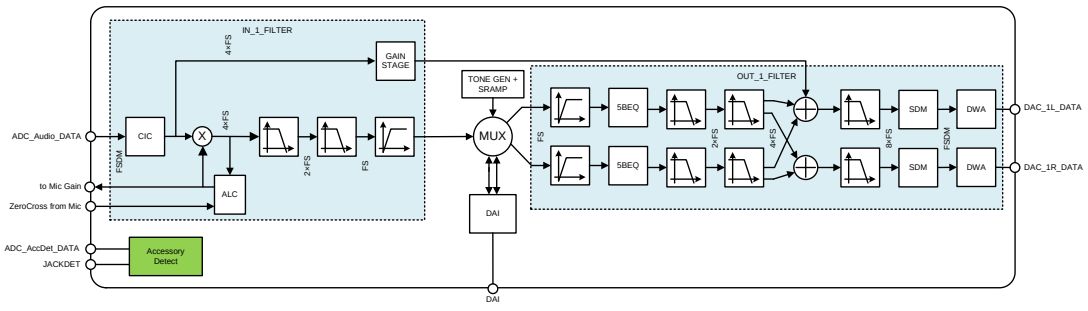

Figure 9: Digital Filters Block Diagram

11.3.1 Input Processing

11.3.1.1 ADC Digital Gain

The ADC channels offer a configurable digital gain from -83.25 dB to +12 dB in 0.75 dB steps after the digital conversion. Individual gain settings can be programmed via the adc_l_digital_gain control. The currently active gain settings are stored in the ADC_L_GAIN_STATUS register.

11.3.1.2 High-Pass Filter

Any DC offset from the input path is removed via configurable IIR high-pass filters (HPFs) with typically < 2 Hz roll-off. After reset the filters for both channels are enabled by default, but can be disabled by clearing adc_hpf_en. The cutoff frequency of the filters can be programmed using adc_audio_hpf_corner.

To improve the quality of microphone recordings, DA7219 provides a programmable HPF engine, enabled via adc_voice_en in the ADC_FILTERS1 register.

In ADC voice mode, adc_voice_en must = 1 and adc_hpf_en must = 1 in which case the HPF corner frequency is set using adc_voice_hpf_corner. The low frequency roll off is configured over a wide range using adc_voice_hpf_corner. This allows for flexible removal of wind and pop noise.

For the first filter, in music mode, adc_voice_en must = 0 and the HPF corner frequency is set using adc_audio_hpf_corner.

The value of the HPF corner frequency also depends on the input sample rate (SR). The sample rates available in the different ADC power modes are summarized in Table 27.

Table 27: Input HPF Settings

adc_voice_en	adc_voice_hpf_corner	adc_voice_en	SR **Sample Rate (kHz)**										
			8	**11.025**	**12**	**16**	**22.05**	**24**	**32**	**44.1**	**48**	**88.2**	**96**
0		00	0.33	0.46	0.5	0.67	0.92	1	1.33	1.84	2	3.68	4
		01	0.67	0.92	1	1.33	1.84	2	2.67	3.68	4	7.35	8
		10	1.33	1.84	2	2.67	3.68	4	5.33	7.35	8	14.7	16
		11	2.67	3.68	4	5.33	7.35	8	10.67	14.7	16	29.4	32
1	000		2.5	3.45	3.75	5	Voice HPF not available for sample rates above 16 kHz.						
	001		25	34.5	37.5	50							
	010		50	68.9	75	100							
	011		100	137.8	150	200							
	100		150	206.7	225	300							
	101		200	275.6	300	400							
	110		300	413.4	450	600							
	111		400	551.3	600	800							

11.3.1.3 Automatic Level Control (ALC)

For improved sound recordings of signals with a large volume range, DA7219 offers a fully-configurable automatic recording level control (ALC) for microphone inputs. This is enabled via the alc_en control. The ALC monitors the digital signal after the ADC and adjusts the microphones' analog and digital gain to maintain a constant recording level, whatever the analog input signal level.

Operation of ALC is illustrated in Figure 10. When the input signal volume is high, the ALC system will reduce the overall gain until the output volume is below the specified maximum value. When the input signal volume is low, the ALC will increase the gain until the output volume increases above the specified minimum value. If the output signal is within the desired signal range (between the specified minimum and maximum levels), the ALC does nothing.

The maximum and the minimum thresholds that trigger a gain change of the ALC are configured via the alc_threshold_min and alc_threshold_max controls.

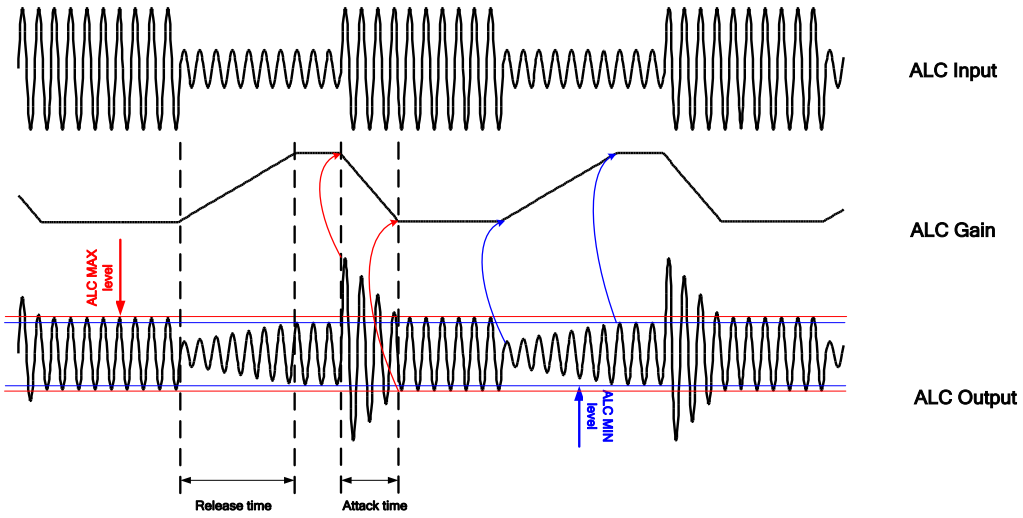

Figure 10: ALC Principle of Operation

The ALC can operate in two modes; Digital-Only mode and Hybrid (combined analog and digital gain) mode.

In Digital-Only mode only the digital gain in the ADC is altered. Although the ALC is controlling the gain, it does not modify adc_l_digital_gain in the ADC_L_GAIN register. This register is ignored while the ALC is in operation. The minimum and maximum levels of digital gain that can be applied by the ALC are controlled using alc_atten_max and alc_gain_max.

The hybrid analog/digital gain mode (Hybrid mode) can be enabled using alc_sync_mode.

In Hybrid mode, the total gain is made up of an analog gain, which is applied to the microphone amplifier, and a digital gain, which is implemented in the filtering stage. The ALC block monitors and controls the gain of the microphone and the ADC.

Hybrid mode offers improved performance and signal tracking over Digital-Only mode. When using the automatic level control (ALC) in Hybrid mode the DC offset between the digital and analog PGAs must be cancelled, see Appendix A.2.

Although the ALC is controlling the gain, it does not modify any of the registers MIXIN_L_GAIN or ADC_L_GAIN, nor does it modify the digital gain register ADC_L_GAIN. These registers are ignored while the ALC is in operation.

Similarly the minimum and maximum levels of analog gain are controlled by alc_ana_gain_min and alc_ana_gain_max. The rates at which the gain is changed are defined by the attack and decay rates in register ALC_CTRL2. When attacking, the gain decreases with alc_attack rate. When decaying, the gain increases with alc_release rate.

The hold-time is defined by alc_hold in the ALC_CTRL3 register. This controls the length of time that the system maintains the current gain level before starting to decay. This prevents unwanted changes in the recording level when there is a short-lived ‘spike’ in input volume, for example when recording speech.

Typically the attack rate should be much faster than the decay rate, as it is necessary to reduce rapidly increasing waveforms as quickly as possible and fast release times will result in the signal appearing to 'pump'. The ALC also has an anti-clipping function that applies a very fast attack rate when the input signal is close to full range. This prevents clipping of the signal by reducing the signal gain at a faster rate than would normally be applied. The anti-clipping function is enabled using alc_antipclip_en, and the threshold above which it is activated is set in the range 0.034 dB/fs to 0.272 dB/fs using alc_anticlip_step.

A recording noise-gate feature is provided to avoid increasing the gain of the channel when there is no signal, or when only a noise signal is present. Boosting a signal on which only noise is present is known as 'noise pumping'. The noise-gate prevents this. Whenever the level of the input signal drops below the noise threshold configured in alc_noise, the channel gain remains constant.

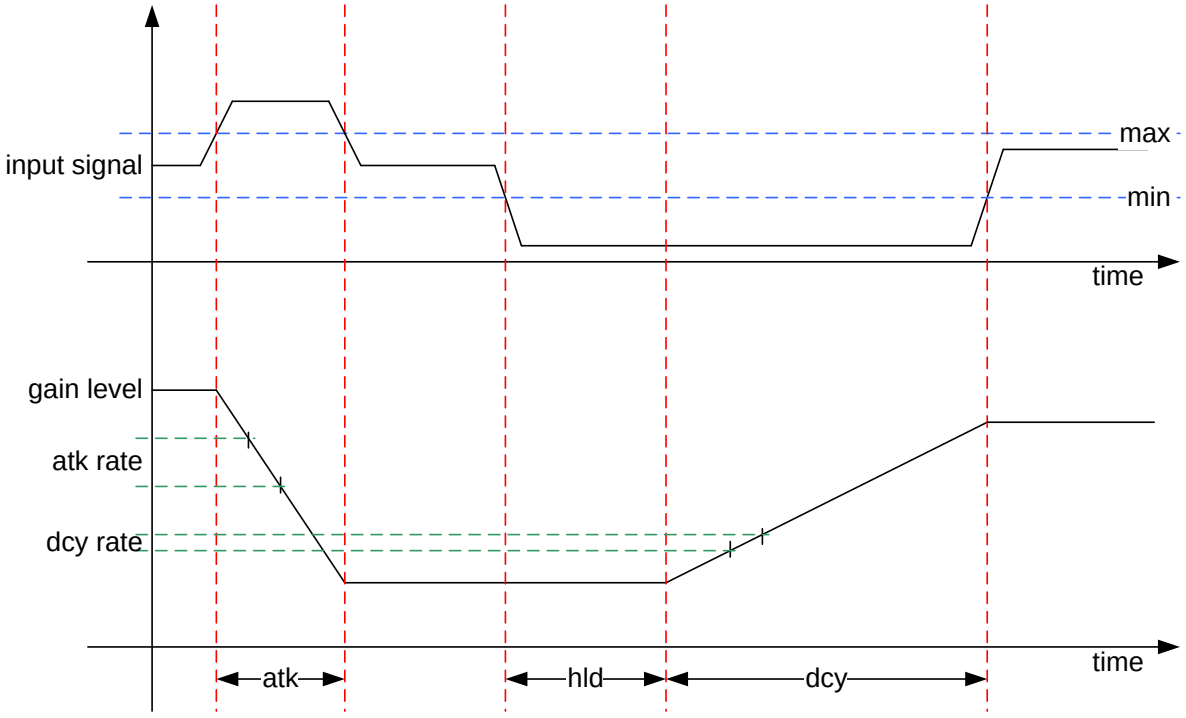

Figure 11: Attack, Delay and Hold Parameters

11.3.2 Sidetone Processing

There is a low latency filter channel between inputs and outputs for implementing a sidetone path. The gain is controlled using sidetone_gain and provides gain in the range -42 dB to +0 dB in +3 dB steps. The sidetone path is enabled using sidetone_en and muted using sidetone_mute_en.

The output from the sidetone channel can be added to left or right (or both) output filters using outfilt_st_1l_src and outfilt_st_1r_src.

11.3.3 Tone Generator

Parameter	Conditions	Min	Typ	Max	Unit
Single-tone frequency	FS = 8,12,16,24,32,48,96 kHz FS = 11.025, 22.05, 44.1, 88.2 kHz	1 1		12000 11025	Hz
Single-tone frequency step			0.2		Hz
Dual-tone modulation frequency A			697 770 852 941		Hz

Parameter	Conditions	Min	Typ	Max	Unit
Dual-tone modulation frequency B			1209 1336 1477 1633		Hz
Output signal level			0		dBFS
On/off pulse duration		10		2000	ms
On/off pulse step size	10 ms to 200 ms duration 200 ms to 2000 ms duration		10 50		ms
On/off pulse repeat	Programmable Continuous		1,2,3,4,5,6∞		Cycles

The tone generator contains two independent sine wave generators, SWG1 and SWG2. Each SWG can generate a sine wave at a frequency (FREQ) from approximately 10 Hz to 12 kHz according to the programmed 16-bit value:

- FREQ[15:0] = 2^16 × fSWG/12000 – 1, for SR2 = 8, 12, 16, 24, 32, 48,96 kHz
- FREQ[15:0] = 2^16 × fSWG/11025 – 1, for SR2 = 11.025, 22.05, 44.1, 88.2 kHz

For SWG1, the FREQ value is stored in two 8-bit registers as freq1_u = FREQ[15:8] and freq1_l = FREQ[7:0]. The SWG2 frequency is programmed in the same way using freq2_u and freq2_l.

The output of the tone generator can come from either of the SWGs, or from a combination of both of them as specified by swg_sel.

In addition the tone generator can produce standard Dual Tone Multi-Frequency (DTMF) tones using the two SWGs if dtmf_en = 1 and the required key pad value is programmed in dtmf_reg as shown in Table 28.

Table 28: DTMF Tones Corresponding to the dtmf_reg Value

SWG2 Freq (Hz)	SWG1 Frequency (Hz)			
	1209	1336	1477	1633
697	0x1	0x2	0x3	0xA
770	0x4	0x5	0x6	0xB
852	0x7	0x8	0x9	0xC
941	0xE	0x0	0xF	0xD

The tone generator can produce 1, 2, 3, 4, 8, 16, or 32 beeps, or a continuous beep, as determined by beep_cycles. Each beep has an on period from 10 ms to 2 s as programmed in beep_on_per and an off period from 10 ms to 2 s as programmed in beep_off_per. The tone generator is started by setting the start_stopn bit, and is halted by clearing this bit. If start_stopn is cleared, the tone generator stops at the completion of the current beep cycle or at the next zero-cross if the number of beeps is set to continuous (beep_cycles = 110 or = 111). The start_stopn bit is automatically cleared once the programmed number of beep cycles has been completed.

11.3.4 Digital Router

DA7219 includes a digital router which is configured by registers DIG_ROUTING_DAI and DIG_ROUTING_DAC.

The router options are illustrated in Figure 12.

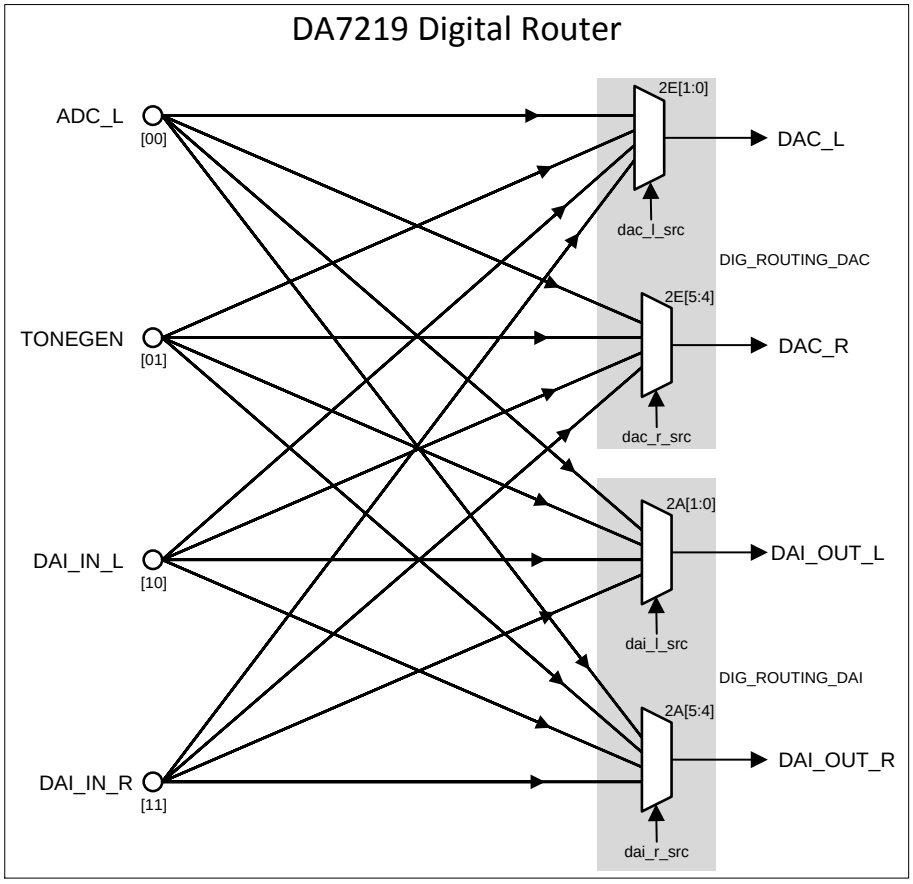

Figure 12: DA7219 Digital Router

DIG_ROUTING_DAC is used to select the inputs to go into the DAC filter chain from the router. DIG_ROUTING_DAI is used to select the inputs to go into the DAI from the router.

For example, for dac_l_src, data selection to the DAC_L path is

- 00 = ADC left output
- 01 = Tone generator
- 10 = DAI input left / DAI mono mix
- 11 = DAI input right / DAI mono mix

The same 2-bit code (00, 01, 10, 11) is used for dac_r_src, dai_l_src and dai_r_src.

11.3.5 System Control

The system control (SC) automates the sequencing of the multiple blocks required to set up one or more particular audio paths. It is an optional feature, and operates by performing register writes with optimal sequencing and timing, thus eliminating pops and clicks.

The SC for the inputs is configured using SYSTEM_MODES_INPUT, and for the outputs by using SYSTEM_MODES_OUTPUT. Writing to the mode_submit field of either of these registers will cause the system controller to process both input and output paths.

11.3.6 Output Processing

11.3.6.1 DAC Digital Gain

Each channel includes individual gain settings that are configurable in 0.75 dB steps ranging from -78 dB (= mute) to 12 dB using dac_l_digital_gain and dac_r_digital_gain. The currently active gain settings are stored in DAC_L_GAIN_STATUS and DAC_R_GAIN_STATUS registers.

11.3.6.2 High-Pass Filter

Any DC offset from the input path is removed via IIR configurable HPFs (typically < 2 Hz roll-off). After reset the filters for both channels are enabled by default, but can be disabled by clearing dac_hpf_en. The cutoff frequency of the filters can be programmed using dac_audio_hpf_corner.

During playback, dedicated voiceband filtering can be enabled using dac_voice_en in the DAC_FILTERS1 register. In DAC voice mode, dac_voice_en must = 1 and dac_hpf_en must = 1 in which case the HPF corner frequency is set using dac_voice_hpf_corner.

The low frequency roll off is configured over a wide range using the dac_voice_hpf_corner control.

In voice mode, the wind noise HPF cutoff frequency is determined by the settings of the adc_voice_hpf_corner and the dac_voice_hpf_corner register bits, These cutoff frequencies are not fixed and vary with the sample rate being used. Table 29 shows the cutoff frequencies for all valid settings of adc_voice_hpf_corner and dac_voice_hpf_corner, at all sample rates of 16 kHz and below.

Table 29: Output HPF Settings

dac_voice_en	dac_voice_hpf_corner	dac_audio_hpf_corner	SR Sample Rate (kHz)										
			8	**11.025**	**12**	**16**	**22.05**	**24**	**32**	**44.1**	**48**	**88.2**	**96**
0		00	0.33	0.46	0.5	0.67	0.92	1	1.33	1.84	2	3.68	4
		01	0.67	0.92	1	1.33	1.84	2	2.67	3.68	4	7.35	8
		10	1.33	1.84	2	2.67	3.68	4	5.33	7.35	8	14.7	16
		11	2.67	3.68	4	5.33	7.35	8	10.67	14.7	16	29.4	32
1	000		2.5	3.45	3.75	5	Voice HPF not available for sample rates above 16 kHz.						
	001		25	34.5	37.5	50							
	010		50	68.9	75	100							
	011		100	137.8	150	200							
	100		150	206.7	225	300							
	101		200	275.6	300	400							
	110		300	413.4	450	600							
	111		400	551.3	600	800							

11.3.6.3 5-Band Equalizer

The gains of each band can be individually configured, from -10.5 dB to 12.0 dB in 1.5 dB steps, using the dac_eq_band1, dac_eq_band2, dac_eq_band3, dac_eq_band4, dac_eq_band5 controls.

The output filters provide gain or attenuation in each of five separate (fixed) frequency bands using the 5-band equalizer. The equalizer, for both left and right channels, is enabled using dac_eq_en.

When the equalizer is enabled, the digital gain is reduced by 12 dB to avoid clipping. If desired the gain can be added back in after the equalizer block via the DAC_L_GAIN and DAC_R_GAIN registers.

The center or cutoff frequency of each of the five bands depends on the output sample rate as shown in Table 30. The equalizer cannot be used with sample rates greater than 48 kHz

Table 30: Output 5-Band Equalizer Center/Cutoff Frequencies

FS (kHz)	Center Frequency (Hz) at Programmed Setting				
	Band 1	Band 2	Band 3	Band 4	Band 5
8	0	99	493	1528	4000
11.025	0	136	680	2106	5512
12	0	148	740	2293	6000
16	0	96	440	2128	8000
22.05	0	133	607	2933	11025
24	0	145	660	3191	12000
32	0	95	418	1797	16000
44.1	0	131	576	2386	22050
48	0	143	627	2596	24000

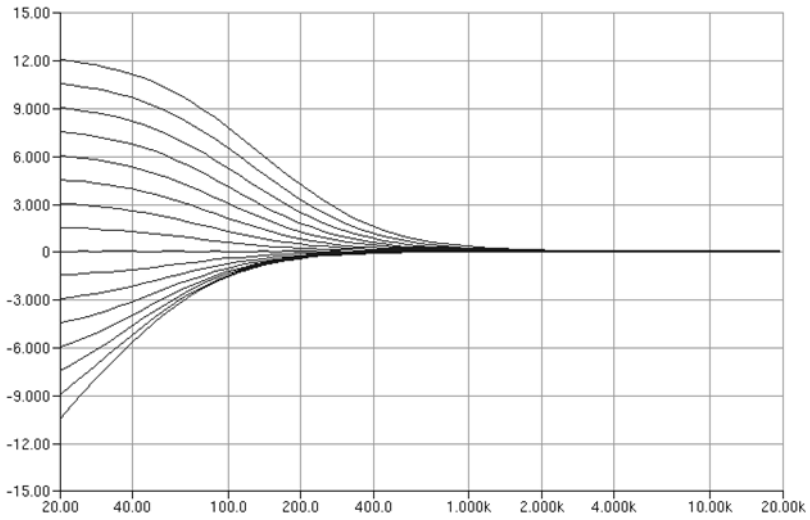

Figure 13: Equalizer Filter Band 1 Frequency Response at FS = 48 kHz

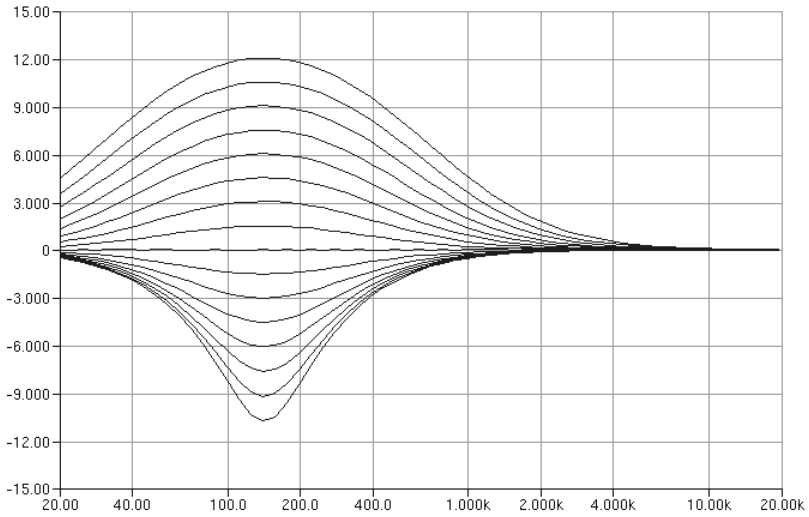

Figure 14: Equalizer Filter Band 2 Frequency Response at FS = 48 kHz

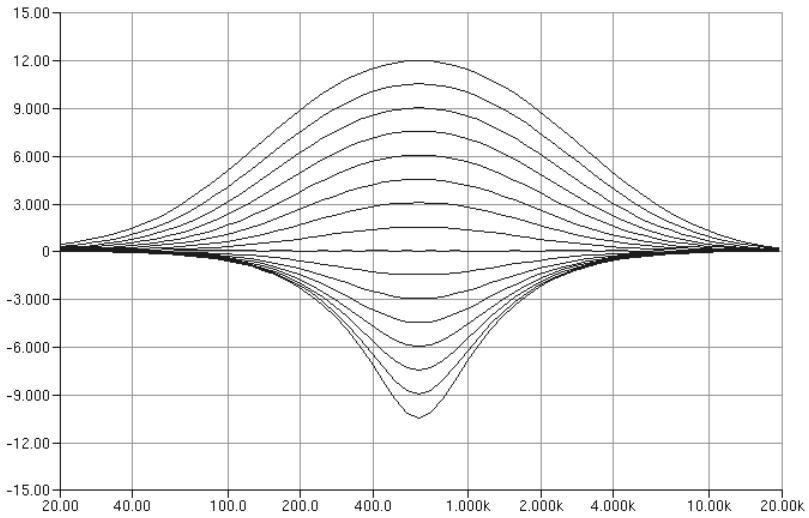

Figure 15: Equalizer Filter Band 3 Frequency Response at FS = 48 kHz

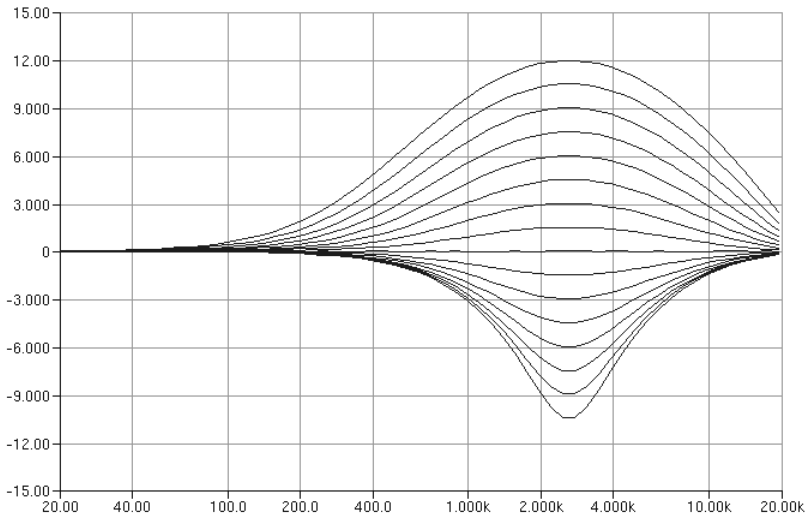

Figure 16: Equalizer Filter Band 4 Frequency Response at FS = 48 kHz

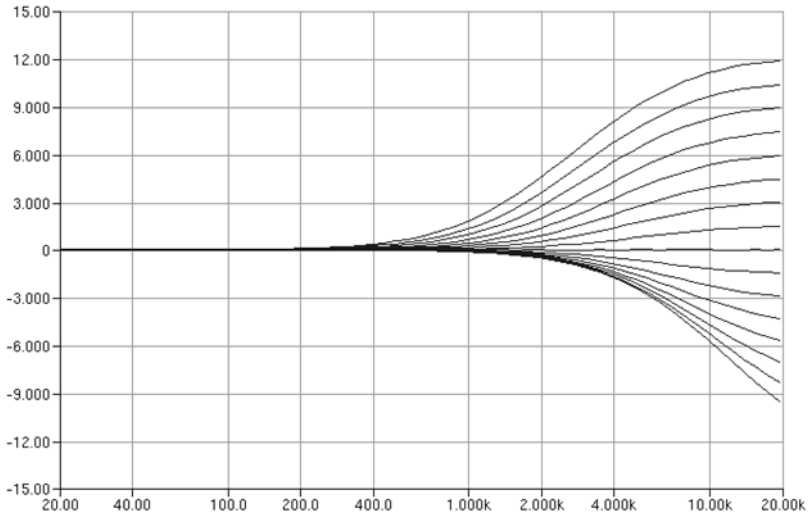

Figure 17: Equalizer Filter Band 5 Frequency Response at FS = 48 kHz

11.3.6.4 DAC Soft Mute

To improve the user's perception of audio reconfigurations, the DAC channel signals may be soft muted by asserting dac_softmute_en (in register DAC_FILTERS5).The soft mute function attenuates the digital input to the DAC, ramping the gain down in steps of 0.1875 dB from its current level to -77.25 dB, then completely muting the channel. When dac_softmute_en is released, the attenuation is set to -77.25 dB, and then ramped up to the previous gain level. Both left and right channels of soft mute enabled output amplifiers are muted simultaneously. The ramping up and down rate is dependent on the audio sample rate and can be individually configured via dac_softmute_en.

Setting dac_softmute_en= 1 enables a soft mute on both channels.

During active soft muting, the digital gain of the DAC will be different to the value programmed inside controls dac_l_digital_gain_status and dac_r_digital_gain_status.

11.4 Output Paths

11.4.1 Digital to Analog Converter

The DA7219 codec includes a stereo audio DAC. Left and right channels of the DAC are independently and automatically enabled whenever the corresponding output filter channel is enabled.

The DAC is clocked at 3.072 MHz or 2.8224 MHz depending on the output sample rate (SR). Left and right channels of the DAC are independently and automatically enabled whenever the corresponding output filter channel is enabled.

The integrated stereo DAC is suitable for high quality audio playback by MP3 players and by portable multimedia players of all kinds.

The left and right channels of the DAC can be individually enabled using controls dac_l_en and dac_r_en.

Each channel includes individual gain settings that are configurable in 0.75 dB steps from -78 dB to 12 dB using dac_l_digital_gain and dac_r_digital_gain. The currently active gain settings are stored in DAC_L_GAIN_STATUS and DAC_R_GAIN_STATUS registers.

On the dedicated DAC_L_CTRL and DAC_R_CTRL registers, settings such as mute and ramping of gain changes can be configured. If ramping is enabled using the control bits dac_l_ramp_en or dac_r_ramp_en, the rate of the ramping can be controlled using gain_ramp_rate in the GAIN_RAMP_CTRL register.

A digital HPF for each DAC channel is implemented with a 3 dB cutoff frequency controlled in the DAC_FILTERS1 register by dac_audio_hpf_corner. The HPFs are enabled by control dac_hpf_en. After reset, the HPFs for both channels are enabled by default.

11.4.2 Headphone Outputs

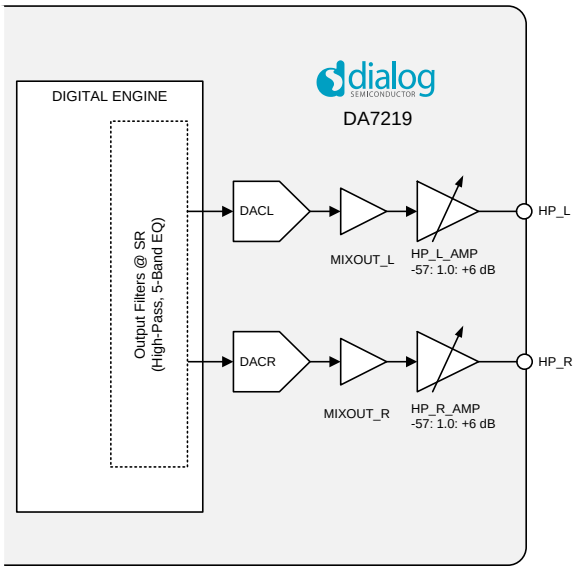

Figure 18: Headphone Output Paths Showing the Two Amplifiers

11.4.2.1 Mixout Amplifier

Each headphone (HP) path has one mixout amplifier which must be enabled when using the headphone outputs. MIXOUT_L, is enabled by setting mixout_l_amp_en = 1 and MIXOUT_L_SELECT = 1, MIXOUT_R is enabled by setting mixout_r_amp_en = 1 and MIXOUT_R_SELECT = 1.

11.4.2.2 Headphone Amplifiers

Each headphone (HP) path has one HP amplifier stage providing a gain of –57 dB to +6 dB in 1.0 dB steps.

The amplifiers are configured to operate in single-ended mode. The HP loads are connected between HP_L and HP_R, and the internal ground set by the MIC/GND switches during the detect sequence.

The HP amplifiers are configured to operate in true-ground (charge pump) mode. In true-ground supply mode, the charge pump must be enabled to generate the ground-centered supply rails for the amplifiers.

The left-channel HP amplifier (HP_L_CTRL) is enabled by setting hp_l_amp_en = 1. The output stage is enabled independently by setting hp_l_amp_oe = 1. The amplifier gain can be set in the range of –57 dB to +6 dB in 1.0 dB steps using hp_l_amp_gain.

Gain updates can be ramped through all intermediate values by setting hp_l_amp_zc_en = 1. This ramp setting overrides the settings of hp_l_amp_zc_en. To prevent zipper noise when gain ramping is selected, the gain is ramped through additional sub-range gain steps.

As an alternative to gain ramping, gain updates can be synchronized with signal zero-crossings by setting hp_l_amp_zc_en = 1. If no zero-crossing is detected within the timeout period, then the gain update is applied unconditionally. The timeout period is approximately 0.1 s, and is not configurable.

The amplifier can be muted by setting hp_l_amp_mute_en = 1.

The amplifier can be put in its minimum gain configuration by setting hp_l_amp_min_gain_en = 1. If either zero-crossing or ramping are enabled when minimum gain is set, the ramping or the zero crossing or both will be performed while activating the minimum gain.

The right-channel HP amplifier (HP_R_CTRL) is controlled in the same manner.

11.4.3 Charge Pump Control

The charge pump is enabled by asserting cp_en in the CP_CTRL register. Once enabled, the charge pump can be controlled manually or automatically. When under manual control (cp_mchange = 00), the output voltage level is reserved.

The amount of charge stored, and therefore the voltage generated, by the charge pump is controlled by the charge pump controller. As the power consumed by devices such as amplifiers is proportional to V^2, significant power savings are available by matching the charge pump's output with the system's power requirement.

There are three modes of operation that are determined by the cp_mchange setting, as described in Table 31.

Table 31: Charge Pump Output Voltage Control

Charge Pump Tracking Mode cp_mchange	Charge Pump Output Voltage	Details
00	Reserved	Reserved
01	Voltage level depends on the programmed gain setting	The charge pump controller monitors the amplifier volume settings, and generates the minimum voltage that is high enough to drive a full-scale signal at the current gain level.
10	Voltage level depends on the DAC signal envelope (DAC Volume Mode)	The charge pump controller monitors the DAC signal, and generates a voltage that is high enough to drive a full-scale output at the current DAC signal volume level
11	Voltage level depends on the signal magnitude and the programmed gain setting (Signal Size Mode)	The charge pump monitors both the programmed volume settings and the actual signal size, and generates the appropriate output voltage. This is the most power-efficient mode of operation.

When cp_mchange = 10 (tracking DAC signal size) or cp_mchange = 11 (tracking the output signal size), the charge pump switches its supply between the ±VDD rails and the ±VDD/2 rails depending on its power requirements.

When low output voltages are needed, the charge pump saves power by using the lower voltage ±VDD/2 rails.

The switching point between using the ±VDD rails and the ±VDD/2 rails is determined by the cp_thresh_vdd2 register setting. The switching points determined by cp_thresh_vdd2 vary between the two cp_mchange modes, and are summarized in Table 32 and Full Scale (FS) = 1.6 * VDD

Table 33.

When the charge pump output voltage is controlled manually (cp_mchange = 00) or when it is tracking the PGA gain settings (cp_mchange = 01), the charge pump always takes its supply from V_{DD_CP}.

Table 32: cp_thresh_vdd2 Settings in DAC Volume Mode (cp_mchange = 10)

cp_thresh_vdd2 Setting	Approximate Switching Point (Note 1)	cp_thresh_vdd2 Setting
0x01	-30 dBFS	Do not use. Very power-inefficient as nearly always ±VDD
0x03	-24 dBFS	Not recommended. Very power-inefficient as nearly always ±VDD

cp_thresh_vdd2 Setting	Approximate Switching Point (Note 1)	cp_thresh_vdd2 Setting
0x07	-18 dBFS	Good to use but not power efficient
0x0E	-12 dBFS	Good to use
0x10	-10 dBFS	Recommended setting
0x3F – 0x13		Not recommended

Note 1 Full Scale (FS) = 1.6 * VDD

Table 33: cp_thresh_vdd2 Settings in Signal Size Mode (cp_mchange = 11)

cp_thresh_vdd2 Setting	Approximate Switching Point (Note 1)	Notes
0x00	Never	Not recommended. Always ±VDD mode
0x01	Never	Not recommended. Always ±VDD mode
0x02	-32 dBFS	Not recommended. Very power-inefficient as nearly always ±VDD
0x03	-24 dBFS	Good to use
0x04	-20 dBFS	Good to use
0x05	-17 dBFS	Good to use
0x06	-15 dBFS	Recommended setting
0x07	-13 dBFS	Good to use
0x08	-12 dBFS	Good to use
0x09	-11 dBFS	Good to use
0x0A	-10 dBFS	Good to use
0x0B	-9 dBFS	Not recommended. ±VDD/2 begins to clip
0x0C	Never	Not recommended. Always ±VDD/2 mode
0x0D	Never	Not recommended. Always ±VDD/2 mode
0x0E	Never	Not recommended. Always ±VDD/2 mode
0x0F	Never	Not recommended. Always ±VDD/2 mode

Note 1 Full Scale (FS) = 1.6 * V_{DD}

11.4.4 Tracking the Demands on the Charge Pump Output

There are three points at which the demands on the charge pump can be tracked. These tracking points are determined by cp_mchange.

11.4.4.1 cp_mchange = 01 (Tracking the PGA Gain Setting)

If cp_mchange = 01, it is the PGA gain setting that is tracked, and which provides the feedback to boost the clock frequency when necessary.

11.4.4.2 cp_mchange = 10 (Tracking the DAC Signal Setting)

If cp_mchange = 10, it is the size of the DAC signal that is tracked, and which provides the feedback to boost the clock frequency when necessary.

11.4.4.3 cp_mchange = 11 (Tracking the Output Signal Magnitude)

If cp_mchange = 11, it is the magnitude of the output signal that is tracked, and which provides the feedback to boost the clock frequency when necessary.

11.5 Advanced Accessory Detection

If the DA7219 is configured for advanced accessory detection (AAD), the insertion of a jack wakes the system up. No external clocking is required to detect a jack insertion, and the clock is only requested if the input is changing and if debouncing is required. This ensures the lowest possible power consumption with no digital leakage.

Once a jack has been inserted, the AAD differentiates between a 3-pole jack (used on headphones and lineouts) and a 4-pole jack (used on headsets). Two-pole jacks are detected as a 3-pole jack, and will work as designed as a mono output.

There are two combinations of 4-pole jack available in the market, both of which are supported by the AAD. The jack configurations are shown in Figure 19.

	Jack Type	
Position	**CTIA**	**OMTP**
SLEEVE	MIC	GND
RING2	GND	MIC
RING1	HP_R	HP_R
TIP	HP_L	HP_L

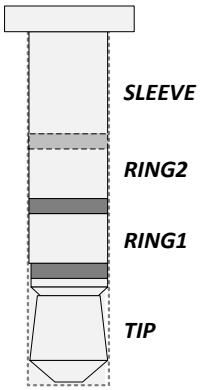

Figure 19: Jack Socket Variants

On detecting the insertion of a jack, the DA7219 moves to the microphone-detect state where it drives current down the SLEEVE pin and measures the impedance to the RING2 pin, which will be connected to GND_HP by the internal GND switch.

NOTE
In order to detect a jack insertion the headphone amplifiers must be disabled

If the impedance measured between the SLEEVE and RING2 pins is below 500 Ω (default, threshold configurable via mic_det_thresh), the DA7219 detects the connected accessory as a 3-pole jack. The DA7219 then returns to the jack detection state to poll for removal, but continues to periodically pulse current down the SLEEVE pin to verify that the connected accessory is 3-pole. This continued polling avoids an incorrect detection, for example, if a 4-pole accessory is inserted with a button depressed.

NOTE
A two-pole jack is detected as a 3-pole jack and will work as a mono output.

If the impedance measured between the SLEEVE and RING2 pins is below the value set in mic_det_thresh, the DA7219 detects the connected accessory as a 4-pole jack. The DA7219 then moves to the pin order-detect state, where it first drives current down the SLEEVE and then the RING2 pins, and compares the voltages measured in each case. The pin that develops the largest voltage will be deemed to be the accessory's microphone, and the other pin as the ground.

The headphone impedance can also be used to determine whether the output is to a headphone or to a line output. Impedance measurements below a pre-set threshold are deemed to be headphones, and impedances above the threshold are line outputs.

The DA7219 will then move to the button detect state, where polling is carried out to detect button presses. If a button is pressed while MICBIAS is off, the DA7219 can only detect that a button has been pressed, but cannot distinguish between the buttons.

To distinguish which one of up to four buttons was pressed, the MICBIAS rail must be enabled so that the impedance can be measured between the MIC and GND pins. See section 11.5.6 for further details.

While any of the four possible buttons is being pressed, any further button presses are ignored. Only once the first button has been released can a second or subsequent button press be detected.

Detection of the jack type and its configuration, detection of the number of buttons, detection of a mic input, and detection of headphone or line outputs are all performed automatically when the AAD block is enabled.

On detecting a button press, the DA7219 can identify all buttons as defined in the Android Wired Headset Specification (v1.1) when MICBIAS is present.

The DA7219 also offers the possibility of overriding the automatically detected accessories, and of setting them manually.

A full cross-reference of the DA7219's functionality and power consumption in different modes is listed in Table 23.

11.5.1 Configuring Advanced Accessory Detection

AAD is enabled by setting accdet_en = 1.

Within the AAD block, all individual accessory detection measurements can be enabled or disabled, and all accessory detect interrupt signals can be masked.

All accessory detection measurements can be manually overridden, and the current statuses of all measurements can be interrogated from the status register fields.

Jack type detection, jack configuration detection, and button detection are all based on measurements of resistance between different pins. The resistance thresholds for every measurement type are all configurable by using the relevant register fields.

A signal timing diagram is illustrated in Figure 20. These features are summarized in Table 34, and Table 35 are described in greater detail in the following sections.

Table 34: DA7219 Advanced Accessory Detection Feature Summary

Feature	DA7219 support	Configuration	Host Reporting
Jack Insertion/Removal Detection	Yes	Enabled when system_active and accdet_en are both 1. Jack insertion latency set by jackdet_debounce (1 ms <--> 1 s).	Host notifiaction via e_jack_inserted and e_jack_removed IRQ events.
Jack Type Detection	Yes - 3-pole / 4-pole	Jack type detection runs on insertion, duration set by jack_detect_rate. Host configurable microphone detection impendance threshold mic_det_thresh (100, 200, 500, 750 Ω). Optional host manual type override provided.	Host notification via e_jack_detect_complete IRQ event. jack_type_sts register available for host readback (3-pole or 4-pole reported), data is qualified by e_jack_detect_complete
Pin Order Detection	Yes - CTIA/OMTP	Detection with GND switching runs on insertion if a 4-pole jack is detected. Optional host manual pin order override provided.	Host notification via e_jack_detect_complete IRQ event. register available for host readback (LRGM or LRMG reported), data is qualified by e_jack_detect_complete.
Button Press Detection	Yes - press / release detection for A,B,C and D button impedances with +/- 1 % accuracy, as per Google Chromebook Headset Accessory Electrical Specification.	Button detection enable and frequency (2 ms<--> 500 ms) set by button_config. Host controlled A_D_BUTTON_THRESH, D_B_BUTTON_THRESH, B_C_BUTTON_THRESH, and C_MIC_BUTTON_THRESH set the ADC voltage thresholds for button press impedance measurements = (R_{LOAD} / (R_{LOAD} + $R_{MICBIAS}$))	Host notification via e_button_*_pressed and e_button_*_released IRQ events, (where * = a/b/c/d). button_type_sts 8-bit ADC measurement result also available for host readback.
Interrupt Reporting	Yes - single dedicated h/w interrupt line.	All events are maskable and are 'Write 1 to clear'.	Interrupt line asserted to host when any unmasked events are captured. Interrupt line is de-asserted when all unmasked events have been cleared by host.
MICBIAS Isolation	Yes - both on insertion and removal.	Host control when the MICBIAS rail can be enabled (requires V_{DD_MIC}) with micbias1_en. AAD will automatically enable the MICBIAS LDO following e_jack_detect_complete if jack_type_sts reports 4-pole. MICBIAS is auto-disabled, discharged and isolated on e_jack_removed to prevent audible artefacts on HPs during a fast jack removal.	micbias_up_sts available for host readback to report MICBIAS rail is up.
HP_L Impedance Measurement	Yes - supported by DA7219 using s/w controlled sequence following insertion.	N/A	N/A
HP_L / HP_R to GND when Device Unpowered	Yes - supported by DA7219 using pulldown on HPs.	N/A	N/A

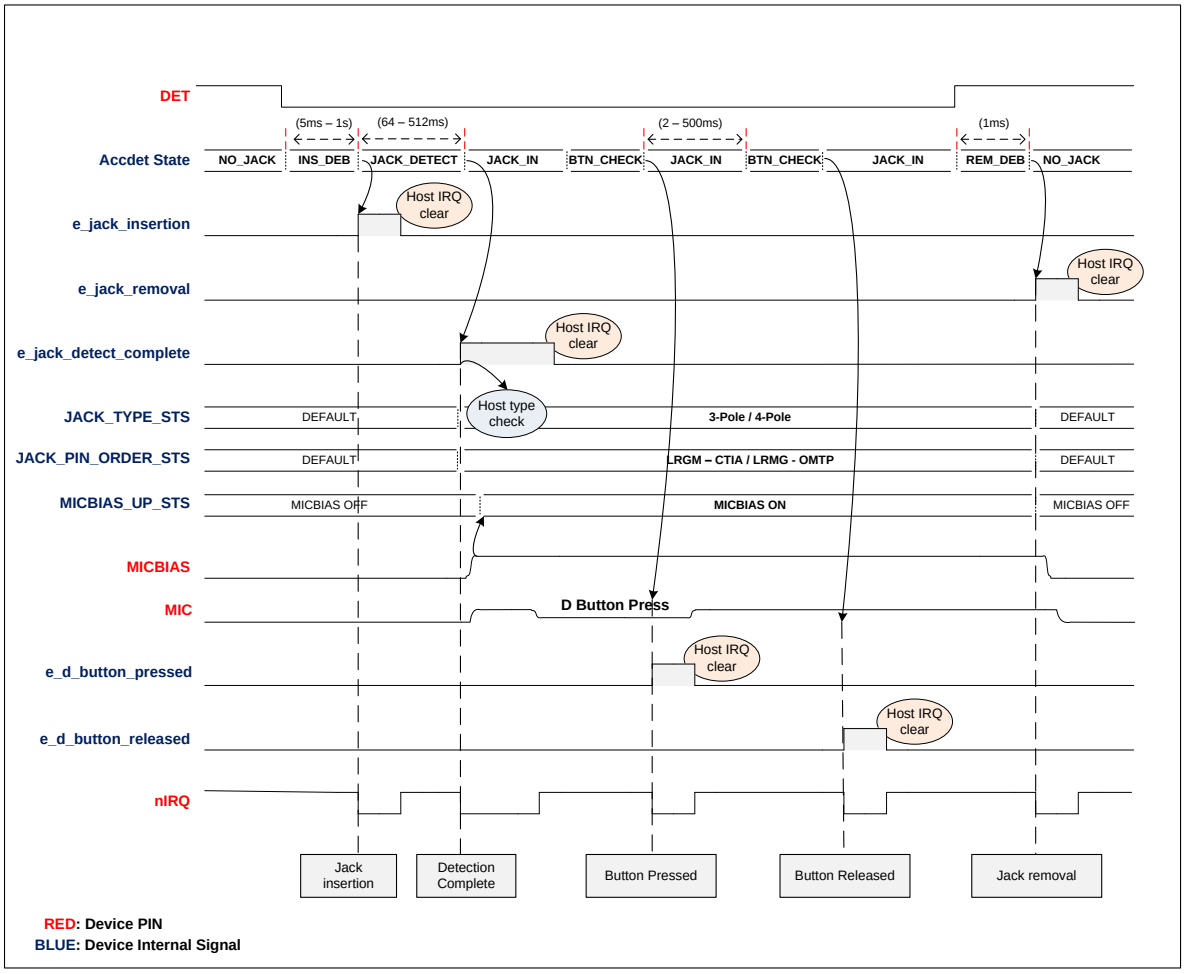

Figure 20: Signal Timing Diagram for the AAD Function

NOTE
V_{DD_MIC} must always be greater than V_{DD}

11.5.2 Detection of Jack Insertion or Removal

Whenever a jack is inserted, a jack insertion event is flagged by e_jack_inserted = 1. Similarly, a jack removal event is flagged by e_jack_removed = 1. The presence or absence of a jack is recorded in jack_insertion_sts.

Any jack insertion will be detected, and is recorded by the setting of jack_insertion_sts. The register field jack_insertion_sts = 1 if a jack has been inserted, and jack_insertion_sts = 0 if no jack has been inserted.

Jack detection latency, that is, the time from an e_jack_inserted event to the point where e_jack_detect_complete is asserted, is configurable using jack_detect_rate. The jack detection latency times are different for 3-pole and 4-pole jacks, and are listed in Table 35.

The JACKDET pin is designed to be pulled either HIGH or LOW on the insertion of the jack. If using an HPLDET type headset socket additional external circuitry is required.

Table 35: Jack Detection Latency Timings Controlled by jack_detect_rate.

jack_detect_rate value	3-pole jacks (ms)	4-pole jacks (ms)
00	32	64
01	64	128
10	128	256
11	256	512

Debouncing is available on jack insertion and removal events. Debounce on jack insertion is specified using jackdet_debounce, and on jack removal using jackdet_rem_deb. The debounce times are listed in Table 36 and Table 37.

Table 36: Debounce Settings for Jack Insertion Events

jackdet_debounce	Debounce Time (ms)
000	5
001	10
010	20 (default)
011	50
100	100
101	200
110	500
111	1

Table 37: Debounce Settings for Jack Removal Events

jackdet_rem_deb	Debounce Time (ms)
00	1 (default)
01	5
10	10
11	20

The jack insertion, jack removal, and jack complete interrupts can be masked using the register fields in the ACCDET_IRQ_MASK_A register. The jack insertion interrupt is masked by setting m_jack_inserted = 1, the jack removal interrupt is masked by setting m_jack_removed = 1, and the jack detection complete interrupt is masked by setting m_jack_detect_complete = 1. These masking fields mask the interrupt signals, but do not prevent updating of the event fields or the status fields previously described.

11.5.3 Three-Pole or Four-Pole Jack Insertion

The type of jack inserted can be determined automatically by setting jack_type_det_en = 1.

Once the jack insertion measurement has been completed, e_jack_detect_complete = 1, the AAD determines whether a 3-pole or a 4-pole jack has been inserted. This is done by measuring the resistance between the SLEEVE and the RING2 pins.

- If the measured impedance is below the threshold setting, a 3-pole jack is deemed to have been inserted.
- If the resistance is above this threshold setting, a 4-pole jack is deemed to have been inserted.

If a mono 2-pole jack is inserted, the AAD will detect this as a 3-pole jack, but the 2-pole jack will work as designed, that is, as a mono output.

The threshold setting used to determine whether a 3-pole or a 4-pole jack has been inserted is set using mic_det_thresh. The settings are listed in Table 38.

Table 38: Resistance Threshold Settings for Three-Pole and Four-Pole Jack Determination

mic_det_thresh	Resistance Threshold (Ω)
00	200
01	500 (default)
10	750
11	1000

Once the jack type has been successfully determined, the type of jack is recorded in jack_type_sts. A 3-pole jack is indicated by jack_type_sts = 0, and a 4-pole jack by jack_type_sts = 1.

The jack type status recorded in the register field jack_type_sts is not valid until the measurement has been completed. Measurement completion is indicated when e_jack_detect_complete = 1.

The assertion of e_jack_detect_complete indicates the completion of both the jack_type_sts measurement and the jack_pin_order_sts measurement.

The measurement of the type of jack, which is performed automatically when jack_type_det_en = 1, can be overridden if required. To do this, set jack_type_det_en = 0 to prevent the measurement taking place, and then use the jack_type_force register field to force the jack type. A 3-pole jack is specified by setting jack_type_force = 0, and a 4-pole jack by setting jack_type_force = 1.

11.5.4 Jack Pin Order Detection with Four-Pole Jacks

Two different polarities are widely used with 4-pole jacks. These are the CTIA tip-ring-ring-sleeve configuration of LEFT-RIGHT-GND-MIC, and the OMTP configuration of LEFT-RIGHT-MIC-GND.

If pin_order_det_en = 1, the detection of jack configuration is performed automatically. The measurement of jack configuration can be overridden by setting pin_order_det_en = 0, and using pin_order_force = 0 to specify the CTIA configurations. Setting pin_order_force = 1 specifies the OMTP configuration.

The jack configuration status recorded in the register field jack_pin_order_sts is not valid until the measurement has been completed. Measurement completion is indicated when e_jack_detect_complete = 1.

The assertion of e_jack_detect_complete indicates the completion of both jack_type_sts and jack_pin_order_sts measurements.

11.5.5 Headphone Output and Line Output

The DA7219 can detect whether the output is a headphone (HP) or a line output.This is enabled by setting hptest_en = 1.

The impedance is measured between HP_L (or HP_R) and the local GND connection on either SLEEVE or RING2 (depending on the jack configuration) to determine whether the output is to an HP or to a lineout. Impedance measurements below a pre-set threshold are deemed to be HP, and impedances above the threshold are line outputs.

The threshold value is set between 1 kΩ and 10 kΩ by setting hptest_res_sel appropriately. The threshold settings available are listed in Table 39.

The Tone Generator is used to develop a slow S-ramp of the signal amplitude at a frequency below the audible range on the HP outputs. The S-ramp profile is configurable for maximum flexibility.

The device monitors the current drawn by the HP amps during this process, and reports back the load as either above or below the threshold level. The accuracy of the measurement is ±40 %.

The host AP must control the test by:

1. Programming the S-ramp profile

2. Initializing the DA7219 signal path and outputs
3. Initiating the S-ramp function
4. Reading back the impedance detection status register for the load condition

Table 39: Resistance Threshold Settings for Headphone and Lineout Determination

hptest_res_sel Setting	Test Threshold Impedance (kΩ)
00	1.0
01	2.5
10	5.0
11	10.0

The result of the headphone threshold test is stored in hptest_comp.

11.5.6 Detection of Buttons

After successful detection of the insertion of a 4-pole jack (e_jack_detect_complete = 1 and jack_type_sts = 1), the DA7219 will move to the button detect state, where polling is carried out for button presses. If a button is pressed while MICBIAS is off, the DA7219 can only detect that a button has been pressed, and cannot distinguish between the buttons. On detecting a button press, the DA7219 can identify all buttons as defined in the Android Wired Audio Headset Specification (v1.1) when MICBIAS is present.

The Android Wired Audio Headset Specification (v1.1) specifies the impedance associated with any button press. The impedance is measured between the MIC and GND.

While any of the four possible buttons is being pressed, any further button presses are ignored. Only after the first button has been released can a second or subsequent button press be detected.

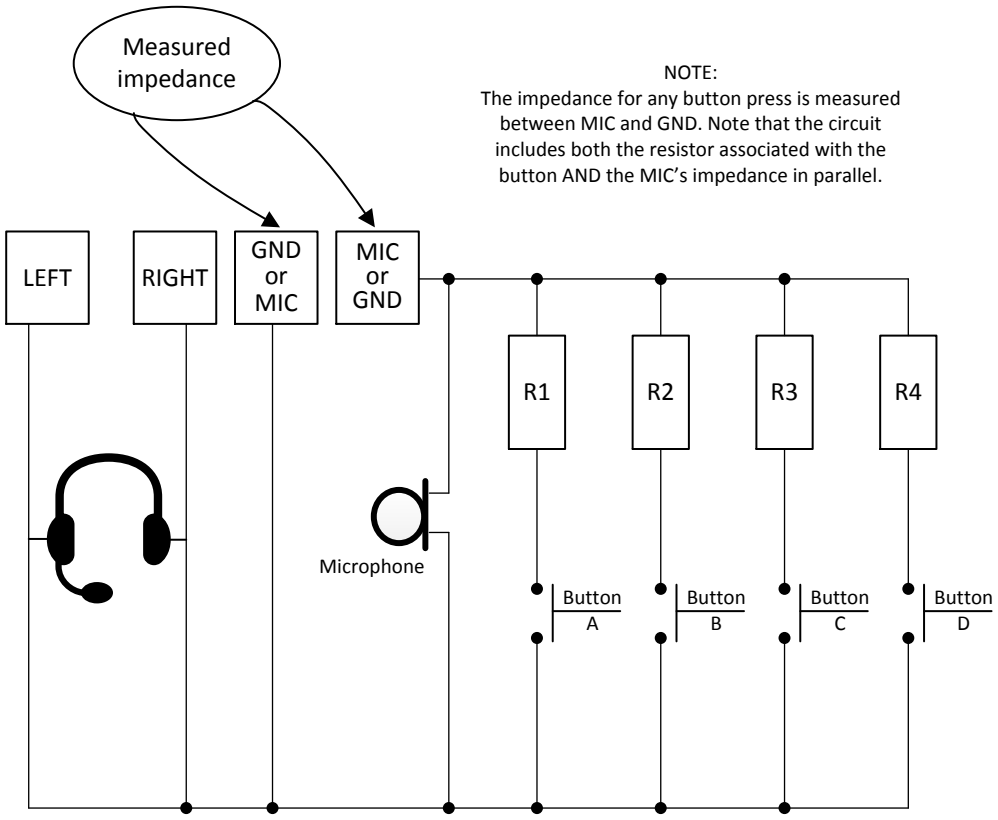

Figure 21: Measuring the Impedance of a Button Press

The Android Wired Audio Headset Specification (v1.1) stipulates the functions and names of the four possible buttons on a headset. These are listed in Table 40.

Table 40: Button Names and Functions in Android Devices

Button	Function
Function A	Play, pause, or hook (short press) Trigger assist (long press) Next (double-press)
Function B	Volume +
Function C	Volume -
Function D	Google voice search feature

Headsets with only one button must implement Function A.

Headsets with multiple buttons must implement functions according to the following patterns:

- Two functions: Functions A and D
- Three functions: Functions A, B, and C
- Four functions: Functions A, B, C, and D

Whenever a button is pressed, a button press event is flagged by e_button_<a|b|c|d>_pressed = 1.

Similarly, a button release event is flagged by e_button_<a|b|c|d>_released = 1.

The measured impedance of the last button press is recorded in button_type_sts. The impedance measurements can be averaged using button_average. Averaging in this manner provides greater immunity to spurious measurements caused by noise, but at a cost of consuming more power and of increasing the measurement latency (every extra measurement used in the averaging takes approximately 1 ms to perform). The number of measurements that are used in the averaging are listed in Table 41.

Table 41: Setting the Number of Measurements Used in Averaging

button_average Setting	Number of Measurements Used in Averaging
00	1
01	2
10	4
11	8

The button press interrupts can be masked by asserting the register fields m_button_<a|b|c|d>_pressed. The button released interrupts can be masked by setting m_button_<a|b|c|d>_released = 1. These masking fields mask the interrupt signals, but do not prevent updating of the event fields or the status fields previously described.

The impedance threshold between Button A and Button D is specified via A_D_BUTTON_THRESH, and is specified as (R_{LOAD} / R_{LOAD} + $R_{MICBIAS}$).

Similarly, the impedance threshold between Button D and Button B is specified using D_B_BUTTON_THRESH, and is specified in the same manner (R_{LOAD} / R_{LOAD} + $R_{MICBIAS}$). The impedance threshold between Button B and Button C is specified using B_C_BUTTON_THRESH, and is specified in the same manner (R_{LOAD} / R_{LOAD} + $R_{MICBIAS}$).

The impedance threshold between Button C and MIC is specified using C_MIC_BUTTON_THRESH and is again specified in the same manner (R_{LOAD} / R_{LOAD} + $R_{MICBIAS}$).

The time between the periodic button press measurements is specified using button_config. The inter-measurement period can be between 2 ms and 500 ms.

The button_config register is only active after a 4-pole jack has been detected. Setting button_config = 0 also disables the button measurements.

11.6 Clocking

The internal system clock (SYSCLK) from which all other clocks are derived is always at one of two possible frequencies:

- 12.288 MHz for SR from the 48 kHz family (8, 12, 16, 24, 32, 48, 96 kHz)
- 11.2896 MHz for SR from the 44.1 kHz family (11.025, 22.05, 44.1, 88.2 kHz).

DA7219 can run with or without an applied MCLK. If no MCLK is applied, the internal reference oscillator will clock the device. However when using the DAI an MCLK must be provided and correctly configured.

The DA7219 contains a phase-locked loop (PLL), which supports a range of clocking modes and input clock (MCLK) frequencies.

11.6.1 MCLK Input

MCLK is the master clock input which must be in the range of 2 MHz to 54 MHz.

MCLK can be applied as a full-amplitude square wave, or as a low-amplitude sine wave if the MCLK squarer circuit has been enabled. The clock squarer circuit is enabled by writing pll_mclk_sqr_en = 1. This clock squarer allows a sine wave or other low amplitude clock (down to 300 mVpp) to be applied to the chip. The MCLK input is AC coupled on chip when using the clock squarer mode.

11.6.1.1 MCLK Detection

A clock detection circuit will set bit [0] of pll_srm_status = 1 whenever the applied MCLK frequency is above the minimum detection frequency of approximately 1 MHz. Whenever this bit is high, the MCLK signal is selected as the clock input to the PLL.

11.6.2 Audio Reference Oscillator

For best audio performance, a system clock within the specified range is required. The DA7219 codec has an internal reference oscillator that provides the system clock when there is no valid MCLK signal.

The reference oscillator is automatically enabled whenever the codec is in ACTIVE mode and the MCLK frequency is below the minimum frequency of 1 MHz. When the codec enters STANDBY mode, the oscillator is automatically disabled to save power.

11.6.3 PLL Bypass Mode

If an MCLK signal at 11.2896/12.288 MHz or 22.5792/24.576 MHz or 45.1584/49.152 MHz is available, the PLL is not required and should be disabled to save power. PLL bypass mode is activated by setting pll_mode = 00.

In this mode the PLL is bypassed and an audio frequency clock is applied to the MCLK pin of the codec. The required clock frequency depends on the sample rate at which the audio DACs and ADCs are operating. These clock frequencies are summarized in Table 42 for the range of DAC and ADC sample rates that can be configured using the SR register.

Table 42: Sample Rate Control Register and Corresponding System Clock Frequency

Sample Rate, FS (kHz)	SR Register	System Clock Frequency (MHz)
8	0001	12.288
11.025	0010	11.2896
12	0011	12.288
16	0101	12.288
22.05	0110	11.2896
24	0111	12.288

32	1001	12.288
44.1	1010	11.2896
48	1011	12.288
88.2	1110	11.2896
96	1111	12.288

If digital playback or record is required in bypass mode then the MCLK frequency should be set to 11.2896/12.288 MHz, or to 22.5792/24.576 MHz, or to 45.1584/49.152 MHz and pll_indiv should be programmed accordingly.

If no valid MCLK is detected, the output of the internal reference oscillator is used instead. However in this case only analog bypass paths may be used.

11.6.4 PLL Normal Mode (DAI Master)

The DA7212 contains a phase locked loop (PLL) that can be used to generate the required 11.2896 MHz or 12.288 MHz internal system clock when a frequency of between 2 MHz and 54 MHz is applied to MCLK. This allows sharing of clocks between devices in an application, reducing total system cost. For example, the codec may operate from a common 13 MHz or 19.2 MHz system clock frequency.

The PLL is enabled by asserting pll_mode = 01. Once the PLL is enabled and has achieved phase lock, PLL bypass mode is disabled, and the output of the PLL is used as the system clock.

The PLL input divider register (pll_indiv) is used to reduce the PLL reference frequency to the usable range of 2 MHz to 54 MHz as shown in Table 43, this reduces the PLL reference frequency according to the following equation:

FREF = FMCLK ÷ N

Table 43: PLL Input Divider

MCLK Input Frequency (MHz)	Input Divider, (÷N)	pll_indiv Register (0x27 [3:2])
2 – 5	÷1	000
5 – 10	÷2	001
10 – 20	÷4	010
20 – 40	÷8	011
40 – 54	÷16	100

The value of the PLL feedback divider is used to set the voltage controlled oscillator (VCO) frequency to eight times the required system clock frequency (see Table 37).

FVCO = FREF × PLL feedback divider

The value of the PLL feedback divider is an unsigned number in the range of 0 to 128. It consists of seven integer bits and 13 fractional bits split across three registers:

- PLL_INTEGER holds the seven integer bits
- PLL_FRAC_TOP holds the top bits (MSB) of the fractional part of the divisor
- PLL_FRAC_BOT holds the bottom bits (LSB) of the fractional part of the divisor

11.6.5 Example Calculation of the Feedback Divider Setting

A codec is operating with Fs (sample rate) = 48 kHz and a reference input clock frequency of 12.288 MHz. The required output frequency = 98.304 MHz.

The reference clock input = 12.288 MHz, which falls in the range 10 MHz to 20 MHz, so pll_indiv will be set to 0b010 (dividing the reference input frequency by four, see Table 43.

The formula for calculating the feedback divider is:

Feedback divider (F) = (VCO output frequency * input divider (pll_indiv)) / reference input clock

Feedback divider = (98.304 * 4) / 12.288 = 32

So

- pll_fbdiv_integer (holding the seven integer bits) = 0x20
- pll_fbdiv_frac_top (holding the top bits (MSB) of the fractional part of the divisor) = 0x00
- pll_fbdiv_frac_bot (holding the bottom bits (LSB) of the fractional part of the divisor) = 0x00

Table 44 shows example register settings that will configure the PLL when using a 13 MHz, 15 MHz or 19.2 MHz clock. Any MCLK input frequency between 2 MHz and 54 MHz is supported. pll_indiv must be used to reduce the PLL reference frequency to the usable range of 2 MHz to 5 MHz as shown in Table 43.

Table 44: Example PLL Configurations

MCLK input frequency (MHz)	System clock frequency (MHz)	pll_mode register	PLL_FRAC_TOP register	PLL_FRAC_BOT register
13	11.2896	0x01	0x19	0x45
13	12.288	0x01	0x07	0xEA
15	11.2896	0x01	0x02	0xB4
15	12.288	0x01	0x06	0xDC
19.2	11.2896	0x01	0x1A	0x1C
19.2	12.288	0x01	0x0F	0x5C

11.6.6 PLL SRM Mode (DAI Slave)

SRM mode enables the PLL output clock to be synchronized to the incoming WCLK signal on the DAI. The SRM PLL mode is enabled by setting pll_mode = 10.

When using the DAI in slave mode with the SRM enabled, removing and re-applying the DAI interface word clock WCLK may cause the PLL lock to be lost. To re-lock the PLL it is recommended that you disable the SRM (pll_mode = 00), reset the PLL by re-writing to register PLL_INTEGER, and then re-enable the SRM (pll_mode = 10) after the DAI WCLK has been reapplied.

When switching sample rates between 44.1 kHz and 48 kHz (or between the multiples of these sample rates), SRM must be disabled and then re-enabled using register bit pll_mode.

11.7 Reference Generation

11.7.1 Voltage References

The audio circuits use supply-derived references of 0.45*V_{DD} (VMID) and 0.9*V_{DD} (DACREF). There is also a bandgap-derived fixed voltage reference of 1.2 V (VREF). All three voltage references require off-chip decoupling capacitors (see Appendix B.6).

Both VREF and VMID are automatically enabled whenever the device enters ACTIVE mode. They are automatically disabled when entering STANDBY mode.

The VMID reference comes from a high-resistance voltage divider, which combines with the decoupling capacitor to create a large RC (resistance-capacitance) time constant. This ensures a noise-free VMID reference.

To minimize start-up time, set vmid_fast_charge = 1. This enables a low resistance path to charge the decoupling capacitor faster.

Fast charge (vmid_fast_charge) must be disabled after start-up as it will increase the noise on the VMID reference.

The bandgap reference VREF also takes time to charge its decoupling capacitor, but an internal timer ensures that no circuit that requires VREF is enabled until VREF has reached 1.2 V.

The DACREF voltage reference is produced from VMID by a times-two buffer so is capable of charging its decoupling capacitor quickly.

11.7.2 Bias Currents

DA7219 has a master bias current generation block, enabled by default, controlled using the bias_en bit. Each subsystem has its own local current generation block, which is automatically enabled whenever any of its subblocks are enabled.

11.7.3 Voltage Levels

11.7.3.1 IO Voltage Level

The digital input/output pins can be set to operate in either a high voltage (2.5 V to 3.6 V) or low voltage (1.5 V to 2.5 V) range using the io_voltage_level bit. See Table 45.

Table 45: IO Voltage Level Setting

io_voltage_level Setting	Digital I/O Voltage Range (V)
0	2.5 to 3.6
1	1.2 to 2.5

11.8 I^2C Control Interface

DA7219 is completely software-controlled from the host by registers accessed via an I^2C compliant serial control interface. Data is shifted into or out of the DA7219 under the control of the host processor, which also provides the serial clock.

The I^2C clock is supplied by the SCL line and the bidirectional I^2C data is carried by the SDA line. The I^2C interface is open-drain supporting multiple devices on a single line. The bus lines have to be pulled HIGH by external pull-up resistors (1 kΩ to 20 kΩ range). The attached devices only drive the bus lines LOW by connecting them to ground. This means that two devices cannot conflict if they drive the bus simultaneously.

Table 46: Device I²C Slave Addresses

Register cif_i2c_addr_cfg	Device I²C Address
00	0x18
01	0x19
10	0x1A (default)
11	0x1B

In Standard/Fast mode the highest frequency of the bus is 1 MHz. The exact frequency can be determined by the application and does not have any relation to the DA7219 internal clock signals. DA7219 will follow the host clock speed within the described limitations and does not initiate any clock arbitration or slow-down.

In High-Speed mode the maximum frequency of the bus can be increased up to 3.4 MHz. This mode is supported if the SCL line is driven with a push-pull stage from the host and if the host enables an external 3 mA pull-up at the SDA pin to decrease the rise time of the data. In this mode the SDA line on DA7219 is able to sink up to 12 mA. In all other respects the High-Speed mode behaves as the Standard/Fast mode. Communication on the I²C bus always takes place between two devices, one acting as the master and the other as the slave. The DA7219 will only operate as a slave. The I²C interface has direct access to the whole register map of the DA7219.

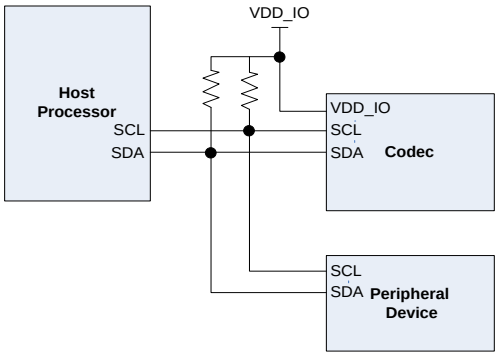

Figure 22: Schematic of the I²C Control Interface Bus

All data is transmitted across the I²C bus in groups of eight bits. To send a bit the SDA line is driven to the intended state while the SCL is LOW (a LOW on SCL indicates a zero bit). Once the SDA has settled, the SCL line is brought HIGH and then LOW. This pulse on SCL clocks the SDA bit into the receiver's shift register.

A two byte serial protocol is used containing one byte for address and one byte for data. Data and address transfer is transmitted MSB first for both read and write operations. All transmission begins with the START condition from the master while the bus is in the IDLE state (the bus is free). It is initiated by a HIGH to LOW transition on the SDA line while the SCL is in the HIGH state (a STOP condition is indicated by a LOW to HIGH transition on the SDA line while the SCL line is in the HIGH state).

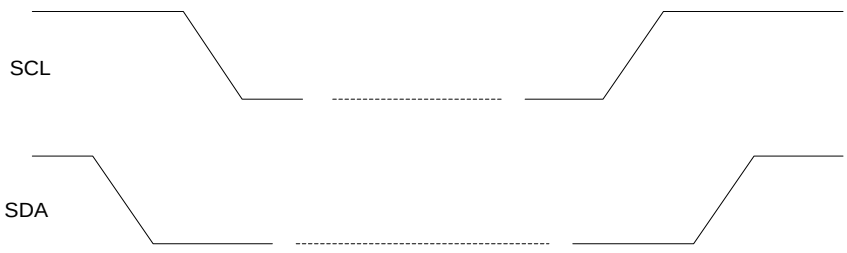

Figure 23: I²C START and STOP Conditions

The I²C bus is monitored by DA7219 for a valid slave address whenever the interface is enabled. It responds with an Acknowledge immediately when it receives its own slave address. The Acknowledge is done by pulling the SDA line LOW during the following clock cycle (white blocks marked with 'A' in Figure 24 to Figure 28).

The protocol for a register write from master to slave consists of a START condition, a slave address with read/write bit and the 8-bit register address followed by 8 bits of data terminated by a STOP condition (DA7219 responds to all bytes with Acknowledge). This is illustrated in Figure 24

Figure 24: I²C Byte Write (SDA line)

When the host reads data from a register it first has to write access DA7219 with the target register address and then read access DA7219 with a repeated START, or alternatively a second START condition. After receiving the data the host sends a Not Acknowledge (NAK) and terminates the transmission with a STOP condition:

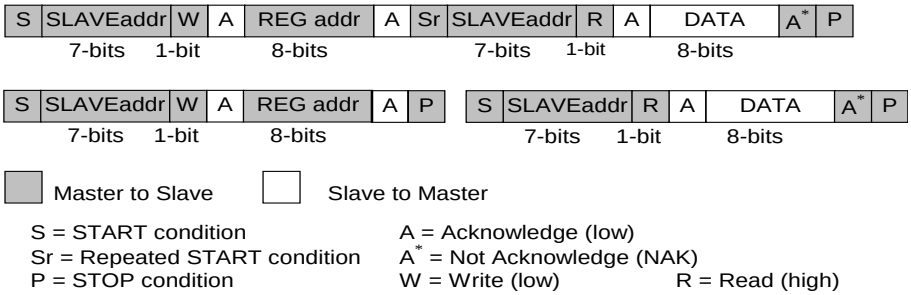

Figure 25: Examples of the I²C Byte Read (SDA line)

Consecutive (Page) Read-Out mode (cif_i2c_write_mode = 0) is initiated from the master by sending an Acknowledge instead of Not Acknowledge (NAK) after receipt of the data word. The I²C control block then increments the address pointer to the next I²C address and sends the data to the master. This enables an unlimited read of data bytes until the master sends an NAK directly after the receipt of data, followed by a subsequent STOP condition. If a non-existent I²C address is read out, the DA7219 will return code zero.

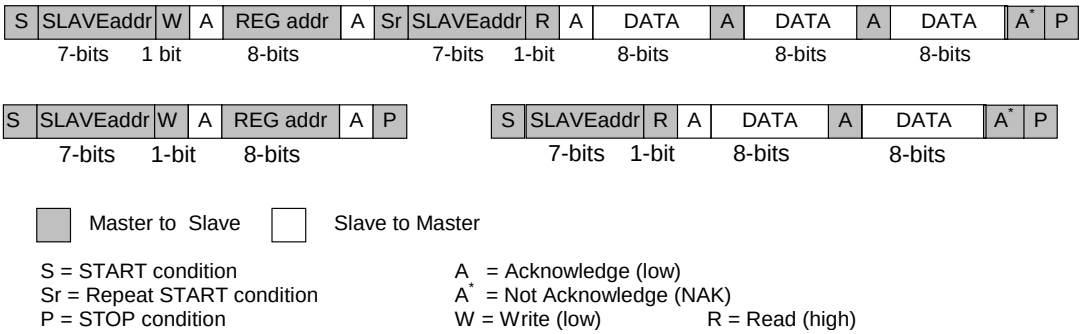

Figure 26: Examples of I²C Page Read (SDA line)

In Page mode the slave address after Sr (Repeated START condition) must be the same as the previous slave address.

Consecutive (Page) Write mode (cif_i2c_write_mode = 0) is supported if the master sends several data bytes following a slave register address. The I²C control block then increments the address

pointer to the next I²C address, stores the received data and sends an Acknowledge until the master sends the STOP condition.

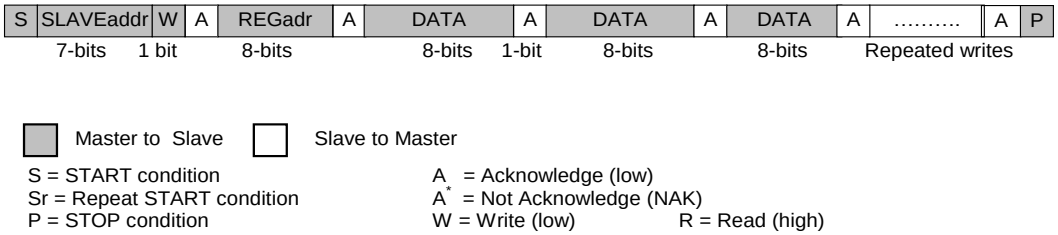

Figure 27: I²C Page Write (SDA line)

An alternative Repeated-Write mode that uses non-consecutive slave register addresses is available using the cif_i2c_write_mode register. In this Repeat Mode (cif_i2c_write_mode = 1), the slave can be configured to support a host's repeated write operations into several non-consecutive registers. Data is stored at the previously received register address. If a new START or STOP condition occurs within a message, the bus returns to Idle mode. This is illustrated in Figure 28.

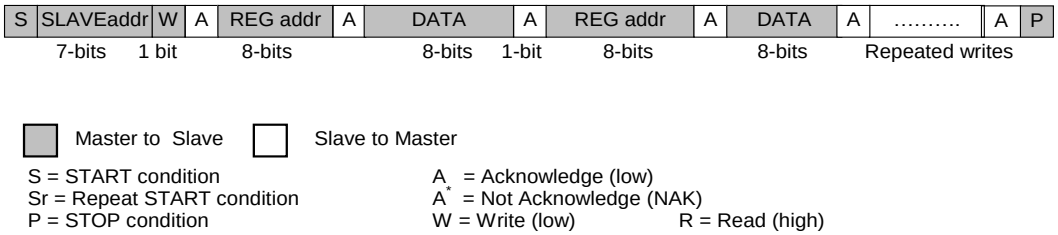

Figure 28: I²C Repeated Write (SDA line)

In Page mode (cif_i2c_write_mode = 0), both Page mode reads and writes using auto-incremented addresses, and Repeat mode reads and writes using non auto-incremented addresses, are supported. In Repeat mode (cif_i2c_write_mode = 1) however, only Repeat mode reads and writes are supported.

11.9 Digital Audio Interface

DA7219 provides one DAI to input DAC data or to output ADC data. It is enabled by asserting dai_en. The DSP provides flexible routing options allowing each interface to be connected to different signal paths as desired in each application.

The DAI consists of a four-wire serial interface, with bit clock (BCLK), word clock (WCLK), data in (DATIN) and data out (DATOUT) pins. Both master and slave clock modes are supported by the DA7219. Master mode is enabled by setting register dai_clk_en = 1. In Master mode, the bit clock and word clock signals are outputs from the codec. In Slave mode these are inputs to the codec.

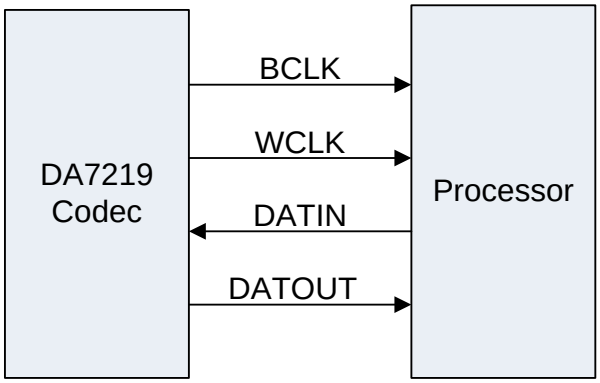

Figure 29: Master Mode (dai_clk_en = 1)

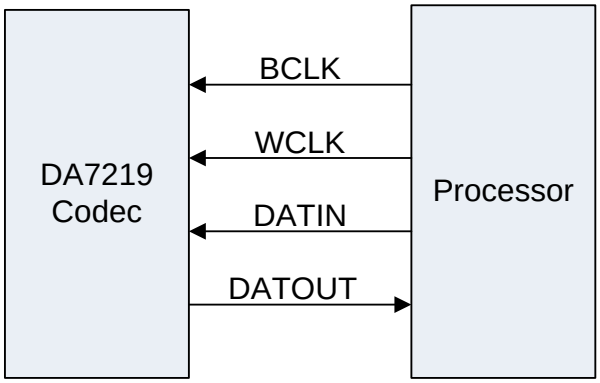

Figure 30: Slave Mode (dai_clk_en = 0)

The internal serialized DAI data is 24 bits wide. Serial data that is not 24 bits wide is either shortened or zero-filled at input to, or at output from, the DAI's internal 24-bit data width. The serial data word length can be configured to be 16, 20, 24 or 32 bits wide using the dai_word_length register bits.

Four different data formats are supported by the DAI. The data format is determined by the setting of the dai_format register bits.

The internal serialized DAI data is 24 bits wide. Serial data that is not 24 bits wide is either shortened or zero-filled at input to, or at output from, the DAI's internal 24-bit data width. The serial data word length can be configured to be 16, 20, 24 or 32 bits wide using the dai_word_length register bits.

Four different data formats are supported by the DAI. The data format is determined by the setting of the dai_format register bits:

- 00 = I^2S mode
- 01 = Left justified mode
- 10 = Right justified mode
- 11 = DSP mode

Time division multiplexing (TDM) is available in any of these modes to support the case where multiple devices are communicating simultaneously on the same bus. TDM is enabled by asserting the dai_tdm_mode_en bit.

11.9.1 DAI Channels

The DAI supports one or two channels, even in non-TDM modes. The number of channels required is specified by setting dai_ch_num which controls the position of the channels.

In TDM mode, each of the two channels can be individually enabled using the dai_tdm_ch_en register.

11.9.2 I²S Mode

In I²S mode (dai_format = 0), the MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. The MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.

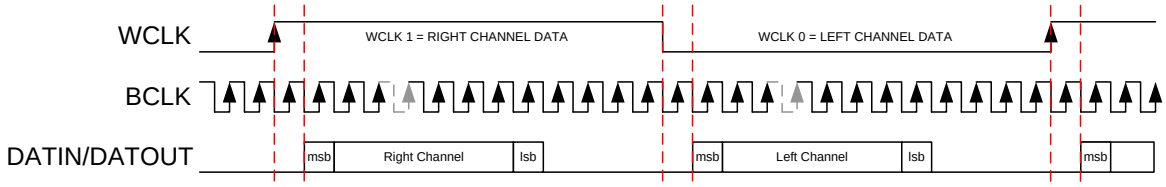

Figure 31: I²S Mode

11.9.3 Left Justified Mode

In left-justified mode (dai_format = 1), the MSB of the right channel is valid on the rising edge of the bit clock following the falling edge of the word clock. The MSB of the left channel is valid on the rising edge of the bit clock following the rising edge of the word clock.

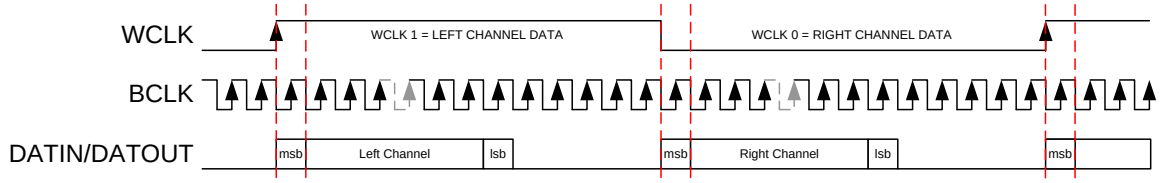

Figure 32: Left Justified Mode

11.9.4 Right Justified Mode

In right-justified mode (dai_format = 2), the LSB of the left channel is valid on the rising edge of the bit clock preceding the falling edge of word clock. The LSB of the right channel is valid on the rising edge of the bit clock preceding the rising edge of the word clock.

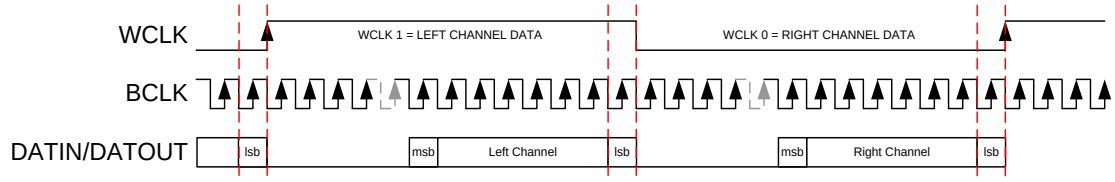

Figure 33: Right Justified Mode

11.9.5 DSP Mode

In DSP mode (dai_format = 3), the rising edge of the word clock starts the data transfer with the left channel data first and immediately followed by the right channel data. Each data bit is valid on the falling edge of the bit clock.

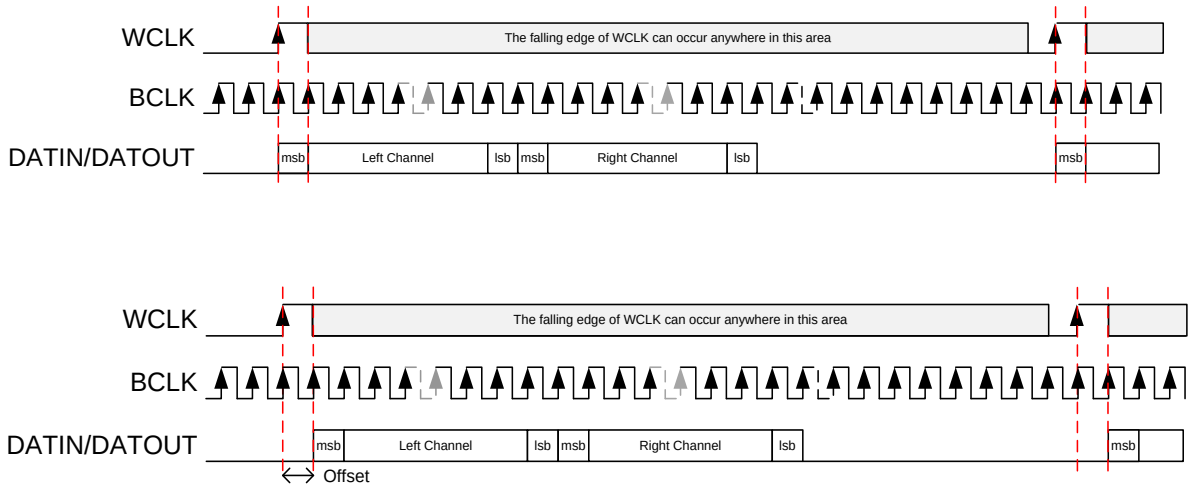

Figure 34 DSP Mode

12 Register Definitions

Table 47: Register map accdet_cad_00 page 0

Address Name	7	6	5	4	3	2	1	0
Register Page 0								
0x000000C0 ACCDET_STATUS_A	Reserved				micbias_up_sts	jack_pin_order_sts	jack_type_sts	jack_insertion_sts
0x000000C1 ACCDET_STATUS_B	button_type_sts							
0x000000C2 ACCDET_IRQ_EVENT_A	Reserved					e_jack_detect_complete	e_jack_removed	e_jack_inserted
0x000000C3 ACCDET_IRQ_EVENT_B	e_button_a_released	e_button_b_released	e_button_c_released	e_button_d_released	e_button_d_pressed	e_button_c_pressed	e_button_b_pressed	e_button_a_pressed
0x000000C4 ACCDET_IRQ_MASK_A	Reserved					m_jack_detect_complete	m_jack_removed	m_jack_inserted
0x000000C5 ACCDET_IRQ_MASK_B	m_button_a_released	m_button_b_released	m_button_c_released	m_button_d_released	m_button_d_pressed	m_button_c_pressed	m_button_b_pressed	m_button_a_pressed
0x000000C6 ACCDET_CONFIG_1	pin_order_det_en	jack_type_det_en	mic_det_thresh		button_config			accdet_en
0x000000C7 ACCDET_CONFIG_2	jackdet_rem_deb		jack_detect_rate		jackdet_debounce			accdet_pause
0x000000C8 ACCDET_CONFIG_3	A_D_BUTTON_THRESH							
0x000000C9 ACCDET_CONFIG_4	D_B_BUTTON_THRESH							
0x000000CA ACCDET_CONFIG_5	B_C_BUTTON_THRESH							
0x000000CB ACCDET_CONFIG_6	C_MIC_BUTTON_THRESH							
0x000000CC ACCDET_CONFIG_7	Reserved		jack_type_force	pin_order_force	adc_1_bit_repeat		button_average	
0x000000CD ACCDET_CONFIG_8	Reserved			hptest_comp	Reserved	hptest_res_sel		hptest_en

Table 48: ACCDET_STATUS_A (Page 0: 0x000000C0)

Bit	Mode	Symbol	Description	Reset
3	R	micbias_up_sts	Status of the microphone supply rail MICBIAS 0 = MICBIAS off 1 = MICBIAS on MICBIAS is enabled automatically when a 4-pole jack is inserted	0x0
2	R	jack_pin_order_sts	Status of the jack pin-order detection. Pins are measured in Tip-Ring1-Ring2-Sleeve order. 0 = LRGM (CTIA format) 1 = LRMG (OMTP format) The data in this bit field is only valid after the e_jack_detect_complete event has fired, that is, once e_jack_detect_complete = 1	0x0
1	R	jack_type_sts	Status of the jack-type detection. 0 = 3-pole jack detected 1 = 4-pole jack detected The data in this bit field is only valid after the e_jack_detect_complete event has fired, that is, once e_jack_detect_complete = 1	0x0
0	R	jack_insertion_sts	Jack insertion status 0 = No jack is present 1 = Jack is present	0x0

Table 49: ACCDET_STATUS_B (Page 0: 0x000000C1)

Bit	Mode	Symbol	Description	Reset
7:0	R	button_type_sts	The last measured 8-bit button impendance value from the ADC.	0x0

Table 50: ACCDET_IRQ_EVENT_A (Page 0: 0x000000C2)

Bit	Mode	Symbol	Description	Reset
2	R	e_jack_detect_complete	Jack detection IRQ event field. This is asserted once the jack detection has completed. This is a 'write 1 to clear' field. jack_type_sts and jack_pin_order_sts status bits are only valid after this event has been asserted.	0x0
1	R	e_jack_removed	Jack removal IRQ event field. This is asserted when a jack is removed. This is a 'write 1 to clear' field.	0x0
0	R	e_jack_inserted	Jack insertion IRQ event field. This is asserted when a jack is inserted. This is a 'write 1 to clear' field.	0x0

Table 51: ACCDET_IRQ_EVENT_B (Page 0: 0x000000C3)

Bit	Mode	Symbol	Description	Reset
7	R	e_button_a_released	Button A release IRQ event field. This is asserted when Button A is released. This is a 'write 1 to clear' field.	0x0
6	R	e_button_b_released	Button B release IRQ event field. This is asserted when Button B is released. This is a 'write 1 to clear' field.	0x0
5	R	e_button_c_released	Button C release IRQ event field. This is asserted when Button C is released. This is a 'write 1 to clear' field.	0x0
4	R	e_button_d_released	Button D release IRQ event field. This is asserted when Button D is released. This is a 'write 1 to clear' field.	0x0
3	R	e_button_d_pressed	Button D press IRQ event field. This is asserted when Button D is pressed. This is a 'write 1 to clear' field.	0x0
2	R	e_button_c_pressed	Button C press IRQ event field. This is asserted when Button C is pressed. This is a 'write 1 to clear' field.	0x0
1	R	e_button_b_pressed	Button B press IRQ event field. This is asserted when Button B is pressed. This is a 'write 1 to clear' field.	0x0
0	R	e_button_a_pressed	Button A press IRQ event field. This is asserted when Button A is pressed. This is a 'write 1 to clear' field.	0x0

Table 52: ACCDET_IRQ_MASK_A (Page 0: 0x000000C4)

Bit	Mode	Symbol	Description	Reset
2	R/W	m_jack_detect_complete	Interrupt mask for e_jack_detect_complete 0 = Jack detection IRQ is not masked 1 = Jack detection IRQ is masked	0x0
1	R/W	m_jack_removed	Interrupt mask for e_jack_removed 0 = Jack removal IRQ is not masked 1 = Jack removal IRQ is masked	0x0
0	R/W	m_jack_inserted	Interrupt mask for e_jack_inserted 0 = Jack insertion IRQ is not masked 1 = Jack insertion IRQ is masked	0x0

Table 53: ACCDET_IRQ_MASK_B (Page 0: 0x000000C5)

Bit	Mode	Symbol	Description	Reset
7	R/W	m_button_a_released	Interrupt mask for e_button_a_released 0 = Button A release IRQ is not masked 1 = Button A release IRQ is masked	0x0
6	R/W	m_button_b_released	Interrupt mask for e_button_b_released 0 = Button B release IRQ is not masked 1 = Button B release IRQ is masked	0x0
5	R/W	m_button_c_released	Interrupt mask for e_button_c_released 0 = Button C release IRQ is not masked 1 = Button C release IRQ is masked	0x0
4	R/W	m_button_d_released	Interrupt mask for e_button_d_released 0 = Button D release IRQ is not masked 1 = Button D release IRQ is masked	0x0
3	R/W	m_button_d_pressed	Interrupt mask for e_button_d_pressed 0 = Button D press IRQ is not masked 1 = Button D press IRQ is masked	0x0
2	R/W	m_button_c_pressed	Interrupt mask for e_button_c_pressed 0 = Button C press IRQ is not masked 1 = Button C press IRQ is masked	0x0
1	R/W	m_button_b_pressed	Interrupt mask for e_button_b_pressed 0 = Button B press IRQ is not masked 1 = Button B press IRQ is masked	0x0
0	R/W	m_button_a_pressed	Interrupt mask for e_button_a_pressed 0 = Button A press IRQ is not masked 1 = Button A press IRQ is masked	0x0

Table 54: ACCDET_CONFIG_1 (Page 0: 0x000000C6)

Bit	Mode	Symbol	Description	Reset
7	R/W	pin_order_det_en	Controls detection of the pin order on insertion of a 4-pole jack 0 = Pin order is determined by the setting of the pin_order_force register field when jack_type_sts = 4-pole 1 = Pin order detection (LRGM / LRMG) runs on insertion of a 4-pole Jack	0x1
6	R/W	jack_type_det_en	Controls detection of the type of jack (3-pole without a mic or 4-pole with a mic) when a jack is inserted 0 = The type of jack (3-pole or 4-pole) is determined by the setting of the jack_type_force register field 1 = Jack type detection runs on jack insertion to determine jack type (3-pole with no mic, or 4-pole with a mic)	0x1

Bit	Mode	Symbol	Description	Reset
5:4	R/W	mic_det_thresh	Impedance threshold for MIC detection measurement. If SLEEVE to RING2 impedance is below the threshold specified here, jack_type_sts is set to 0 (3-pole). If SLEEVE to RING2 impedance is above the threshold specified here, jack_type_sts is set to 1 (4-pole). 00 = 200 Ω 01 = 500 Ω (default) 10 = 750 Ω 11 = 1000 Ω	0x1
3:1	R/W	button_config	Specifies the time between the periodic button-press measurements when jack_type_sts = 1 (4-pole). 000 = Disabled 001 = 2 ms 010 = 5 ms 011 = 10 ms (default) 100 = 50 ms 101 = 100 ms 110 = 200 ms 111 = 500 ms	0x3
0	R/W	accdet_en	Controls accessory detection 0 = Accessory detection is disabled 1 = Accessory detection is enabled The ACCDET analog components require master bias to be enabled before enabling the digital block	0x0

Table 55: ACCDET_CONFIG_2 (Page 0: 0x000000C7)

Bit	Mode	Symbol	Description	Reset
7:6	R/W	jackdet_rem_deb	Control of the JACKDET deassertion debounce 00 = 1 ms (default) 01 = 5 ms 10 = 10 ms 11 = 20 ms	0x0

Bit	Mode	Symbol	Description	Reset
5:4	R/W	jack_detect_rate	Controls the jack-detection latency time, that is, the time from assertion of e_jack_insertion to assertion of e_jack_detect_complete 3-pole jack: 00 = 32 ms 01 = 64 ms 10 = 128 ms 11 = 256 ms (default) 4-pole jack: 00 = 64 ms 01 = 128 ms 10 = 256 ms 11 = 512 ms (default) Latency time is altered by changing the ramp rate of the MICDET current during jack type and pin order detection.	0x3
3:1	R/W	jackdet_debounce	Control of the JACKDET assertion debounce 0 = 5 ms 1 = 10 ms 2 = 20 ms (default) 3 = 50 ms 4 = 100 ms 5 = 200 ms 6 = 500 ms 7 = 1 s	0x2
0	R/W	accdet_pause	Pauses the periodic button checking within the accessory detection function. This allows you to reconfigure the button measurements or to change MICBIAS or both. 0 = No effect 1 = Pauses the periodic button checking within the accessory detection block The difference between pausing by asserting this register field and disabling the accessory detection function entirely (accdet_en = 0) is that pausing allows for dynamic reconfiguration of the button measurements. When paused, DA7219 will still respond to new removal or insertion events whereas when disabled, no insertion or removal events are detected.	0x0

Table 56: ACCDET_CONFIG_3 (Page 0: 0x000000C8)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	A_D_BUTTON_THRESH	Sets the impedance threshold between Button A and Button D. If the measured impedance of a button-press is lower than the threshold value specified here, the button that was pressed is Button A. The value of this register field is a calculated value. It is calculated as: 256 * Required threshold in Ω/(Required threshold in Ω + MICBIAS resistance in Ω) Example calculation: Assuming that MICBIAS resistance = 2200 Ω and the required threshold = 89 Ω, the bit value of this register field = 256 * 89/(89 + 2200) = 10 [or 0x0A]. So, in this example, setting this register field = 0x0A will give you a threshold value of 89 Ω.	0xA

Table 57: ACCDET_CONFIG_4 (Page 0: 0x000000C9)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	D_B_BUTTON_THRESH	Sets the impedance threshold between Button D and Button B. If the measured impedance of a button-press is lower than the threshold value specified here, the button that was pressed is Button D. The value of this register field is a calculated value. It is calculated as: 256 * Required threshold in Ω/(Required threshold in Ω + MICBIAS resistance in Ω) Example calculation: Assuming that MICBIAS resistance = 2200Ω and the required threshold = 195 Ω, the bit value of this register field = 256 * 195/(195 + 2200) = 21 [or 0x15]. So, in this example, setting this register field = 0x15 will give you a threshold value of 195 Ω.	0x16

Table 58: ACCDET_CONFIG_5 (Page 0: 0x000000CA)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	B_C_BUTTON_THRESH	Sets the impedance threshold between Button B and Button C. If the measured impedance of a button-press is lower than the threshold value specified here, the button that was pressed is Button B. The value of this register field is a calculated value. It is calculated as: 256 * Required threshold in Ω/(Required threshold in Ω + MICBIAS resistance in Ω) Example calculation: Assuming that MICBIAS resistance = 2200 Ω and the required threshold = 325 Ω, the bit value of this register field = 256 * 325/(325 + 2200) = 33 [or 0x21]. So, in this example, setting this register field = 0x21 will give you a threshold value of 325 Ω.	0x21

Table 59: ACCDET_CONFIG_6 (Page 0: 0x000000CB)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	C_MIC_BUTTON_THRESH	Sets the impedance threshold between Button C and the microphone. If the measured impedance of a button-press is lower than the threshold value specified here, the button that was pressed is Button C. The value of this register field is a calculated value. It is calculated as: 256 * Required threshold in Ω/(Required threshold in Ω + MICBIAS resistance in Ω) Example calculation: Assuming that MICBIAS resistance = 2200 Ω and the required threshold = 688 Ω, the bit value of this register field = 256 * 688/(688 + 2200) = 61 [or 0x3D]. So, in this example, setting this register field = 0x3D will give you a threshold value of 688 Ω.	0x3E

Table 60: ACCDET_CONFIG_7 (Page 0: 0x000000CC)

Bit	Mode	Symbol	Description	Reset
5	R/W	jack_type_force	Specifies the jack type when jack type detection is disabled (jack_type_det_en is 0) 0 = 3-pole jack is specified 1 = 4-pole jack is specified	0x0

Bit	Mode	Symbol	Description	Reset
4	R/W	pin_order_force	Specifies the jack pin order for 4-pole jacks when pin order detection is disabled (pin_order_det_en = 0) 0 = LRGM (CTIA format) 1 = LRMG (OMTP format)	0x0
3:2	R/W	adc_1_bit_repeat	Sets the number of repeated 1-bit measurements. Repeating the 1-bit measurements multiple times gives greater noise immunity but adds latency, and possible distortion, during periodic button checking 00 = One 1-bit measurement (default) 01 = Two 1-bit measurements 10 = Four 1-bit measurements 11 = Eight 1-bit measurements	0x0
1:0	R/W	button_average	Sets the number of repeated 8-bit ADC measurements used to generate an averaged result Using more measurements for averaging will increase button-checking noise immunity but also increases the detection latency by about 1 ms per measurement 00 = One 8-bit measurement (no averaging) 01 = Two 8-bit measurements used for averaging (default) 10 = Four 8-bit measurements used for averaging 11 = Eight 8-bit measurements used for averaging	0x1

Table 61: ACCDET_CONFIG_8 (Page 0: 0x000000CD)

Bit	Mode	Symbol	Description	Reset
4	R	hptest_comp	HP TEST comparator result 1 = HP impedance is < threshold 0 = HP impedance is > threshold	0x0
2:1	R/W	hptest_res_sel	HP Impedance Test threshold control 00 - 1000 Ω 01 = 2500 Ω 10 = 5000 Ω 11 = 10000 Ω	0x1
0	R/W	hptest_en	Headphone impedance test block control 0 = HP impedance test block disabled 1 = HP impedance test block enabled	0x0

Table 62: Register map adc_filters_cad_00 page 0

Address Name	7	6	5	4	3	2	1	0
Register Page 0								
0x00000038 ADC_FILTERS1	adc_hpf_en	Reserved	adc_audio_hpf_corner		adc_voice_en	adc_voice_hpf_corner		

Table 63: ADC_FILTERS1 (Page 0: 0x00000038)

Bit	Mode	Symbol	Description	Reset
7	R/W	adc_hpf_en	ADC high pass filter control 0 = ADC high pass filter disabled 1 = ADC high pass filter enabled	0x1
5:4	R/W	adc_audio_hpf_corner	ADC high pass filter 3 dB cut-off point. At 48 kHz, the cutoff point is at: 00 = 2 Hz 01 = 4 Hz 10 = 8 Hz 11 = 16 Hz For other sample rates the 3 dB cuttoff point scales proportionately	0x0
3	R/W	adc_voice_en	ADC voice filter control 0 = Voice filter disabled 1 = Voice filter enabled	0x0
2:0	R/W	adc_voice_hpf_corner	Voice (8 kHz) high-pass 3 dB cutoff point 000 = 2.5 Hz 001 = 25 Hz 010 = 50 Hz 011 = 100 Hz 100 = 150 Hz 101 = 200 Hz 110 = 300 Hz 111 = 400 Hz For other sample rates the 3 dB cutoff point scales proportionately	0x0

Table 64: Register map alc_cad_00 page 0

Address Name	7	6	5	4	3	2	1	0
Register Page 0								
0x0000002F ALC_CTRL1	Reserved		alc_calib_overflow	alc_auto_calib_en	alc_en	Reserved	alc_sync_mode	alc_offset_en

Address Name	7	6	5	4	3	2	1	0
Register Page 0								
0x0000009A ALC_CTRL2	alc_release				alc_attack			
0x0000009B ALC_CTRL3	alc_integ_release		alc_integ_attack		alc_hold			
0x0000009C ALC_NOISE	Reserved		alc_noise					
0x0000009D ALC_TARGET_MIN	Reserved		alc_threshold_min					
0x0000009E ALC_TARGET_MAX	Reserved		alc_threshold_max					
0x0000009F ALC_GAIN_LIMITS	alc_gain_max				alc_atten_max			
0x000000A0 ALC_ANA_GAIN_LIMITS	Reserved		alc_ana_gain_max		Reserved		alc_ana_gain_min	
0x000000A1 ALC_ANTICLIP_CTRL	alc_antipclip_en		Reserved					alc_anticlip_step
0x000000A2 ALC_ANTICLIP_LEVEL	Reserved		alc_anticlip_level					
0x000000A3 ALC_OFFSET_AUTO_M_L	alc_offset_auto_m_l							
0x000000A4 ALC_OFFSET_AUTO_U_L	Reserved				alc_offset_auto_u_l			

Table 65: ALC_CTRL1 (Page 0: 0x0000002F)

Bit	Mode	Symbol	Description	Reset
5	R	alc_calib_overflow	Indicates that an offset overflow occurred during calibration 0 = No offset overflow 1 = Offset overflow occurred	0x0
4	R/W	alc_auto_calib_en	Automatic calibration control 0 = Automatic calibration not enabled 1 = Automatic calibration enabled This is a self-clearing bit	0x0
3	R/W	alc_en	Controls the ALC operation on the left ADC channel 0 = ALC is disabled 1 = ALC is enabled	0x0
1	R/W	alc_sync_mode	ALC hybrid mode control. Hybrid mode uses both analogue and digital gains. 0 = Hybrid mode is Off (digital gain only) 1 = Hybrid mode is On (digital and analogue gain)	0x0

Bit	Mode	Symbol	Description	Reset
0	R/W	alc_offset_en	DC offset cancellation control 0 = DC offset cancellation is disabled 1 = DC offset cancellation is enabled	0x0

Table 66: ALC_CTRL2 (Page 0: 0x0000009A)

Bit	Mode	Symbol	Description	Reset
7:4	R/W	alc_release	ALC release rate. This is the speed at which the ALC increases the gain. 0000 = 28.66/Fs (0.6 ms/dB @48 kHz) 0001 = 57.33/Fs (1.2 ms/dB @48 kHz) 0010 = 114.66/Fs (2.4 ms/dB @48 kHz) then doubling at every step to... 1001 = 14674/Fs (306 ms/dB @48 kHz) 1010 to 1111 = 29348/Fs (611 ms/dB @48 kHz)	0x0
3:0	R/W	alc_attack	ALC attack rate control. This is the speed at which the ALC reduces the gain. 0000 = 7.33/Fs (0.153 ms/dB @48 kHz) 0001 = 14.66/Fs (0.305 ms/dB @48 kHz) 0010 = 29.32/Fs (0.612 ms/dB @48 kHz) then doubling at every step to... 1011 = 15012/Fs (312 ms/dB @48 kHz) 1100 to 1111 = 30024/Fs (625 ms/dB @48 kHz)	0x0

Table 67: ALC_CTRL3 (Page 0: 0x0000009B)

Bit	Mode	Symbol	Description	Reset
7:6	R/W	alc_integ_release	Controls the rate at which the input signal envelope is tracked as the signal gets smaller 00 = 1/4 01 = 1/16 10 = 1/256 11 = 1/65537	0x0
5:4	R/W	alc_integ_attack	Controls the rate at which the input signal envelope is tracked as the signal gets larger 00 = 1/4 01 = 1/16 10 = 1/256 11 = 1/65537	0x0

Bit	Mode	Symbol	Description	Reset
3:0	R/W	alc_hold	ALC hold time control. This is the period the ALC waits before releasing. 0000 = 62/Fs (1.3 ms @48 kHz) 0001 = 124/Fs (2.6 ms @48 kHz) 0010 = 248/Fs (5.2 ms @48 kHz) then doubling at every step to… 1110 = 1015808/Fs (21 s @48 kHz) 1111 = 2031616/Fs (42 s @48 kHz)	0x0

Table 68: ALC_NOISE (Page 0: 0x0000009C)

Bit	Mode	Symbol	Description	Reset
5:0	R/W	alc_noise	Sets the threshold below which input signals will not cause the ALC to change gain 000000 = 0 dBFS 000001 = -1.5 dBFS 000010 = -3.0 dBFS then continuing in -1.5 dBFS steps to… 111110 = -93.0 dBFS 111111 = -94.5 dBFS (default)	0x3F

Table 69: ALC_TARGET_MIN (Page 0: 0x0000009D)

Bit	Mode	Symbol	Description	Reset
5:0	R/W	alc_threshold_min	Sets the minimum amplitude of the ALC output signal at which the ALC increases the gain. If the minimum attenuation level is reached, the ALC will not increase the gain even if this threshold is breached. 000000 = 0 dBFS 000001 = -1.5 dBFS 000010 = -3.0 dBFS then continuing in -1.5 dBFS steps to... 111110 = -93.0 dBFS 111111 = -94.5 dBFS (default)	0x3F

Table 70: ALC_TARGET_MAX (Page 0: 0x0000009E)

Bit	Mode	Symbol	Description	Reset
5:0	R/W	alc_threshold_max	Sets the maximum amplitude of the ALC output signal at which the ALC reduces the gain. If the maximum attenuation level is reached, the ALC will not reduce the gain even if this threshold is exceeded. 000000 = 0 dBFS 000001 = -1.5 dBFS 000010 = -3.0 dBFS then continuing in -1.5 dBFS steps to... 111110 = -93.0 dBFS 111111 = -94.5 dBFS	0x0

Table 71: ALC_GAIN_LIMITS (Page 0: 0x0000009F)

Bit	Mode	Symbol	Description	Reset
7:4	R/W	alc_gain_max	Sets the maximum amount of gain that can be applied to the input signal by the ALC when the input signal is large relative to the maximum threshold 0000 = 0 dB 0001 = 6 dB 0010 = 12 dB then continuing in 6 dB steps to… 1110 = 84 dB 1111 = 90 dB	0xF
3:0	R/W	alc_atten_max	Sets the maximum amount of attenuation that can be applied to the input signal by the ALC when the input signal is large relative to the maximum threshold 0000 = 0 dB 0001 = 6 dB 0010 = 12 dB then continuing in 6 dB steps to… 1110 = 84 dB 1111 = 90 dB	0xF

Table 72: ALC_ANA_GAIN_LIMITS (Page 0: 0x000000A0)

Bit	Mode	Symbol	Description	Reset
6:4	R/W	alc_ana_gain_max	Sets the maximum amount of analogue gain that can be applied to the input signal by the ALC when the input signal is large relative to the maximum threshold. This setting applies only to mixed analogue and digital gain mode (alc_sync_mode = 1). 000 = reserved 001 = 0 dB 010 = 6 dB 011 = 12 dB 100 = 18 dB 101 = 24 dB 110 = 30 dB 111 = 36 dB	0x7
2:0	R/W	alc_ana_gain_min	Sets the minimum amount of analogue gain that can be applied to the input signal by the ALC when the input signal is large relative to the maximum threshold. This setting applies only to mixed analogue and digital gain mode (alc_sync_mode = 1). 000 = reserved 001 = 0 dB 010 = 6 dB 011 = 12 dB 100 = 18 dB 101 = 24 dB 110 = 30 dB 111 = 36 dB	0x1

Table 73: ALC_ANTICLIP_CTRL (Page 0: 0x000000A1)

Bit	Mode	Symbol	Description	Reset
7	R/W	alc_antipclip_en	Controls the ALC signal clip prevention mechanism 0 = Clip prevention is disabled 1 = Clip prevention is enabled	0x0
1:0	R/W	alc_anticlip_step	Sets the attack rate for the ALC when the output signal exceeds the anticlip threshold level 00 = 0.034 dB/Fs 01 = 0.068 dB/Fs 10 = 0.136 dB/Fs 11 = 0.272 dB/Fs	0x0

Table 74: ALC_ANTICLIP_LEVEL (Page 0: 0x000000A2)

Bit	Mode	Symbol	Description	Reset
6:0	R/W	alc_anticlip_level	ALC anticlip threshold control. The ALC anticlip operates when signals are above this threshold. The formula used to calculate the threshold value, using 'x' to denote the decimal value of this bit field, is: x = ((x+1)/128) Fs 0x00 = 0.0078 Fs 0x01 = 0.0156 Fs 0x02 = 0.0234 Fs then contnuing in aproximately 0.0078 steps to... 0x7E = 0.9922 Fs 0x7F = 1.0 Fs	0x0

Table 75: ALC_OFFSET_AUTO_M_L (Page 0: 0x000000A3)

Bit	Mode	Symbol	Description	Reset
7:0	R	alc_offset_auto_m_l	This read-only bit field contains the middle eight bits (bits [15:8]) of the value used for automatic offset correction	0x0

Table 76: ALC_OFFSET_AUTO_U_L (Page 0: 0x000000A4)

Bit	Mode	Symbol	Description	Reset
3:0	R	alc_offset_auto_u_l	This read-only bit field contains the upper four bits (bits [19:16]) of the value used for automatic offset correction	0x0

Table 77: Register map analogue_cad_00 page 0

Address Name	7	6	5	4	3	2	1	0
Register Page 0								
0x00000006 MIC_1_GAIN_STATUS	Reserved					mic_1_amp_gain_status		
0x00000008 MIXIN_L_GAIN_STATUS	Reserved				mixin_l_amp_gain_status			
0x0000000A ADC_L_GAIN_STATUS	Reserved	adc_l_digital_gain_status						

Address Name	7	6	5	4	3	2	1	0
Register Page 0								
0x0000000C DAC_L_GAIN_STATUS	Reserved	dac_l_digital_gain_status						
0x0000000D DAC_R_GAIN_STATUS	Reserved	dac_r_digital_gain_status						
0x0000000E HP_L_GAIN_STATUS	Reserved		hp_l_amp_gain_status					
0x0000000F HP_R_GAIN_STATUS	Reserved		hp_r_amp_gain_status					
0x00000010 MIC_1_SELECT	Reserved						mic_1_amp_in_sel	
0x00000032 REFERENCES	Reserved			vmid_fast_charge	bias_en	Reserved		
0x00000033 MIXIN_L_SELECT	Reserved						mixin_l_mix_select	
0x00000034 MIXIN_L_GAIN	Reserved				mixin_l_amp_gain			
0x00000036 ADC_L_GAIN	Reserved	adc_l_digital_gain						
0x00000039 MIC_1_GAIN	Reserved					mic_1_amp_gain		
0x00000045 DAC_L_GAIN	Reserved	dac_l_digital_gain						
0x00000046 DAC_R_GAIN	Reserved	dac_r_digital_gain						
0x00000048 HP_L_GAIN	Reserved		hp_l_amp_gain					
0x00000049 HP_R_GAIN	Reserved		hp_r_amp_gain					
0x0000004B MIXOUT_L_SELECT	Reserved						mixout_l_mix_select	
0x0000004C MIXOUT_R_SELECT	Reserved						mixout_r_mix_select	
0x00000062 MICBIAS_CTRL	Reserved				micbias1_en	micbias1_level		
0x00000063 MIC_1_CTRL	mic_1_amp_en	mic_1_amp_mute_en	mic_1_amp_ramp_en	Reserved				
0x00000065 MIXIN_L_CTRL	mixin_l_amp_en	mixin_l_amp_mute_en	mixin_l_amp_ramp_en	mixin_l_amp_zc_en	mixin_l_mix_en	Reserved		
0x00000067 ADC_L_CTRL	adc_l_en	adc_l_mute_en	adc_l_ramp_en	Reserved				
0x00000069 DAC_L_CTRL	dac_l_en	dac_l_mute_en	dac_l_ramp_en	Reserved				

Address Name	7	6	5	4	3	2	1	0
Register Page 0								
0x0000006A DAC_R_CTRL	dac_r_en	dac_r_mute_en	dac_r_ramp_en	Reserved				
0x0000006B HP_L_CTRL	hp_l_amp_en	hp_l_amp_mute_en	hp_l_amp_ramp_en	hp_l_amp_zc_en	hp_l_amp_oe	hp_l_amp_min_gain_en	Reserved	
0x0000006C HP_R_CTRL	hp_r_amp_en	hp_r_amp_mute_en	hp_r_amp_ramp_en	hp_r_amp_zc_en	hp_r_amp_oe	hp_r_amp_min_gain_en	Reserved	
0x0000006E MIXOUT_L_CTRL	mixout_l_amp_en	Reserved						
0x0000006F MIXOUT_R_CTRL	mixout_r_amp_en	Reserved						
0x00000091 IO_CTRL	Reserved							io_voltage_level

Table 78: MIC_1_GAIN_STATUS (Page 0: 0x00000006)

Bit	Mode	Symbol	Description	Reset
2:0	R	mic_1_amp_gain_status	Contains the currently active mic_1_amp gain setting 000 = -6 dB 001 = 0 dB 010 = 6 dB 011 = 12 dB 100 = 18 dB 101 = 24 dB 110 = 30 dB 111 = 36 dB	0x1

Table 79: MIXIN_L_GAIN_STATUS (Page 0: 0x00000008)

Bit	Mode	Symbol	Description	Reset
3:0	R	mixin_l_amp_gain_status	Contains the currently active mixin_l_amp gain setting 0000 = -4.5 dB 0001 = -3.0 dB 0010 = -1.5 dB 0011 = 0.0 dB then continuing in 1.5 dB steps to… 1110 = 16.5 dB 1111 = 18.0 dB	0x0

Table 80: ADC_L_GAIN_STATUS (Page 0: 0x0000000A)

Bit	Mode	Symbol	Description	Reset
6:0	R	adc_l_digital_gain_status	Contains the currently active ADC_L digital gain setting 0x00 = -83.25 dB 0x01 = -82.5 dB then continuing in 0.75 dB steps through 0x6F = 0 dB to... 0x7E = 11.25 dB 0x7F = 12 dB	0x0

Table 81: DAC_L_GAIN_STATUS (Page 0: 0x0000000C)

Bit	Mode	Symbol	Description	Reset
6:0	R	dac_l_digital_gain_status	Contains the currently active DAC_L digital gain setting 0x00 to 0x07 = mute 0x08 = -77.25 dB 0x09 = -76.5 dB then continuing in 0.75 dB steps through 0x6F = 0 dB to... 0x7E = 11.25 dB 0x7F = 12 dB	0x0

Table 82: DAC_R_GAIN_STATUS (Page 0: 0x0000000D)

Bit	Mode	Symbol	Description	Reset
6:0	R	dac_r_digital_gain_status	Contains the currently active DAC_R digital gain setting 0x00 to 0x07 = mute 0x08 = -77.25 dB 0x09 = -76.5 dB then continuing in 0.75 dB steps through 0x6F = 0 dB to... 0x7E = 11.25 dB 0x7F = 12 dB	0x0

Table 83: HP_L_GAIN_STATUS (Page 0: 0x0000000E)

Bit	Mode	Symbol	Description	Reset
5:0	R	hp_l_amp_gain_status	Contains the currently active HP_L_AMP gain setting 000000 = -57.0 dB 000001 = -56.0 dB 000010 = -55.0 dB then continuing in 1 dB steps to… 111001 = 0.0 dB 111111 = 6.0 dB	0x0

Table 84: HP_R_GAIN_STATUS (Page 0: 0x0000000F)

Bit	Mode	Symbol	Description	Reset
5:0	R	hp_r_amp_gain_status	Contains the currently active HP_R_AMP gain setting 000000 = -57.0 dB 000001 = -56.0 dB 000010 = -55.0 dB then continuing in 1 dB steps to… 111001 = 0.0 dB 111111 = 6.0 dB	0x0

Table 85: MIC_1_SELECT (Page 0: 0x00000010)

Bit	Mode	Symbol	Description	Reset
1:0	R/W	mic_1_amp_in_sel	MIC_1 input source control 00 = Differential 01 = MIC_1_P single-ended 10 = MIC_1_N single-ended 11 = Reserved	0x0

Table 86: REFERENCES (Page 0: 0x00000032)

Bit	Mode	Symbol	Description	Reset
4	R/W	vmid_fast_charge	VMID reference fast charge control 0 = low noise, slow charge mode 1 = high noise, fast charge mode	0x0

Bit	Mode	Symbol	Description	Reset
3	R/W	bias_en	Master bias control. Master bias is required for analog circuitry. 0 = Master bias disabled 1 = Master bias enabled	0x1

Table 87: MIXIN_L_SELECT (Page 0: 0x00000033)

Bit	Mode	Symbol	Description	Reset
0	R/W	mixin_l_mix_select	MIXIN_L mixer input control 0 = No input selected 1 = MIC_1 selected as input	0x0

Table 88: MIXIN_L_GAIN (Page 0: 0x00000034)

Bit	Mode	Symbol	Description	Reset
3:0	R/W	mixin_l_amp_gain	mixin_l_amp gain control 0000 = -4.5 dB 0001 = -3.0 dB 0010 = -1.5 dB 0011 = 0.0 dB then continuing in 1.5 dB steps to… 1110 = 16.5 dB 1111 = 18.0 dB	0x3

Table 89: ADC_L_GAIN (Page 0: 0x00000036)

Bit	Mode	Symbol	Description	Reset
6:0	R/W	adc_l_digital_gain	ADC_L digital gain control 00x0 = -83.25 dB 0x01 = -82.5 dB then continuing in 0.75 dB steps through 0x6F = 0 dB to... 0x7E = 11.25 dB 0x7F = 12 dB	0x6F

Table 90: MIC_1_GAIN (Page 0: 0x00000039)

Bit	Mode	Symbol	Description	Reset
2:0	R/W	mic_1_amp_gain	mic_1_amp gain control 000 = -6 dB 001 = 0 dB 010 = 6 dB 011 = 12 dB 100 = 18 dB 101 = 24 dB 110 = 30 dB 111 = 36 dB	0x1

Table 91: DAC_L_GAIN (Page 0: 0x00000045)

Bit	Mode	Symbol	Description	Reset
6:0	R/W	dac_l_digital_gain	DAC_L digital gain control 0x00 to 0x07 = mute 0x08 = -77.25 dB 0x09 = -76.5 dB then continuing in 0.75 dB steps through 0x6F = 0 dB to... 0x7E = 11.25 dB 0x7F = 12 dB	0x6F

Table 92: DAC_R_GAIN (Page 0: 0x00000046)

Bit	Mode	Symbol	Description	Reset
6:0	R/W	dac_r_digital_gain	DAC_R digital gain control 0x00 to 0x07 = mute 0x08 = -77.25 dB 0x09 = -76.5 dB then continuing in 0.75 dB steps through 0x6F = 0 dB to... 0x7E = 11.25 dB 0x7F = 12 dB	0x6F

Table 93: HP_L_GAIN (Page 0: 0x00000048)

Bit	Mode	Symbol	Description	Reset
5:0	R/W	hp_l_amp_gain	HP_L_AMP gain control 000000 = -57.0 dB 000001 = -56.0 dB 000010 = -55.0 dB then continuing in 1 dB steps through… 111001 = 0.0 dB to… 111111 = 6.0 dB	0x39

Table 94: HP_R_GAIN (Page 0: 0x00000049)

Bit	Mode	Symbol	Description	Reset
5:0	R/W	hp_r_amp_gain	HP_R_AMP gain control 000000 = -57.0 dB 000001 = -56.0 dB 000010 = -55.0 dB then continuing in 1 dB steps through… 111001 = 0.0 dB to… 111111 = 6.0 dB	0x39

Table 95: MIXOUT_L_SELECT (Page 0: 0x0000004B)

Bit	Mode	Symbol	Description	Reset
0	R/W	mixout_l_mix_select	Output left mixer channel selection 0 = No channel selected 1 = DAC_L selected as output	0x0

Table 96: MIXOUT_R_SELECT (Page 0: 0x0000004C)

Bit	Mode	Symbol	Description	Reset
0	R/W	mixout_r_mix_select	Ouput right mixer channel selection 0 = No channel selected 1 = DAC_R selected as output	0x0

Table 97: MICBIAS_CTRL (Page 0: 0x00000062)

Bit	Mode	Symbol	Description	Reset
3	R/W	micbias1_en	Microphone Bias 1 control 0 = Micbias1 disabled 1 = Micbias1 enabled	0x0
2:0	R/W	micbias1_level	Microphone Bias 1 level control 000 = 1.6 V 001 = 1.8 V 010 = 2.0 V 011 = 2.2 V 100 = 2.4 V 101 = 2.6 V 110 = 2.8 V 111 = 2.9 V This must only be modified while micbias_1 is disabled (micbias1_en = 0)	0x3

Table 98: MIC_1_CTRL (Page 0: 0x00000063)

Bit	Mode	Symbol	Description	Reset
7	R/W	mic_1_amp_en	MIC_1 amplifier control 0 = MIC_1 disabled 1 = MIC_1 enabled	0x0
6	R/W	mic_1_amp_mute_en	MIC_1 amplifier mute control 0 = MIC_1 unmuted 1 = MIC_1 muted	0x1
5	-	mic_1_amp_ramp_en	MIC_1 amplifier gain ramping control 0 = Gain changes are instant 1 = Gain changes are ramped to the new level	0x0

Table 99: MIXIN_L_CTRL (Page 0: 0x00000065)

Bit	Mode	Symbol	Description	Reset
7	R/W	mixin_l_amp_en	MIXIN_L amplifier control 0 = MIXIN_L disabled 1 = MIXIN_L enabled	0x0
6	R/W	mixin_l_amp_mute_en	MIXIN_L amplifier mute control 0 = MIXIN_L unmuted 1 = MIXIN_L muted	0x1

Bit	Mode	Symbol	Description	Reset
5	R/W	mixin_l_amp_ramp_en	MIXIN_L amplifier gain ramping control 0 = Gain changes are instant 1 = Gain changes are ramped to the new level This setting overrides zero crossing	0x0
4	R/W	mixin_l_amp_zc_en	MIXIN_L amplifier zero cross control 0 = Gain changes are instant 1 = Gain changes are performed when the signal crosses zero If no zero-crossing is detected within the timeout period of approximately 100 ms, the update is applied unconditionally	0x0
3	R/W	mixin_l_mix_en	MIXIN_L mixer control. When this mixer is disabled, all inputs are deselected. 0 = Mixer disabled 1 = Mixer enabled	0x0

Table 100: ADC_L_CTRL (Page 0: 0x00000067)

Bit	Mode	Symbol	Description	Reset
7	R/W	adc_l_en	ADC_L control 0 = ADC_L disabled 1 = ADC_L enabled	0x0
6	R/W	adc_l_mute_en	ADC_L mute control 0 = ADC_L unmuted 1 = ADC_L muted	0x1
5	R/W	adc_l_ramp_en	ADC_L digital gain ramping control 0 = Gain changes are instant 1 = Gain changes are ramped to the new level	0x0

Table 101: DAC_L_CTRL (Page 0: 0x00000069)

Bit	Mode	Symbol	Description	Reset
7	R/W	dac_l_en	DAC_L control 0 = DAC_L disabled 1 = DAC_L enabled	0x0
6	R/W	dac_l_mute_en	DAC_L mute control 0 = DAC_L unmuted 1 = DAC_L muted	0x1

Bit	Mode	Symbol	Description	Reset
5	R/W	dac_l_ramp_en	DAC_L digital gain ramping control 0 = Gain changes are instant 1 = Gain changes are ramped to the new level	0x0

Table 102: DAC_R_CTRL (Page 0: 0x0000006A)

Bit	Mode	Symbol	Description	Reset
7	R/W	dac_r_en	DAC_R control 0 = DAC_R disabled 1 = DAC_R enabled	0x0
6	R/W	dac_r_mute_en	DAC_R mute control 0 = DAC_R unmuted 1 = DAC_R muted	0x1
5	R/W	dac_r_ramp_en	DAC_R digital gain ramping control 0 = Gain changes are instant 1 = Gain changes are ramped to the new level	0x0

Table 103: HP_L_CTRL (Page 0: 0x0000006B)

Bit	Mode	Symbol	Description	Reset
7	R/W	hp_l_amp_en	HP_L_AMP amplifier control 0 = HP_L_AMP disabled 1 = HP_L_AMP enabled	0x0
6	R/W	hp_l_amp_mute_en	HP_L_AMP amplifier mute control 0 = HP_L_AMP unmuted 1 = HP_L_AMP muted	0x1
5	R/W	hp_l_amp_ramp_en	HP_L_AMP amplifier gain ramping control 0 = Gain changes are instant 1 = Gain changes are ramped to the new level This setting overrides zero crossing	0x0
4	R/W	hp_l_amp_zc_en	HP_L_AMP amplifier zero cross control 0 = Gain changes are instant 1 = Gain changes are performed when the signal crosses zero If no zero-crossing is detected within the timeout period of approximately 100 ms, the update is applied unconditionally	0x0

Bit	Mode	Symbol	Description	Reset
3	R/W	hp_l_amp_oe	HP_L_AMP amplifier output control 0 = Output is high-impedance 1 = Output is driven	0x0
2	R/W	hp_l_amp_min_gain_en	HP_L_AMP amplifier minimum gain control. 0 = Normal gain operation 1 = Minimum gain only. HP_L amplifier is held at minimum gain regardless of other gain settings	0x0

Table 104: HP_R_CTRL (Page 0: 0x0000006C)

Bit	Mode	Symbol	Description	Reset
7	R/W	hp_r_amp_en	HP_R_AMP amplifier control 0 = HP_R_AMP disabled 1 = HP_R_AMP enabled	0x0
6	R/W	hp_r_amp_mute_en	HP_R_AMP amplifier mute control 0 = HP_R_AMP unmuted 1 = HP_R_AMP muted	0x1
5	R/W	hp_r_amp_ramp_en	HP_R_AMP amplifier gain ramping control 0 = Gain changes are instant 1 = Gain changes are ramped to the new level This setting overrides zero crossing	0x0
4	R/W	hp_r_amp_zc_en	HP_R_AMP amplifier zero cross control 0 = Gain changes are instant 1 = Gain changes are performed when the signal crosses zero If no zero-crossing is detected within the timeout period of approximately 100 ms, the update is applied unconditionally	0x0
3	R/W	hp_r_amp_oe	HP_R_AMP amplifier output control 0 = Output is high-impedance 1 = Output is driven	0x0
2	R/W	hp_r_amp_min_gain_en	HP_R_AMP amplifier minimum gain control. 0 = Normal gain operation 1 = Minimum gain only. HP_R_AMP is held at minimum gain regardless of other gain settings	0x0

Table 105: MIXOUT_L_CTRL (Page 0: 0x0000006E)

Bit	Mode	Symbol	Description	Reset
7	R/W	mixout_l_amp_en	MIXIN_L amplifier control 0 = Mixer disabled 1 = Mixer enabled	0x0

Table 106: MIXOUT_R_CTRL (Page 0: 0x0000006F)

Bit	Mode	Symbol	Description	Reset
7	R/W	mixout_r_amp_en	MIXIN_R amplifier control 0 = Mixer disabled 1 = Mixer enabled	0x0

Table 107: IO_CTRL (Page 0: 0x00000091)

Bit	Mode	Symbol	Description	Reset
0	R/W	io_voltage_level	Digital I/O voltage range control 0 = 2.5 V to 3.6 V 1 = 1.2 V to 2.8 V	0x0

Table 108: Register map charge_pump_cad_00 page 0

Address Name	7	6	5	4	3	2	1	0
Register Page 0								
0x00000047 CP_CTRL	cp_en	Reserved	cp_mchange		Reserved			
0x00000095 CP_VOL_THRESHOLD1	Reserved		cp_thresh_vdd2					

Table 109: CP_CTRL (Page 0: 0x00000047)

Bit	Mode	Symbol	Description	Reset
7	R/W	cp_en	Chargepump control 0 = Chargepump disabled 1 = Chargepump enabled	0x0

Bit	Mode	Symbol	Description	Reset
5:4	R/W	cp_mchange	Charge pump tracking mode control 00 = Reserved 01 = Voltage level is controlled by the largest output volume level 10 = Voltage level is controlled by the DAC volume level 11 = Voltage level is controlled by the signal magnitude	0x2

Table 110: CP_VOL_THRESHOLD1 (Page 0: 0x00000095)

Bit	Mode	Symbol	Description	Reset
5:0	R/W	cp_thresh_vdd2	Threshold at and below which the charge pump can use the CPVDD/2 rail. This setting is only effective when cp_mchange = 10 or cp_mchange = 11. It is ignored for cp_mchange settings of 00 and 01	0xE

Table 111: Register map cif_i2c_addr_cad_00 page 0

Address Name	7	6	5	4	3	2	1	0
Register Page 0								
0x0000001B CIF_I2C_ADDR_CFG	Reserved						cif_i2c_addr_cfg	

Table 112: CIF_I2C_ADDR_CFG (Page 0: 0x0000001B)

Bit	Mode	Symbol	Description	Reset
1:0	R/W	cif_i2c_addr_cfg	I2C address [1:0] configuration This allows multiple DA7219 devices to reside on the same bus by allowing the least significant two bits to be written to a specific value. The I2C clock must be externally controlled while writing this register to ensure that only the target DA7219 device's I2C address is modified.	0x2

Table 113: Register map common1_cad_00 page 0

Address Name	7	6	5	4	3	2	1	0
Register Page 0								
0x00000012 CIF_TIMEOUT_CTRL	Reserved							i2c_timeout_en
0x00000013 CIF_CTRL	cif_reg_soft_reset	Reserved						cif_i2c_write_mode
0x00000016 SR_24_48	Reserved							sr_24_48
0x00000017 SR	Reserved				sr			
0x00000092 GAIN_RAMP_CTRL	Reserved						gain_ramp_rate	
0x00000094 PC_COUNT	Reserved						pc_resync_auto	pc_freerun

Table 114: CIF_TIMEOUT_CTRL (Page 0: 0x00000012)

Bit	Mode	Symbol	Description	Reset
0	R/W	i2c_timeout_en	I2C (2-wire) timeout control. The timeout period is approximately 43.9 ms. 0 = Timeout disabled 1 = Timeout enabled	0x0

Table 115: CIF_CTRL (Page 0: 0x00000013)

Bit	Mode	Symbol	Description	Reset
7	R/W	cif_reg_soft_reset	Software reset which returns all the registers back to their default values. Writing to this bit causes all the registers to reset. 0 = No reset 1 = Reset all registers to their default values	0x0
0	R/W	cif_i2c_write_mode	I2C (2-wire) interface write mode control 0 = Page mode. The register address is autoincremented after the first write. 1 = Repeat mode. The register address and data are sent for each write.	0x0

Table 116: SR_24_48 (Page 0: 0x00000016)

Bit	Mode	Symbol	Description	Reset
0	R/W	sr_24_48	24_48_mode control. Setting this bit runs the ADC and the DAC paths at different speeds. 0 = The ADC path and the DAC path both run at the same speed. This speed is determined by the setting of the sr bit in this register 1 = The ADC path runs at 24 kHz, and the DAC path and the rest of the system run at 48 kHz To use this mode, the system sample rate sr must be set to 48 kHz. Therefore the I2S will also run at 48 kHz and the 24 kHz ADC output will be double sampled.	0x0

Table 117: SR (Page 0: 0x00000017)

Bit	Mode	Symbol	Description	Reset
3:0	R/W	sr	Sample rate control: 0001 = 8.000 kHz 0010 = 11.025 kHz 0011 = 12.000 kHz 0101 = 16.000 kHz 0110 = 22.050 kHz 0111 = 24.000 kHz 1001 = 32.000 kHz 1010 = 44.100 kHz 1011 = 48.000 kHz 1110 = 88.200 kHz 1111 = 96.000 kHz	0xA

Table 118: GAIN_RAMP_CTRL (Page 0: 0x00000092)

Bit	Mode	Symbol	Description	Reset
1:0	R/W	gain_ramp_rate	Controls the speed of the gain ramping when ramping is activated 0 = nominal rate * 8 1 = nominal rate 2 = nominal rate / 8 3 = nominal rate / 16 (slowest) The nominal rate (excluding headphone circuits) = 0.88 ms/dB. The nominal rate for the headphone circuits is = 1.3 ms/dB.	0x0

Table 119: PC_COUNT (Page 0: 0x00000094)

Bit	Mode	Symbol	Description	Reset
1	R/W	pc_resync_auto	Program Counter resynchronisation control 0 = No resynchronisation. If the DAI drifts with respect to the system clocks, either a sample is skipped or it is double-sampled 1 = Automatic resynchronisation if the DAI drifts with respect to the system clock	0x1
0	R/W	pc_freerun	Controls the filter operation when the DAI is not enabled or when no DAI clocks are available on the ADC to DAC processing path 0 = Filters are synchronised to the DAI 1 = Filters are free running	0x0

Table 120: Register map common2_cad_00 page 0

Address Name	7	6	5	4	3	2	1	0
Register Page 0								
0x00000081 CHIP_ID1	chip_id1							
0x00000082 CHIP_ID2	chip_id2							
0x00000083 CHIP_REVISION	chip_major				chip_minor			

Table 121: CHIP_ID1 (Page 0: 0x00000081)

Bit	Mode	Symbol	Description	Reset
7:0	R	chip_id1	First two digits of the four-digit Chip ID The last two numbers of the Chip ID are held in chip_id2	0x23

Table 122: CHIP_ID2 (Page 0: 0x00000082)

Bit	Mode	Symbol	Description	Reset
7:0	R	chip_id2	Last two digits of the four-digit Chip ID The first two numbers of the Chip ID are held in chip_id1	0x93

Table 123: CHIP_REVISION (Page 0: 0x00000083)

Bit	Mode	Symbol	Description	Reset
7:4	R	chip_major	Chip major revision	0x0
3:0	R	chip_minor	Chip minor revision	0x2

Table 124: Register map dac_filters_cad_00 page 0

Address Name	7	6	5	4	3	2	1	0
Register Page 0								
0x00000040 DAC_FILTERS5	dac_softmute_en	dac_softmute_rate			Reserved			
0x00000041 DAC_FILTERS2	dac_eq_band2				dac_eq_band1			
0x00000042 DAC_FILTERS3	dac_eq_band4				dac_eq_band3			
0x00000043 DAC_FILTERS4	dac_eq_en	Reserved			dac_eq_band5			
0x00000044 DAC_FILTERS1	dac_hpf_en	Reserved	dac_audio_hpf_corner		dac_voice_en	dac_voice_hpf_corner		

Table 125: DAC_FILTERS5 (Page 0: 0x00000040)

Bit	Mode	Symbol	Description	Reset
7	R/W	dac_softmute_en	DAC softmute control. When this bit is set, both channels are soft-muted. 0 = Soft-mute disabled 1 = Soft-mute enabled	0x0
6:4	R/W	dac_softmute_rate	Softmute gain update control 000 = 1 sample per 0.1875 dB 001 = 2 samples per 0.1875 dB 010 = 4 samples per 0.1875 dB 011 = 8 samples per 0.1875 dB 100 = 16 samples per 0.1875 dB 101 = 32 samples per 0.1875 dB 110 = 64 samples per 0.1875 dB 111 = Reserved	0x0

Table 126: DAC_FILTERS2 (Page 0: 0x00000041)

Bit	Mode	Symbol	Description	Reset
7:4	R/W	dac_eq_band2	Gain control of Band 2 in the 5-band EQ 0000 = -10.5 dB 0001 = -9.0 dB 0010 = -7.5 dB Continuing in 1.5 dB steps through 0111 = 0 dB to… 1110 = 10.5 dB 1111 = 12 dB	0x8
3:0	R/W	dac_eq_band1	Gain control of Band 1 in the 5-band EQ 0000 = -10.5 dB 0001 = -9.0 dB 0010 = -7.5 dB Continuing in 1.5 dB steps through 0111 = 0 dB to… 1110 = 10.5 dB 1111 = 12 dB	0x8

Table 127: DAC_FILTERS3 (Page 0: 0x00000042)

Bit	Mode	Symbol	Description	Reset
7:4	R/W	dac_eq_band4	Gain control of Band 4 in the 5-band EQ 0000 = -10.5 dB in 1.5 dB steps 0001 = -9.0 dB 0010 = -7.5 dB Continuing in 1.5 dB steps through 0111 = 0 dB to… 1110 = 10.5 dB 1111 = 12 dB	0x8
3:0	R/W	dac_eq_band3	Gain control of Band 3 in the 5-band EQ 0000 = -10.5 dB 0001 = -9.0 dB 0010 = -7.5 dB Continuing in 1.5 dB steps through 0111 = 0 dB to… 1110 = 10.5 dB 1111 = 12 dB	0x8

Table 128: DAC_FILTERS4 (Page 0: 0x00000043)

Bit	Mode	Symbol	Description	Reset
7	R/W	dac_eq_en	DAC 5-band EQ control 0 = Equaliser disabled 1 = Equaliser enabled	0x0
3:0	R/W	dac_eq_band5	Gain control of Band 5 in the 5-band EQ 0000 = -10.5 dB 0001 = -9.0 dB 0010 = -7.5 dB Continuing in 1.5 dB steps through 0111 = 0 dB to… 1110 = 10.5 dB 1111 = 12 dB	0x8

Table 129: DAC_FILTERS1 (Page 0: 0x00000044)

Bit	Mode	Symbol	Description	Reset
7	R/W	dac_hpf_en	DAC High Pass Filter control 0 = High Pass Filter disabled 1 = High Pass Filter enabled	0x1
5:4	R/W	dac_audio_hpf_corner	High Pass Filter 3 dB cutoff control. At 48 kHz, the 3 dB cutoff point is at: 00 = 2 Hz 01 = 4 Hz 10 = 8 Hz 11 = 16 Hz For other sample rates, the corner cutoff point scales proportionately.	0x0
3	R/W	dac_voice_en	DAC Voice Filter control : For 8/11.025/12/16 kHz sample rates and for best performance should always be enabled when running at one these rates. 0 = DAC Voice Filter disabled 1 = DAC Voice Filter enabled This DAC Voice Filter control overrides the 5-band EQ setting in dac_eq_en	0x0

Bit	Mode	Symbol	Description	Reset
2:0	R/W	dac_voice_hpf_corner	Voice Filter 3 dB cutoff control. At 8 kHz, the 3 dB cutoff point is at: 000 = 2.5 Hz 001 = 25 Hz, 010 = 50 Hz 011 = 100 Hz 100 = 150 Hz 101 = 200 Hz 110 = 275 Hz 111 = 363 Hz	0x0

Table 130: Register map dac_ng_cad_00 page 0

Address Name	7	6	5	4	3	2	1	0
Register Page 0								
0x000000AF DAC_NG_SETUP_TIME	Reserved				dac_ng_rampdn_rate	dac_ng_rampup_rate	dac_ng_setup_time	
0x000000B0 DAC_NG_OFF_THRESH	Reserved					dac_ng_off_threshold		
0x000000B1 DAC_NG_ON_THRESH	Reserved					dac_ng_on_threshold		
0x000000B2 DAC_NG_CTRL	dac_ng_en	Reserved						

Table 131: DAC_NG_SETUP_TIME (Page 0: 0x000000AF)

Bit	Mode	Symbol	Description	Reset
3	R/W	dac_ng_rampdn_rate	DAC Noise Gate ramp down control 0 = 0.88 ms/dB 1 = 14.08 ms/dB	0x0
2	R/W	dac_ng_rampup_rate	DAC Noise Gate ramp up control 0 = 0.22 ms/dB 1 = 0.0138 ms/dB	0x0
1:0	R/W	dac_ng_setup_time	Noise Gate timing control This specifies the number of samples for which the largest signal through the DACs must be above (or below) dac_ng_off _threshold (or dac_ng_on_threshold) for the Noise Gate to unmute (or mute) the data 00 = 256 samples 01 = 512 samples 10 = 1024 samples 11 = 2048 samples	0x0

Table 132: DAC_NG_OFF_THRESH (Page 0: 0x000000B0)

Bit	Mode	Symbol	Description	Reset
2:0	R/W	dac_ng_off_threshold	Threshold above which the Noise Gate is deactivated. If the signal rises above this level, the Noise Gate is deactivated. 000 = -102 dB 001 = -96 dB 010 = -90 dB 011 = -84 dB 100 = -78 dB 101 = -72 dB 110 = -66 dB 111 = -60 dB	0x0

Table 133: DAC_NG_ON_THRESH (Page 0: 0x000000B1)

Bit	Mode	Symbol	Description	Reset
2:0	R/W	dac_ng_on_threshold	Threshold below which the Noise Gate is dactivated. If the signal drops below this level for dac_ng_setup_time samples, the Noise Gate is activated. 000 = -102 dB 001 = -96 dB 010 = -90 dB 011 = -84 dB 100 = -78 dB 101 = -72 dB 110 = -66 dB 111 = -60 dB	0x0

Table 134: DAC_NG_CTRL (Page 0: 0x000000B2)

Bit	Mode	Symbol	Description	Reset
7	R/W	dac_ng_en	DAC Noise Gate control 0 = Noise Gate is disabled 1 = Noise Gate is enabled	0x0

Table 135: Register map dai_cad_00 page 0

Address Name	7	6	5	4	3	2	1	0
Register Page 0								
0x0000002B DAI_CLK_MODE	dai_clk_en	Reserved		dai_wclk_tri_state	dai_wclk_pol	dai_clk_pol	dai_bclks_per_wclk	
0x0000002C DAI_CTRL	dai_en	Reserved	dai_ch_num		dai_word_length		dai_format	
0x0000002D DAI_TDM_CTRL	dai_tdm_mode_en	dai_oe	Reserved				dai_tdm_ch_en	
0x00000030 DAI_OFFSET_LOWER	dai_offset_lower							
0x00000031 DAI_OFFSET_UPPER	Reserved					dai_offset_upper		

Table 136: DAI_CLK_MODE (Page 0: 0x0000002B)

Bit	Mode	Symbol	Description	Reset
7	R/W	dai_clk_en	DAI Master mode control 0 = Slave mode (BCLK/WCLK inputs) 1 = Master mode (BCLK/WCLK outputs)	0x0
4	R/W	dai_wclk_tri_state	WLCK tri-state control 0 = WCLK state is set by dai_clk_en. WCLK is set as output in master mode, and as input in slave mode 1 = WCLK forced as an input	0x0
3	R/W	dai_wclk_pol	DAI word clock polarity control 0 = Normal polarity 1 = Inverted polarity	0x0
2	R/W	dai_clk_pol	DAI bit clock polarity control 0 = Normal polarity 1 = Inverted polarity	0x0
1:0	R/W	dai_bclks_per_wclk	Number of BCLKs per WCLK period when in DAI Master mode 00 = 32 BCLKS per WCLK 01 = 64 BCLKS per WCLK 10 = 128 BCLKS per WCLK 11 = 256 BCLKS per WCLK	0x1

Table 137: DAI_CTRL (Page 0: 0x0000002C)

Bit	Mode	Symbol	Description	Reset
7	R/W	dai_en	DAI control 0 = DAI disabled. No data is transferred. 1 = DAI enabled. Input and output data streams are transferred	0x0
5:4	R/W	dai_ch_num	Channel control 00 = No channels are enabled 01 = Left channel is enabled 10 = Left and right channels are enabled 11 = Reserved	0x2
3:2	R/W	dai_word_length	DAI data word length control 0 = 16 bits per channel 1 = 20 bits per channel 2 = 24 bits per channel 3 = 32 bits per channel	0x2
1:0	R/W	dai_format	DAI data format 00 = I2S mode 01 = Left justified mode 10 = Right justified mode 11 = DSP mode	0x0

Table 138: DAI_TDM_CTRL (Page 0: 0x0000002D)

Bit	Mode	Symbol	Description	Reset
7	R/W	dai_tdm_mode_en	DAI TDM mode control. In TDM mode, the output is high impedence when not actively driving data as this allows other devices to share the DATOUT line. 0 = DAI normal mode 1 = DAI TDM mode	0x0
6	R/W	dai_oe	DAI output control 0 = DAI DATOUT pin is high impedence 1 = DAI DATOUT pin is driven when required	0x1
1:0	R/W	dai_tdm_ch_en	DAI TDM channel control. Bit 0 = Left channel; Bit 1: Riight channel. For each bit, 0 = Disabled; 1 = Enabled. 00 = Left channel and right channel both disabled 01 = Left channel enabled, right channel disabled 10 = Left channel disabled, right channel enabled 11 = Left channel and right channel both enabled	0x0

Table 139: DAI_OFFSET_LOWER (Page 0: 0x00000030)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	dai_offset_lower	DAI data offset with respect to WCLK measured in BCLK periods. The total offset is determined by an 11-bit binary number formed by a combination of this register (dai_offset_lower) and dai_offset_upper. With the maximum BCLK frequency of 6 MHz, the maximum number of BCLK periods is 768. The maximum DAI offset value is therefore 767 (0x2FF), represented by dai_offset_lower = 1111 1111, and dai_offset_upper = 010. 0x000 = No offset relative to the normal formatting 0x001 = One BCLK period offset relative to the normal formatting 0x002 = Two BCLK periods offset relative to the normal formatting 0xn = n BCLK periods offset relative to the normal formatting (max = 0x2FF)	0x0

Table 140: DAI_OFFSET_UPPER (Page 0: 0x00000031)

Bit	Mode	Symbol	Description	Reset
2:0	R/W	dai_offset_upper	DAI data offset with respect to WCLK measured in BCLK periods. The total offset is determined by an 11-bit binary number formed by a combination of dai_offset_lower and this register (dai_offset_upper). With the maximum BCLK frequency of 6 MHz, the maximum number of BCLK periods is 768. The maximum DAI offset value is therefore 767 (0x2FF), represented by dai_offset_lower = 1111 1111, and dai_offset_upper = 010. 0x000 = No offset relative to the normal formatting 0x001 = One BCLK period offset relative to the normal formatting 0x002 = Two BCLK periods offset relative to the normal formatting 0xn = n BCLK periods offset relative to the normal formatting (max = 0x2FF)	0x0

Table 141: Register map pll_cad_00 page 0

Address Name	7	6	5	4	3	2	1	0
Register Page 0								
0x00000020 PLL_CTRL	pll_mode		pll_mclk_sqr_en	pll_indiv			Reserved	

Address Name	7	6	5	4	3	2	1	0
Register Page 0								
0x00000022 PLL_FRAC_TOP	Reserved			pll_fbdiv_frac_top				
0x00000023 PLL_FRAC_BOT	pll_fbdiv_frac_bot							
0x00000024 PLL_INTEGER	Reserved	pll_fbdiv_integer						
0x00000025 PLL_SRM_STS	pll_srm_status				Reserved			

Table 142: PLL_CTRL (Page 0: 0x00000020)

Bit	Mode	Symbol	Description	Reset
7:6	R/W	pll_mode	PLL mode control 00 = Bypass mode. The PLL is disabled, and the system clock is MCLK (after input divider) 01 = Normal mode.The PLL is enabled, and the system clock is a fixed multiple of MCLK 10 = SRM. The PLL is enabled, and the system clock tracks WCLK 11 = Reserved	0x0
5	R/W	pll_mclk_sqr_en	PLL clock squarer control. 0 = Clock squarer is disabled 1 = Clock squarer is enabled	0x0
4:2	R/W	pll_indiv	PLL reference input clock (MCLK) control 0 = 2 to 4.5 MHz 1 = 4.5 to 9 MHz 2 = 9 to 18 MHz 3 = 18 to 36 MHz 4 = 36+ MHz	0x4

Table 143: PLL_FRAC_TOP (Page 0: 0x00000022)

Bit	Mode	Symbol	Description	Reset
4:0	R/W	pll_fbdiv_frac_top	PLL fractional division value (top bits). The full PLL fractional division value is a concatenation of these bits (MSB) and PLL_FBDIV_FRAC_BOT (LSB). The value in this register does not take effect until pll_fbdiv_integer is written.	0x0

Table 144: PLL_FRAC_BOT (Page 0: 0x00000023)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	pll_fbdiv_frac_bot	PLL fractional division value (bottom bits). The full PLL fractional division value is a concatenation of PLL_FBDIV_FRAC_TOP (MSB) and these bits (LSB). The value in this register does not take effect until pll_fbdiv_integer is written.	0x0

Table 145: PLL_INTEGER (Page 0: 0x00000024)

Bit	Mode	Symbol	Description	Reset
6:0	R/W	pll_fbdiv_integer	PLL integer division value. Writing this register causes the entire pll_fbdiv value (PLL_INTEGER, PLL_FRAC_TOP, PLL_FRAC_BOT) to be updated.	0x20

Table 146: PLL_SRM_STS (Page 0: 0x00000025)

Bit	Mode	Symbol	Description	Reset
7:4	R	pll_srm_status	PLL/SRM status (user mode). Within this four-bit register field, Bit position [3] = SRM lock Bit position [2] = PLL/SRM active Bit position [1] = PLL lock Bit position [0] = MCLK status (1=valid MCLK detected, subject to minimum detection frequency of approximately 1 MHz) For each bit position, 0 = Inactive or invalid 1 = Active or valid	0x1

Table 147: Register map router_cad_00 page 0

Address Name	7	6	5	4	3	2	1	0
Register Page 0								
0x0000002A DIG_ROUTING_DAI	Reserved			dai_r_src		Reserved		dai_l_src
0x0000002E DIG_ROUTING_DAC	dac_r_mono	Reserved		dac_r_src	dac_l_mono	Reserved		dac_l_src
0x00000099 DIG_CTRL	dac_r_inv	Reserved			dac_l_inv	Reserved		

Table 148: DIG_ROUTING_DAI (Page 0: 0x0000002A)

Bit	Mode	Symbol	Description	Reset
5:4	R/W	dai_r_src	Data selection for the DAI right output stream 00 = ADC left 01 = Tone generator 10 = DAI input left data / DAI mono mix 11 = DAI input right data / DAI mono mix	0x1
1:0	R/W	dai_l_src	Data selection for the DAI left output stream 00 = ADC left 01 = Tone generator 10 = DAI input left data / DAI mono mix 11 = DAI input right data / DAI mono mix	0x0

Table 149: DIG_ROUTING_DAC (Page 0: 0x0000002E)

Bit	Mode	Symbol	Description	Reset
7	R/W	dac_r_mono	Mono-mix control for the DAI right input stream 0 = No mono-mix 1 = The DAI right input stream is replaced with a mono mix of left and right	0x0
5:4	R/W	dac_r_src	Data selection to the DAC_R path 00 = ADC left output 01 = Tone generator 10 = DAI input left / dai mono mix 11 = DAI input right / dai mono mix	0x3
3	R/W	dac_l_mono	Mono-mix control for the DAI left input stream 0 = No mono-mix 1 = The DAI left input stream is replaced with a mono mix of left and right	0x0
1:0	R/W	dac_l_src	Data selection to the DAC_L path 00 = ADC left output 01 = Tone generator 10 = DAI input left / dai mono mix 11 = DAI input right / dai mono mix	0x2

Table 150: DIG_CTRL (Page 0: 0x00000099)

Bit	Mode	Symbol	Description	Reset
7	R/W	dac_r_inv	DAC right input stream invertion control 0 = No inversion of the right input strem 1 = The right input stream is inverted	0x0
3	R/W	dac_l_inv	DAC left input stream invertion control 0 = No inversion of the left input stream 1 = The left input stream is inverted	0x0

Table 151: Register map sidetone_cad_00 page 0

Address Name	7	6	5	4	3	2	1	0
Register Page 0								
0x0000003A SIDETONE_CTRL	sidetone_en	sidetone_mute_en	Reserved					
0x0000003B SIDETONE_GAIN	Reserved				sidetone_gain			
0x0000003C DROUTING_ST_OUTFILT_1L	Reserved					outfilt_st_1l_src		
0x0000003D DROUTING_ST_OUTFILT_1R	Reserved					outfilt_st_1r_src		

Table 152: SIDETONE_CTRL (Page 0: 0x0000003A)

Bit	Mode	Symbol	Description	Reset
7	R/W	sidetone_en	Sidetone path control 0 = Sidetone path disabled 1 = Sidetone path enabled	0x0
6	R/W	sidetone_mute_en	SideTone mute control 0 = Sidetone mute disabled 1 = Sidetone mute enabled	0x1

Table 153: SIDETONE_GAIN (Page 0: 0x0000003B)

Bit	Mode	Symbol	Description	Reset
3:0	R/W	sidetone_gain	Sidetone gain control 0000 = -42 dB 0001 = -39 dB 0010 = -36 dB Continuing in 3 dB steps to… 1101 = -3dB 1110 = 0dB 1111 = Reserved	0xE

Table 154: DROUTING_ST_OUTFILT_1L (Page 0: 0x0000003C)

Bit	Mode	Symbol	Description	Reset
2:0	R/W	outfilt_st_1l_src	Data selection for the output filter 1 left output stream bit 0 = Output filter 1L bit 1 = Output filter 1R bit 2 = Sidetone For each bit position/output stream, 0 = disabled and 1 = enabled	0x1

Table 155: DROUTING_ST_OUTFILT_1R (Page 0: 0x0000003D)

Bit	Mode	Symbol	Description	Reset
2:0	R/W	outfilt_st_1r_src	Data selection for the output filter 1 right output stream bit 0 = Output filter 1L bit 1 = Output filter 1R bit 2 = Sidetone For each bit position/output stream, 0 = disabled and 1 = enabled	0x2

Table 156: Register map system_active_cad_00 page 0

Address Name	7	6	5	4	3	2	1	0
Register Page 0								
0x000000FD SYSTEM_ACTIVE	Reserved							system_active

Table 157: SYSTEM_ACTIVE (Page 0: 0x000000FD)

Bit	Mode	Symbol	Description	Reset
0	R/W	system_active	System Standby mode 0 = Standby mode 1 = Active mode	0x0

Table 158: Register map system_controller_cad_00 page 0

Address Name	7	6	5	4	3	2	1	0
Register Page 0								
0x00000050 SYSTEM_MODES_INPUT	adc_mode							mode_submit
0x00000051 SYSTEM_MODES_OUTPUT	dac_mode							mode_submit
0x000000E0 SYSTEM_STATUS	Reserved						sc2_busy	sc1_busy

Table 159: SYSTEM_MODES_INPUT (Page 0: 0x00000050)

Bit	Mode	Symbol	Description	Reset
7:1	R/W	adc_mode	preconfigured system modes (input side): [1] = reserved [2] = MIC [3] = reserved [4] = MIXIN [5] = reserved [6] = ADC [7] = reserved	0x0
0	R/W	mode_submit	Causes both the adc_mode and dac_mode to become active	0x0

Table 160: SYSTEM_MODES_OUTPUT (Page 0: 0x00000051)

Bit	Mode	Symbol	Description	Reset
7:1	R/W	dac_mode	preconfigured system modes (output side): [1] = reserved [2] = reserved [3] = reserved [4] = HP_L [5] = HP_R [6] = DAC_L [7] = DAC_R	0x0
0	-	mode_submit	Causes both the adc_mode and dac_mode to become active	0x0

Table 161: SYSTEM_STATUS (Page 0: 0x000000E0)

Bit	Mode	Symbol	Description	Reset
1	R	sc2_busy	Indicates the current status of the system mode controller 0 = complete 1 = busy	0x0
0	R	sc1_busy	Indicates the current status of the system controller 0 = complete 1 = busy	0x0

Table 162: Register map tone_gen_cad_00 page 0

Address Name	7	6	5	4	3	2	1	0
Register Page 0								
0x000000B4 TONE_GEN_CFG1	start_stopn	Reserved		dtmf_en	dtmf_reg			
0x000000B5 TONE_GEN_CFG2	tone_gen_gain				Reserved		swg_sel	
0x000000B6 TONE_GEN_CYCLES	Reserved					beep_cycles		
0x000000B7 TONE_GEN_FREQ1_L	freq1_l							
0x000000B8 TONE_GEN_FREQ1_U	freq1_u							
0x000000B9 TONE_GEN_FREQ2_L	freq2_l							
0x000000BA TONE_GEN_FREQ2_U	freq2_u							
0x000000BB TONE_GEN_ON_PER	Reserved		beep_on_per					
0x000000BC TONE_GEN_OFF_PER	Reserved		beep_off_per					

Table 163: TONE_GEN_CFG1 (Page 0: 0x000000B4)

Bit	Mode	Symbol	Description	Reset
7	R/W	start_stopn	Tone Generator stop-start control. Setting this bit = 1 starts the Tone Generator for the number of beeps defined by beep_cycles. Once complete, the bit is automatically cleared. If beep_cycles = 111 (continuous), then this bit must be cleared manually 0 = Tone Generator disabled 1 = Tone Generator enabled	0x0
4	R/W	dtmf_en	DTMF control 0 = DTMF is disabled. The Tone Generator uses values in the registers freq1 and freq2 to generate sine wave(s) 1 = DTMF is enabled. The Tone Generator uses values from the register dtmf_reg to generate sine-waves	0x0
3:0	R/W	dtmf_reg	The DTMF key pad values 0 to 15 0000 = 0 0001 = 1 0010 = 2 0011 = 3 0100 = 4 0101 = 5 0110 = 6 0111 = 7 1000 = 8 1001 = 9 1010 = A 1011 = B 1100 = C 1101 = D 1110 = * 1111 = #	0x0

Table 164: TONE_GEN_CFG2 (Page 0: 0x000000B5)

Bit	Mode	Symbol	Description	Reset
7:4	R/W	tone_gen_gain	Tone Generator gain control 0000 = 0 dB 0001 = -2.5 dB 0010 = -6 dB Continuing in 2.5/3.5 dB steps to… 1110 = -42 dB 1111 = -44.5 dB	0x0

Bit	Mode	Symbol	Description	Reset
1:0	R/W	swg_sel	Sine wave selection control 00 = Sum of both Sine Wave Generator (SWG) values is mixed into the audio stream 01 = Only the first SWG value is output 10 = Only the second SWG value is output 11 = 1-Cos(SWG1) or S_ramp function for headphone detection. The high period is determined by the beep_on_per setting	0x0

Table 165: TONE_GEN_CYCLES (Page 0: 0x000000B6)

Bit	Mode	Symbol	Description	Reset
2:0	R/W	beep_cycles	Beep control. This specified the number of beep cycles required. 000 = 1 cycle 001 = 2 cycles 010 = 3 cycles 011 = 4 cycles 100 = 8 cycles 101 = 16 cycles 110 = 32 cycles 111 = continuous (until start_stopn is set to 0)	0x0

Table 166: TONE_GEN_FREQ1_L (Page 0: 0x000000B7)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	freq1_l	Lower byte of the output frequency for the first Sine Wave Generator (SWG) If sample rate (SR) = 8/12/16/24/32/48/96 kHz freq1=(2^16*(f/12000))-1 If sample rate (SR) =11.025/22.05/44.4/88.2 kHz, freq1=(2^16*(f/11025))-1	0x55

Table 167: TONE_GEN_FREQ1_U (Page 0: 0x000000B8)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	freq1_u	Upper byte of the output frequency for the first Sine Wave Generator (SWG) If sample rate (SR) = 8/12/16/24/32/48/96 kHz freq1=(2^16*(f/12000))-1 If sample rate (SR) =11.025/22.05/44.4/88.2 kHz, freq1=(2^16*(f/11025))-1	0x15

Table 168: TONE_GEN_FREQ2_L (Page 0: 0x000000B9)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	freq2_l	Lower byte of the output frequency for the second Sine Wave Generator (SWG) If sample rate (SR) = 8/12/16/24/32/48/96 kHz freq1=(2^16*(f/12000))-1 If sample rate (SR) =11.025/22.05/44.4/88.2 kHz, freq1=(2^16*(f/11025))-1	0x0

Table 169: TONE_GEN_FREQ2_U (Page 0: 0x000000BA)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	freq2_u	Upper byte of the output frequency for the second Sine Wave Generator (SWG) If sample rate (SR) = 8/12/16/24/32/48/96 kHz freq1=(2^16*(f/12000))-1 If sample rate (SR) =11.025/22.05/44.4/88.2 kHz, freq1=(2^16*(f/11025))-1	0x40

Table 170: TONE_GEN_ON_PER (Page 0: 0x000000BB)

Bit	Mode	Symbol	Description	Reset
5:0	R/W	beep_on_per	Beep ON period control 0x0 = 10 ms 0x1 = 20 ms 0x2 = 30 ms Continuing in 10 ms steps to… 0x14 = 200 ms then… 0x15 = Reserved 0x16 = Reserved 0x17 = Reserved 0x18 = Reserved then... 0x19 = 250 ms 0x1A = 300 ms 0x1B = 350 ms Continuing in 50 ms steps to 0x3B = 1950 ms 0x3C = 2000 ms 0x3D = Reserved 0x3E = Reserved 0x3F = Continuous	0x2

Table 171: TONE_GEN_OFF_PER (Page 0: 0x000000BC)

Bit	Mode	Symbol	Description	Reset
5:0	R/W	beep_off_per	Beep OFF period control 0x0 = 10 ms 0x1 = 20 ms 0x2 = 30 ms Continuing in 10 ms steps to… 0x14 = 200 ms then… 0x15 = Reserved 0x16 = Reserved 0x17 = Reserved 0x18 = Reserved then... 0x19 = 250 ms 0x1A = 300 ms 0x1B = 350 ms Continuing in 50 ms steps to… 0x3B = 1950 ms 0x3C = 2000 ms 0x3D = Reserved 0x3E = Reserved 0x3F = Reserved	0x1

13 Package Information

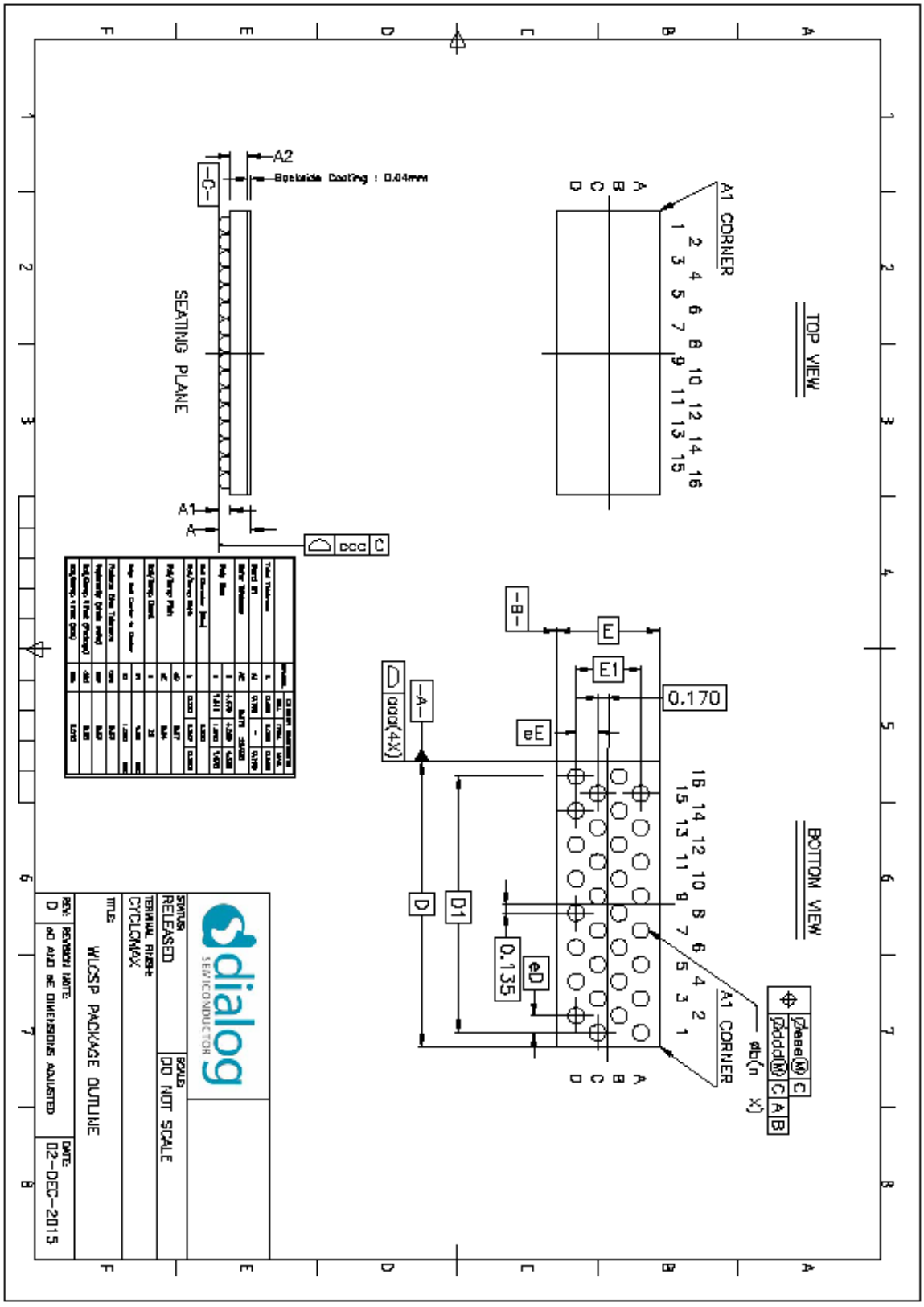

Figure 35: DA7219 Package Outline Drawing

14 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult Dialog Semiconductor's customer portal or your local sales representative.

Table 172: Ordering Information

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
DA7219-02VBA	32 WLCSP	4.5 x 1.64 mm	Tape and reel	4,500
DA7219-02VB6	32 WLCSP	4.5 x 1.64 mm	Tray/Waffle Pack (engineering samples only - not for mass production	98

Appendix A Applications Information

A.1 Codec Initialization

Depending on the specific application, some general settings need to be set. Examples of these settings include the sample rate, the PLL, and the DAI. Then the amplifiers, the mixers and channels of the ADC/DAC have to be configured and enabled using their respective control registers.

An example sequence is shown below:

1. Configure clock mode as required for operation, (for example PLL bypass, PLL or SRM mode).
2. Configure the DAI.
3. Configure the charge pump if the headphone path is in use.
4. Set input and output mixer paths and gains.
5. Enable input and output paths using the system controller.

A.2 Automatic ALC Calibration

When using the automatic level control (ALC) in hybrid mode the DC offset between the digital and analog PGAs must be cancelled. This is performed automatically if the following steps are followed:

1. Enable microphone amplifiers unmuted
2. Mute microphones
3. Enable input mixer and ADC unmuted
4. Enable AIF interface
5. Set alc_auto_calib_en in ALC_CTRL1 to ‘1’ (ALC_CTRL1 = 0x2F). This bit will auto clear when calibration is complete.
6. When calibration is complete, enable the ALC with alc_sync_mode and alc_offset_en (ALC_CTRL1 = 0x2F)
7. Unmute microphones

Appendix B Components

The following recommended components are examples selected from requirements of a typical application. The electrical characteristics (that is, the supported voltage/current ranges) have to be cross-checked and component types may need to be adapted from the individual needs of the target circuitry.

B.1 Audio Inputs

Table 173: Audio Inputs

Pin Name	Bump/Pin	Power Domain	Description	Type
MIC_N	A15	VDD	Differential mic. input (negative) / single-ended mic. input	Analog input
MIC_P	B16	VDD	Differential mic. input (positive) / single-ended mic. input	Analog input
MIC	C15	N/A	Supply input for headset microphone power	Analog input

DA7219 microphone inputs can be configured to accommodate single-ended or differential analog microphones, line inputs or digital microphones.

When using the inputs in an analog configuration, a DC blocking capacitor is required for each input bump used in the target application. The choice of capacitor is determined by the filter that is formed between that capacitor and the input impedance of the input pin, see Table 7.

$$C = \frac{1}{2\pi . R . F_c}$$

Where Fc is the 3 dB cutoff frequency of the low-pass filter (typically 20 Hz for audio applications). A 1 µF capacitor is suitable for most applications.

Due to their high stability, tantalum capacitors are particularly suitable for this application. Ceramic equivalents with an X5R dielectric are recommended as a cost effective alternative. Care should be taken to ensure that the desired capacitance is maintained over operating temperature and voltage.

Z5U dielectric ceramics should be avoided due to their susceptibility to microphonic effects.

Unused input bumps can be left floating or connected via a capacitor to ground.

The MIC pin would normally be connected to MICBIAS using a 2k2 resistor. This pin is an input to supply the microphone power when a headset is connected to the headset socket. The polarity of the microphone pin is determined by the accessory detect circuitry and the power is switched internally in the device to allow the microphone bias to be provided from this pin.

B.2 Microphone Bias

Table 174: Microphone Bias

Pin Name	Bump/Pin	Power Domain	Description	Type
MICBIAS	B14	VDD_MIC	Microphone bias output (Note 1)	Analog output
MIC	C15	VDD_MIC	Microphone bias input to AccDet	Analog Input

Note 1 A 1 µF capacitor to GND should be used to decouple the MICBIAS output.

Note 2 The recommended value for RBIAS = 2.2 kΩ

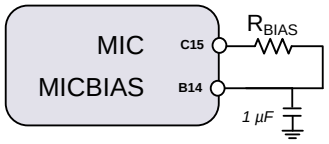

Figure 36: MICBIAS Decoupling

B.3 Audio Outputs

Table 175: Headset

Pin Name	Bump/Pin	Power Domain	Description	Type
HP_L	A5	VDD	headphone output (left)	Analog output
HP_R	A3	VDD	headphone output (right)	Analog output
RING2	C13	VDD_MIC	Connection to RING2 on headset jack	Analog input/ground
RING2_SENSE	B4	VDD_MIC	Ring2 sense line	Analog input/ground
SLEEVE	A11	VDD_MIC	Connection to SLEEVE on headset jack	Analog input/ground
SLEEVE_SENSE	B6	VDD_MIC	Sleeve sense line	Analog input/ground
JACKDET	D16	VDD	Jack insertion detect pin (Note 1)	Analog input
MIC_P	B16	VDD	Microphone input (P)	Analog Input
MIC_N	A15	VDD	Microphone input (N)	Analog Input

Note 1 The JACKDET pin is designed to be pulled either HIGH or LOW on the insertion of the jack. If using an HPLDET type headset socket additional external circuitry is required.

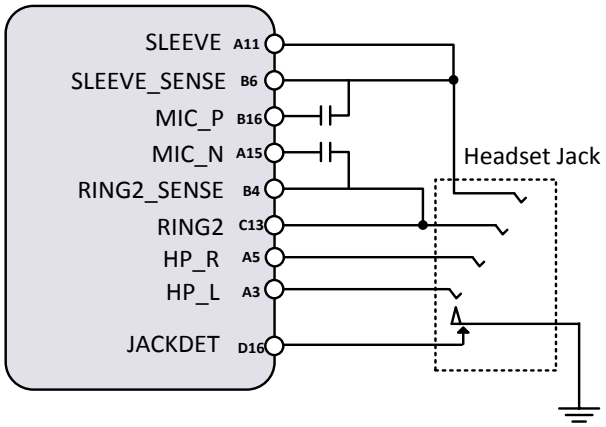

Figure 37: Recommended Headphone Layout

B.4 Headphone Charge Pump

Table 176: Headphone Charge Pump

Pin name	Bump/pin	Power Domain	Description	Type
HPCSP	A1	VDD	Charge pump reservoir capacitor (pos)	Charge pump
HPCSN	C1	VDD	Charge pump reservoir capacitor (neg)	Charge pump
HPCFP	D2	VDD	Charge pump flying capacitor (pos)	Charge pump
HPCFN	C3	VDD	Charge pump flying capacitor (neg)	Charge pump

A 1 µF reservoir capacitor is required between the HPCSP and GND and between HPCSN and GND. For best performance the capacitors should be fitted as near to the device as possible.

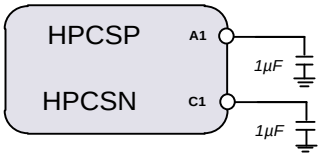

Figure 38: Charge Pump Decoupling

A 1 µF flying capacitor is required between HPCFP and HPCFN. For best performance the capacitor should be fitted as near to the device as possible.

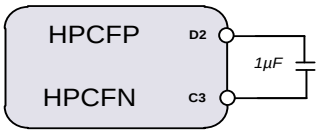

Figure 39: Charge Pump Flying Capacitor

To ensure stable charge pump operation the effective series resistance of the flying capacitor should be kept to a minimum. This can be achieved by selecting an appropriate capacitor dielectric (X5R, X7R) and ensuring that the capacitor is placed as near to the device as possible. Ideally the connection between the pins and the capacitor should not run through vias (connected on top layer of PCB only).

B.5 Digital Interfaces

Table 177: Digital Interfaces – I²C

Pin name	Bump/pin	Power domain	Description	Type
SDA	D14	VDD_IO	I²C bidirectional data	Digital input / output
SCL	D12	VDD_IO	I²C clock input	Digital input

The I²C data and clock lines are powered from VDD_IO. Both I²C lines require a pull up to VDD_IO. The value of this pull up is dependent on I²C bus speed, bus length and supply voltage. A 2.2 kΩ resistor is satisfactory in most applications.

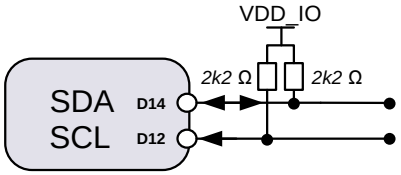

Figure 40: I²C Pull Ups

Table 178: Digital Interfaces - I²S

Pin name	Bump/pin	Power domain	Description	Type
DATIN	C7	VDD_IO	DAI data input	Digital input
DATOUT	C9	VDD_IO	DAI data output	Digital output
BCLK	D6	VDD_IO	DAI bit clock	Digital input / output
WCLK	D8	VDD_IO	DAI word clock (L/R select)	Digital input / output
MCLK	C11	VDD_IO	Master clock	Digital input

The DAI interface pins should be treated as clock signals and the appropriate layout rules for routing clocks should be adhered to.

B.6 References

Table 179: References

Pin name	Bump/pin	Power domain	Description	Type
VMID	A9	VDD	Audio mid-rail reference capacitor	Reference
VREF	A7	VDD	Bandgap reference capacitor	Reference
DACREF	B8	VDD	Audio DAC reference capacitor	Reference

A 1 µF capacitor should be connected between each of the references and GND. For best performance the capacitors should be fitted as near to the device as possible.

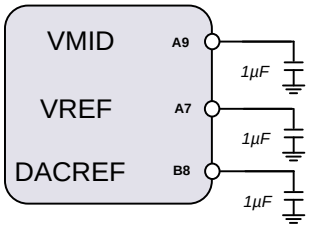

Figure 41: Reference Capacitors

B.7 Supplies

Table 180: Power Supplies

Pin Name	Bump/Pin	Power Domain	Description	Type
VDD	C5	Min: 1.7 V Max: 2.65 V	Supply for analog and digital circuits / Supply for headphone charge pump	Power supply
VDD_IO	D4	Min: 1.7 V Max: 3.6 V	Supply for digital interfaces. V_{DD_IO} must be greater than or equal to V_{DD}	Power supply
VDD_MIC	A13	Min: 1.8 V* Max: 3.6 V	Supply for microphone bias circuits. V_{DD_MIC} must be greater than or equal to V_{DD}	Power supply

Note: Both V_{DD_IO} and V_{DD_MIC} must be greater or equal to V_{DD}.

Decoupling capacitors are recommended between all supplies and GND. These capacitors should be located as near to the device as possible.

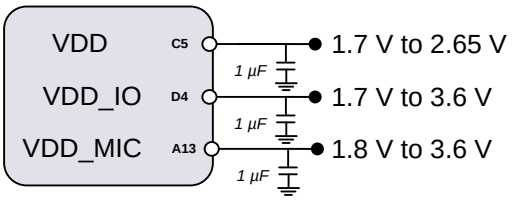

Figure 42: Power Supply Decoupling

B.8 Ground

Table 181: Ground

Pin name	Bump/pin	Power domain	Description	Type
GND	B10		Analog ground	Power ground
GND_HP	B12		Headphone ground	Power ground
GND_CP	B2		Charge pump/digital ground	Power ground

GND, GND_HP and GND_CP should be connected directly to the system ground. In addition, GND_HP and GND_CP should be routed separately and connected to the system GND plane by their own seperate vias.

Appendix C PCB Layout Guidelines

DA7219 uses Dialog Semiconductor's RouteEasy™ technology allowing the device to be routed using conventional, low cost, PCB technology. All device balls are routable on the top level and conventional plated through hole vias can be used throughout.

This design is fully realizable using a two-layer PCB. For optimum performance it is recommended that a four-layer PCB is used with layers two and three as solid ground planes.

Decoupling and reference capacitors should be located as close to the device as possible and appropriately sized tracks should be used for all power connections.

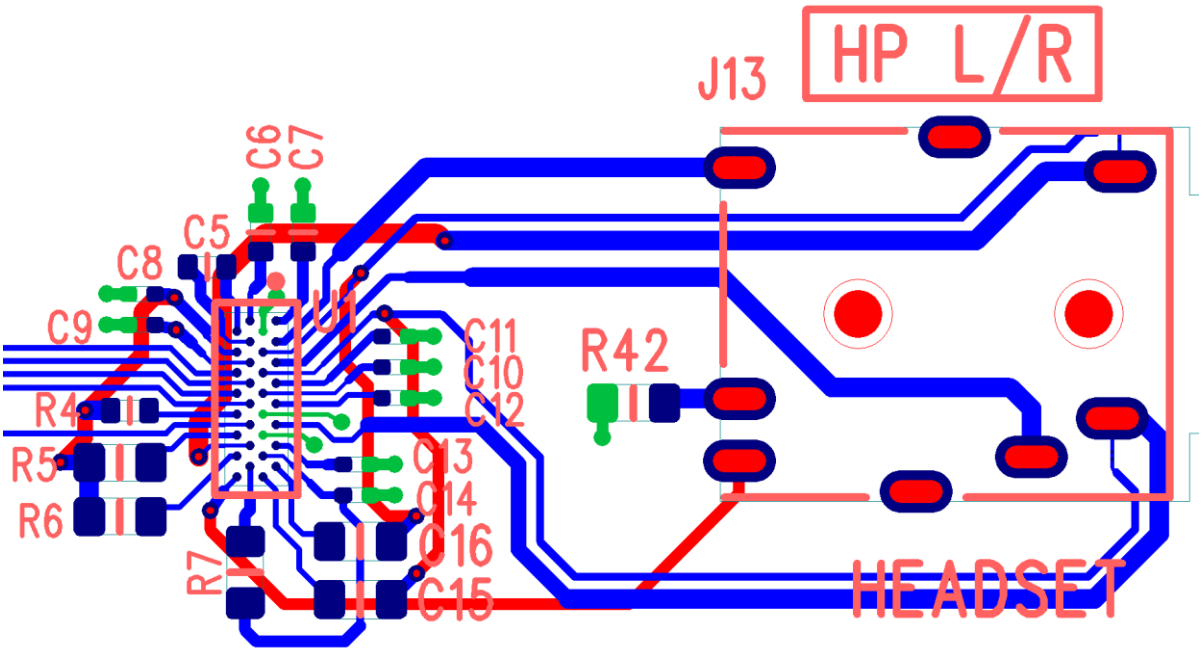

Figure 43: DA7219 Example Layout

C.1 Layout and Schematic Support

Copies of the evaluation board schematics and layout are available on request to aid in PCB development. Dialog Semiconductor also offer a schematic and layout review service for all designs using Dialog's devices. Please contact your local Dialog Semiconductor Office if you wish to use this service.

C.2 General Recommendations

- Appropriate trace width and number of vias should be used for all power supply paths.
- A common ground plane should be used, which allows proper electrical and thermal performance.
- Noise-sensitive analog signals such as feedback lines or clock connections should be kept away from traces carrying pulsed analog or digital signals. This can be achieved by separation (distance) or by shielding with quiet signals or ground traces.
- Decoupling capacitors should be X5R ceramics and should be placed as near to the device as possible.
- Charge pump capacitors should be X5R ceramics and should be placed as near to the device as possible.

C.3 Capacitor Selection

Ceramic capacitors are manufactured with a variety of dielectrics, each with a different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range, dc bias conditions and low Equivalent Series Resistance (ESR). X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended for best performance. Y5V and Z5U dielectrics are not recommended for use because of their poor temperature and dc bias characteristics.

The worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage is calculated using the following equation:

$$C_{EFF} = C_{OUT}\ x\ (1 - TEMPCO)\ x\ (1 - TOL)$$

where: C_{EFF} is the effective capacitance at the operating voltage. TEMPCO is the worst-case capacitor temperature coefficient. TOL is the worst-case component tolerance. These figures can be found in the manufacturer's datasheet.

In the example below, the worst-case temperature coefficient (TEMPCO) over −55°C to +85°C is assumed to be 15%. The tolerance of the capacitor (TOL) is assumed to be 10%, and COUT is 0.65 µF at 1.8 V.

Substituting these values in the equation yields

$$C_{EFF} = 0.65\mu F\ x\ (1 - 0.15)\ x\ (1 - 0.1) = 0.497\ \mu F$$

Table 182: Recommended Capacitor Values

Application	Value	Size	Temp. Char.	Tolerance	Rated Voltage	Type
VDD,VDD_IO, VDD_MIC, DACREF, VMID,VREF, HPCFP/HPCFN, HPCSP, HPCSN, MICBIAS	10 x 1 µF	0201	X5R +/- 15 %	+/-10 %	6.3 V	Murata GRM033R60J105M

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.dialog-semiconductor.com.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

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RoHS Compliance

Dialog Semiconductor's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

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