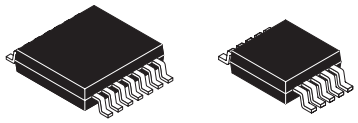


SLVS333 − AUGUST 2001

LDO AND DUAL SWITCH WITH CONTROLLED RISE TIMES FOR DSP AND PORTABLE APPLICATIONS

FEATURES

- **Two 340-mΩ (Typical) High-Side MOSFETs**
- **200 mA Low-Dropout Voltage Regulator In Fixed 3.3-V or Adjustable Versions**
- **Independent Thermal- and Short-Circuit Protection for LDO and Each Switch**
- **Overcurrent Indicators With Transient Filter**
- **2.9-V to 5.5-V Operating Range**
- **CMOS- and TTL-Compatible Enable Inputs**
- **75-μA (Typical) Supply Current**
- **Available in 10-Pin MSOP or 14-Pin TSSOP (PowerPAD™)**
- **−40°C to 85°C Ambient Temperature Range**

APPLICATIONS

- **USB Hubs and Peripherals**
  - **Keyboards**
  - **Zip Drives**
  - **Speakers and Headsets**
- **PDAs and Portable Electronics**
- **DSP Power Sequencing**

DESCRIPTION

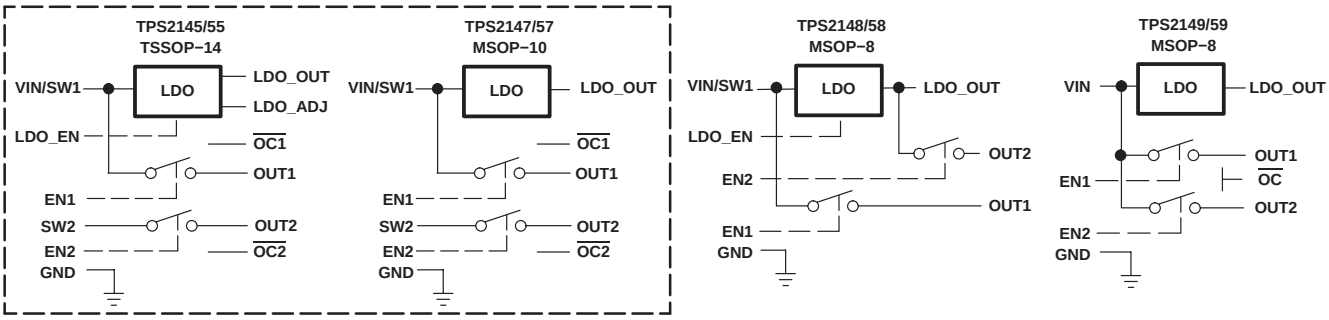
Two power-distribution switches and an adjustable (TPS2145) or fixed (TPS2147) LDO are incorporated in one small package, providing a power management solution that saves up to 60% in board space over typical implementations.

Designed to meet USB 2.0 bus-powered hub requirements, these devices also allow core and I/O voltage sequencing in DSP applications, or power segmentation in portable equipment. Each current-limited switch is a 340-mΩ N-channel MOSFET capable of supplying 200 mA of continuous current. A logic enable compatible with 5-V logic and 3-V logic controls each MOSFET as well as the LDO in the TPS2145. The internal charge pump provides the gate drive controlling the power-switch rise times and fall times, minimizing current surges during switching. The charge pump requires no external components.

The LDO has a drop-out voltage of only 0.35 V and with the independent enable on the TPS2145 LDO, the LDO can be used as an additional switch. The LDO output range for the TPS2145 is 1 V to 3.3 V, while the TPS2147 is fixed at 3.3 V.

The TPS2145 and TPS2147 have active-low switch enables and the TPS2155 and TPS2157 have active-high switch enables.

LDO and dual switch family selection guide and schematics



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

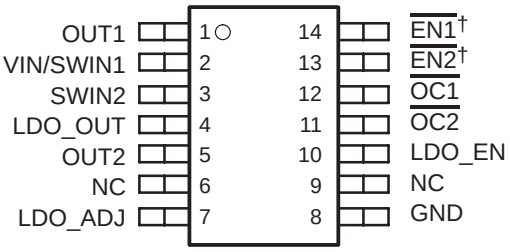
PowerPAD is a trademark of Texas Instruments.

AVAILABLE OPTIONS

T_A	DESCRIPTION	PACKAGE AND PIN COUNT	PACKAGED DEVICES	
			ACTIVE LOW (SWITCH)	ACTIVE HIGH (SWITCH)
−40°C to 85°C	Adjustable LDO with LDO enable	TSSOP-14	TPS2145IPWP	TPS2155IPWP
	3.3-V fixed LDO	MSOP-10	TPS2147IDGQ	TPS2157IDGQ
	3.3-V Fixed LDO with LDO enable and LDO output switch	MSOP-8	TPS2148IDGN	TPS2158IDGN
	3.3-V Fixed LDO, shared input with switches	MSOP-8	TPS2149IDGN	TPS2159IDGN

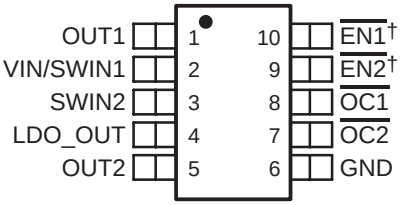
NOTE: All options available taped and reeled. Add an R suffix (e.g. TPS2145IPWPR)

TPS2145, TPS2155
TSSOP (PWP) PACKAGE
(TOP VIEW)



NC − No internal connection
† Pin 13 and 14 are active high for TPS2155.

TPS2147, TPS2157
MSOP (DGQ) PACKAGE
(TOP VIEW)



† Pin 9 and 10 are active high for TPS2157.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Input voltage range: $V_{I(VIN/SWIN1)}$, $V_{I(SWIN2)}$, $V_{I(ENx)}$, $V_{I(LDO\_EN)}$ . . . . . −0.3 V to 6 V
Output voltage range: $V_{O(OUTx)}$, $V_{O(LDO\_OUT)}$, $V_{O(OCx)}$ . . . . . −0.3 V to 6 V
Maximum output current, $I_{O(OCx)}$ . . . . . ±10 mA
Continuous output current, $I_{O(OUTx)}$, $I_{O(LDO\_OUT)}$ . . . . . Internally limited
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating virtual-junction temperature range, T_J . . . . . −40°C to 110°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Electrostatic discharge (ESD) protection: Human body model . . . . . 2 kV
Charged device model (CDM) . . . . . 1 kV

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
MSOP10	1293.1 mW	17.2 mW/°C	517.2 mW	258.6 mW
PWP14	2000 mW	26.6 mW/°C	800 mW	400 mW

recommended operating conditions

		MIN	MAX	UNIT
Input voltage	$V_{I(VIN/SWIN1)}$	2.9	5.5	V
	$V_{I(SWIN2)}$	2.9	5.5	
	$V_{I(ENx)}$	0	5.5	
	$V_{I(LDO\_EN)}$	0	5.5	
Continuous output current, I_O	LDO_OUT		200	mA
	OUT1, OUT2		150	
Output current limit, $I_{O(LMT)}$	LDO_OUT	275	550	mA
	OUT1, OUT2	200	400	
Operating virtual-junction temperature range, T_J		−40	100	°C

electrical characteristics over recommended operating junction-temperature range, $2.9\ V \le V_{I(VIN/SWIN1)} \le 5.5\ V$, $2.9\ V \le V_{I(SWIN2)} \le 5.5\ V$, $T_J = -40°C$ to 100°C (unless otherwise noted)

general

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Off-state supply current	$V_{I(VIN/SWIN1)} = 5\ V$, $V_{I(SWIN2)} = 5\ V$	$V_{I(\overline{ENx})} = 5\ V$ (inactive), $V_{I(LDO\_EN)} = 0\ V$ (inactive), $V_{O(LDO\_OUT)}$ = no load, $V_{O(OUTx)}$ = no load			20	µA
	Forward leakage current		$V_{I(\overline{ENx})} = 5\ V$ (inactive), $V_{I(LDO\_EN)} = 0\ V$ (inactive), $V_{O(LDO\_OUT)} = 0\ V$, $V_{O(OUTx)} = 0\ V$ (measured from outputs to ground)			1	µA
I_I	Total input current at VIN/SWIN1 and SWIN2	$V_{I(VIN/SWIN1)} = 5\ V$, $V_{I(SWIN2)} = 5\ V$, No load on OUTx, No load on LDO_OUT	$V_{I(LDO\_EN)} = 5\ V$ (active), $V_{I(ENx)}$ = on (active)			150	µA
			$V_{I(LDO\_EN)} = 0\ V$ (inactive), $V_{I(ENx)}$ = on (active)			100	µA
			$V_{I(LDO\_EN)} = 5\ V$ (active), $V_{I(ENx)}$ = off (inactive)			100	µA

electrical characteristics over recommended operating junction-temperature range, $2.9\ V \le V_{I(VIN/SWIN1)} \le 5.5\ V$, $2.9\ V \le V_{I(SWIN2)} \le 5.5\ V$, $V_{I(\overline{ENx})} = 0\ V$ or $V_{I(ENx)} = 5\ V$, $V_{I(LDO\_EN)} = 5\ V$, $T_J = -40°C$ to $100°C$ (unless otherwise noted)

power switches

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$r_{DS(on)}$	Static drain-source on-state resistance, VIN/SWIN1 or SWIN2 to OUTx	T_J = −40°C to 100°C, $I_{O(LDO\_OUT)}$ = 200 mA, IOUT1 and IOUT2 = 150 mA				580	mΩ
		T_J = 25°C, $I_{O(LDO\_OUT)}$ = 200 mA, IOUT1 and IOUT2 = 150 mA			340		
$I_{lkg(R)}$	Reverse leakage current at OUTx	$V_{O(OUTx)}$ = 5 V, LDO_EN = don't care	$V_{I(\overline{ENx})}$ = 5 V, $V_{I(ENx)}$ = 0 V, SWIN2 floating, $V_{I(VIN/SWIN1)}$ = 5 V			10	µA
			$V_{I(\overline{ENx})}$ = 5 V, $V_{I(ENx)}$ = 0 V, $V_{I(SWIN2)}$ = 0, $V_{I(VIN/SWIN1)}$ = 2.9 V			10	
			$V_{I(\overline{ENx})}$ = 5 V, $V_{I(ENx)}$ = 0 V, $V_{I(SWIN2)}$ = 0, $V_{I(VIN/SWIN1)}$ = 0 V			10	
I_{OS}	Short circuit output current	OUTx connected to GND, device enabled into short circuit		0.2		0.4	A
	Delay time for asserting $\overline{OC}$ flag	From IOUTx at 95% of current limit level to 50% $\overline{OC}$			5.5		ms
	Delay time for deasserting $\overline{OC}$ flag	From IOUTx at 95% of current limit level to 50% $\overline{OC}$			10.5		ms

timing parameters, power switches

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{on}	Turnon time, OUTx switch, (see Note 1)	C_L = 100 µF	R_L = 33 Ω	0.5		6	ms
		C_L = 1 µF		0.1		3	
t_{off}	Turnoff time, OUTx switch (see Note 1)	C_L = 100 µF	R_L = 33 Ω	5.5		12	
		C_L = 1 µF		0.05		4	
t_r	Rise time, OUTx switch (see Note 1)	C_L = 100 µF	R_L = 33 Ω	0.5		5	
		C_L = 1 µF		0.1		2	
t_f	Fall time, OUTx switch (see Note 1)	C_L = 100 µF	R_L = 33 Ω	5.5		9	
		C_L = 1 µF		0.05		1.2	

NOTE 1. Specified by design, not tested in production.

undervoltage lockout at VIN/SWIN1

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
UVLO Threshold		2.2		2.85	V
Hysteresis (see Note 1)			260		mV
Deglitch (see Note 1)		50			µs

NOTE 1. Specified by design, not tested in production.

electrical characteristics over recommended operating junction-temperature range, $2.9\ V \le V_{I(VIN/SWIN1)} \le 5.5\ V$, $2.9\ V \le V_{I(SWIN2)} \le 5.5\ V$, $V_{I(ENx)} = 0\ V$ or $V_{I(ENx)} = 5\ V$, $V_{I(LDO\_EN)} = 5\ V$, $T_J = -40°C$ to $100°C$ (unless otherwise noted) (continued)

undervoltage lockout at SWIN2

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	UVLO Threshold		2.2		2.85	V
	Hysteresis (see Note 1)			260		mV
	Deglitch (see Note 1)		50			µs

NOTE 1. Specified by design, not tested in production.

electrical characteristics over recommended operating junction-temperature range, $2.9\ V \le V_{I(VIN/SWIN1)} \le 5.5\ V$, $2.9\ V \le V_{I(SWIN2)} \le 5.5\ V$, $V_{I(ENx)} = 0\ V$ or $V_{I(ENx)} = 5\ V$, $V_{I(LDO\_EN)} = 5\ V$, $C_{L(LDO\_OUT)} = 10\ \mu F$, $T_J = -40°C$ to $100°C$ (unless otherwise noted)

fixed-voltage regulator, 3.3 V

PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
V_O	Output voltage, dc	$V_{I(VIN/SWIN1)}$ = 4.25 V to 5.25 V, $I_{O(LDO\_OUT)}$ = 0.5 mA to 200 mA	3.20	3.3	3.40	V
	Dropout voltage	$V_{I(VIN/SWIN1)}$ = 3.2 V, $I_{O(LDO\_OUT)}$ = 200 mA, $I_{O(OUT1)}$ = 150 mA			0.35	V
	Line regulation voltage (see Note 1)	$V_{I(VIN/SWIN1)}$ = 4.25 V to 5.25 V, $I_{O(LDO\_OUT)}$ = 5 mA			0.1	%/V
	Load regulation voltage (see Note 1)	$V_{I(VIN/SWIN1)}$ = 4.25 V, $I_{O(LDO\_OUT)}$ = 5 mA to 200 mA		0.4%	1.15%	
I_{OS}	Short-circuit current limit	$V_{I(VIN/SWIN1)}$ = 4.25 V, LDO_OUT connected to GND	0.275	0.33	0.55	A
$I_{lkg(R)}$	Reverse leakage current into LDO_OUT	$V_{O(LDO\_OUT)}$ = 3.3 V, $V_{I(VIN/SWIN1)}$ = 0 V, $V_{I(LDO\_EN)}$ = 0 V		10		µA
		$V_{O(LDO\_OUT)}$ = 5.5 V, $V_{I(VIN/SWIN1)}$ = 2.9 V, $V_{I(LDO\_EN)}$ = 0 V		10		µA
t_{on}	Turnoff time, LDO_EN transitioning low (see Note 1)	R_L = 16 Ω, $C_{L(LDO\_OUT)}$ = 10 µF	0.25		1	ms
t_{off}	Turnon time, LDO_EN transitioning high (see Note 1)	R_L = 16 Ω, $C_{L(LDO\_OUT)}$ = 10 µF	0.1		1	ms
	Ramp-up time, LDO_OUT (0% to 90%)	$V_{I(LDO\_EN)}$ = 5 V, VIN/SWIN1 ramping up from 10% to 90% in 0.1 ms, R_L = 16 Ω, $C_{L(LDO\_OUT)}$ = 10 µF	0.1		1	ms
	Power supply rejection	f = 1 kHz, $C_{L(LDO\_OUT)}$ = 4.7 µF, ESR = 0.25 Ω, IO = 5 mA, $V_{I(VIN/SWIN1)p-p}$ = 100 mV		50		dB

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
NOTE 1. Specified by design, not tested in production.

electrical characteristics over recommended operating junction-temperature range, $2.9\ V \le V_{I(VIN/SWIN1)} \le 5.5\ V$, $2.9\ V \le V_{I(SWIN2)} \le 5.5\ V$, $V_{I(ENx)} = 0\ V$ or $V_{I(ENx)} = 5\ V$, $V_{I(LDO\_EN)} = 5\ V$, $C_{L(LDO\_OUT)} = 10\ \mu F$, $T_J = -40°C$ to $100°C$ (unless otherwise noted) (continued)

adjustable voltage regulator (Vx = 1 V to 3.3 V)

PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
V_O	Output voltage, dc (see Note 2)	$V_{I(VIN/SWIN1)}$ =Vx + 0.6 V to 5.5 V and $V_{I(VIN/SWIN1)}$ > 2.9 V, I_O = 0.5 mA to 200 mA	0.97Vx	Vx	1.03Vx	V
	Dropout voltage (VIN/SWIN1 to LDO_OUT)	$V_{I(VIN/SWIN1)}$ = Vx − 0.1 V, I_O = 200 mA			0.5	V
	Line regulation voltage (see Note 1)	$V_{I(VIN/SWIN1)}$ = Vx + 0.6 V to 5.5 V and $V_{I(VIN/SWIN1)}$ > 2.9 V, I_O = 5 mA			0.1	%/V
	Load regulation voltage (see Note 1)	$V_{I(VIN/SWIN1)}$ = Vx + 0.6 V to 5.5 V and $V_{I(VIN/SWIN1)}$ > 2.9 V, I_O = 5 mA to 200 mA		0.4%	1%	
I_{OS}	Short-circuit current limit	$V_{I(VIN/SWIN1)}$ = Vx + 0.6 V to 5.5 V and $V_{I(VIN/SWIN1)}$ > 2.9 V, LDO_OUT connected to GND	0.275	0.33	0.575	A
$I_{lkg(R)}$	Reverse leakage current into LDO_OUT	$V_{O(LDO\_OUT)}$ = Vx, $V_{I(VIN/SWIN1)}$ = 0 V, $V_{I(LDO\_EN)}$ = 0 V		10		µA
		$V_{O(LDO\_OUT)}$ = 5.5 V, $V_{I(VIN/SWIN1)}$ = 2.8 V, $V_{I(LDO\_EN)}$ = 0 V		10		µA
t_{on}	Turnoff time, LDO_EN transitioning low (see Note 1)	From 50% LDO_EN to 10% LDO_OUT, R_L = Vx/0.2 Ω, $C_{L(LDO\_OUT)}$ = 10 µF	0.1		1	ms
t_{off}	Turnon time, LDO_EN transitioning high (see Note 1)	From 50% LDO_EN to 90% LDO_OUT, R_L = Vx/0.2 Ω, $C_{L(LDO\_OUT)}$ = 10 µF	0.1		1	ms
	Ramp-up time, LDO_OUT (0% to 90%)	$V_{I(LDO\_EN)}$ = 5 V, VIN/SWIN1 ramping up from 10% to 90% in 0.1 ms, R_L = Vx/0.2 Ω, $C_{L(LDO\_OUT)}$ = 10 µF	0.1		1	ms
	Output tracking OUT1 lag time from LDO_OUT given LDO_EN and EN1 have been asserted simultaneously to turnon their respective outputs. Measured at 1 V. (see Note 1)	LDO load R_L = Vx/0.2 Ω, $C_{L(LDO\_OUT)}$ = 10 µF, OUT1 R_L = 33 Ω, 10 µF, $V_{I(VIN/SWIN1)}$ = 3.3 V	0		1	ms
	Power supply rejection	f = 1 kHz, $C_{L(LDO\_OUT)}$ = 4.7 µF, ESR = 0.25 Ω, IO = 5 mA, $V_{I(VIN/SWIN1)p-p}$ = 100 mV		50		dB

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

NOTES: 1. Specified by design, not tested in production.
2. Does not include error introduced by external resistive divider R1, R2 tolerance.

electrical characteristics over recommended operating junction-temperature range, $2.9\ V \le V_{I(VIN/SWIN1)} \le 5.5\ V$, $2.9\ V \le V_{I(SWIN2)} \le 5.5\ V$, $V_{I(\overline{ENx})} = 0\ V$ or $V_{I(ENx)} = 5\ V$, $V_{I(LDO\_EN)} = 5\ V$, $T_J = -40°C$ to $100°C$ (unless otherwise noted)

enable input, $\overline{ENx}$ (active low)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_I	Input current, pullup (source)	$V_{I(\overline{ENx})} = 0\ V$			5	µA

enable input, ENx (active high)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_I	Input current, pulldown (sink)	$V_{I(ENx)} = 5\ V$			5	µA

enable input, LDO_EN (active high)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_I	Input current, pulldown	$V_{I(LDO\_EN)} = 5\ V$			5	µA
	Falling-edge deglitch (see Note 1)		50			µs

NOTE 1. Specified by design, not tested in production.

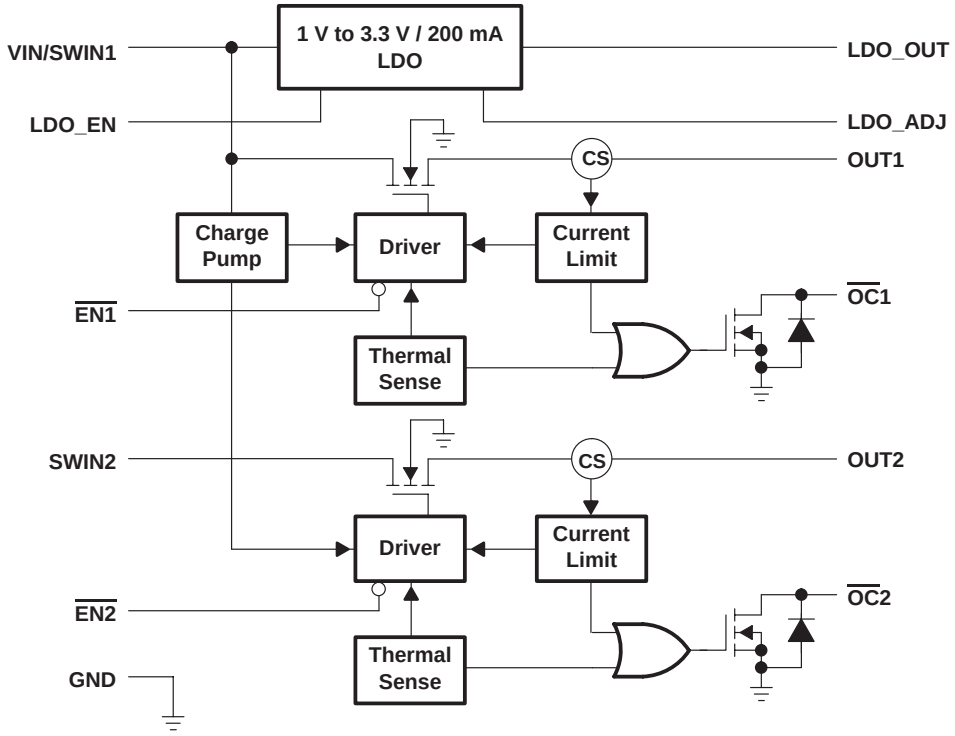
logic output, $\overline{OCx}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current sinking at $V_O = 0.4\ V$		1			mA

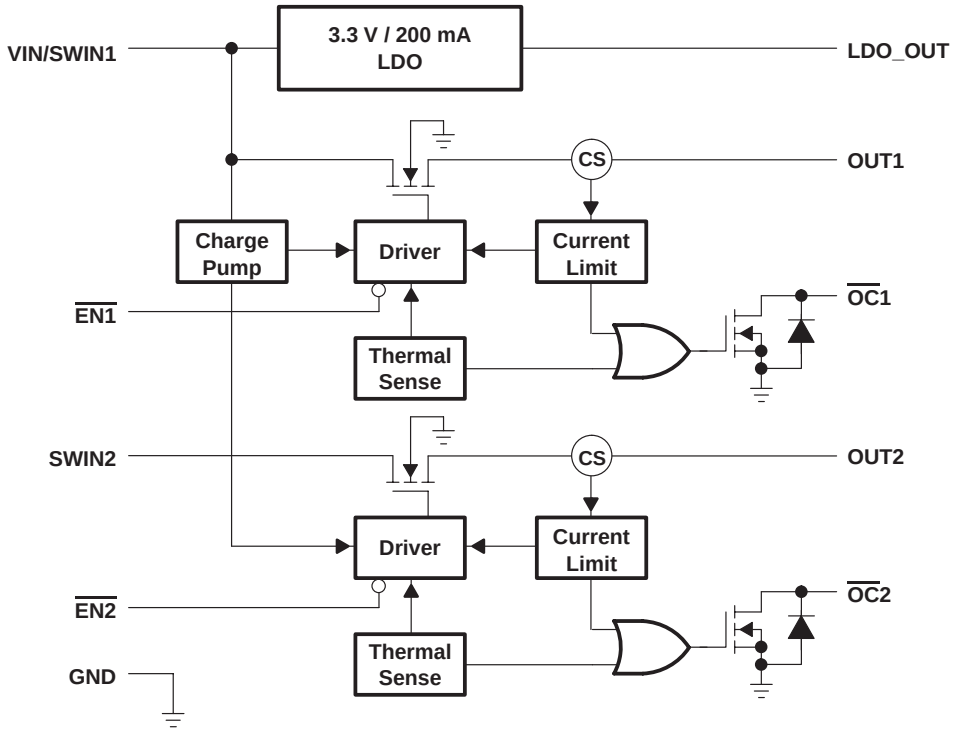
thermal shutdown characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
First thermal shutdown (shuts down switch or regulator in overcurrent)	Occurs at or above specified temperature when overcurrent is present.	120			°C
Recovery from thermal shutdown		110			
Second thermal shutdown (shuts down all switches and regulator)	Occurs on rising temperature, irrespective of overcurrent.	155			
Second thermal shutdown hysteresis			10		

TPS2145 functional block diagram



TPS2147 functional block diagram



Terminal Functions

TERMINAL					I/O	DESCRIPTION
NAME	NO.					
	PWP-14		DGQ-10			
	TPS2145	TPS2155	TPS2147	TPS2157		
EN1		14		10	I	Logic level enable to transfer power to OUT1
$\overline{\text{EN1}}$	14		10			
EN2		13		9	I	Logic level enable to transfer power to OUT2
$\overline{\text{EN2}}$	13		9			
GND	8	8	6	6		Ground
LDO_ADJ	7	7			I	User feedback for adjustable regulator
LDO_EN	10	10			I	Logic level LDO enable. Active high.
LDO_OUT	4	4	4	4	O	LDO output
NC	6, 9	6, 9				No connection
$\overline{\text{OC1}}$	12	12	8	8	O	Overcurrent status flag for OUT1. Open-drain output.
$\overline{\text{OC2}}$	11	11	7	7	O	Overcurrent status flag for OUT2. Open-drain output.
OUT1	1	1	1	1	O	Switch 1 output
OUT2	5	5	5	5		Switch 2 output
SWIN2	3	3	3	3	I	Input for switch 2
VIN/SWIN1	2	2	2	2	I	Input for LDO and switch 1; device supply voltage

detailed description

VIN/SWIN1

The VIN/SWIN1 serves as the input to the internal LDO and as the input to one N-channel MOSFET. The fixed or adjustable LDO has a dropout voltage of 0.35 V and is rated for 200 mA of continuous current. The power switch is an N-channel MOSFET with a maximum on-state resistance of 580 mΩ. Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled. The power switch is rated at 200 mA, continuous current. VIN/SWIN1 must be connected to a voltage source for device operation.

SWIN2

SWIN2 is the input to the other N-channel MOSFET, which also has a maximum on-state resistance of 580 mΩ. Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled. The power switch is rated at 200 mA, continuous current.

OUTx

OUT1 and OUT2 are the outputs from the internal power-distribution switches.

LDO_OUT

LDO_OUT is the output of the internal 200-mA LDO. The fixed version of the LDO has an output of 3.3 V. The adjustable version has an output voltage range of 1 V to 3.3 V.

LDO_ADJ

This input only applies to the adjustable LDO version of this device (TPS2145/55). LDO_ADJ is used to adjust the output voltage anywhere between 1 V and 3.3 V.

LDO_EN

The active high input, LDO_EN, only applies to the adjustable LDO version of this device (TPS2145/55). LDO_EN is used to enable the internal LDO and is compatible with TTL and CMOS logic.

detailed description (continued)

enable ($\overline{\text{ENx}}$, ENx)

The logic enable disables the power switch. Both switches have independent enables and are compatible with both TTL and CMOS logic.

overcurrent ($\overline{\text{OCx}}$)

The $\overline{\text{OCx}}$ open-drain output is asserted (active low) when an overcurrent condition is encountered. The output will remain asserted until the overcurrent condition is removed.

current sense

A sense FET monitors the current supplied to the load. Current is measured more efficiently by the sense FET than by conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant-current mode and holds the current constant while varying the voltage on the load.

thermal sense

A dual-threshold thermal trip is implemented to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition, the junction temperature rises. When the die temperature rises to approximately 120°C, the internal thermal sense circuitry determines which power switch is in an overcurrent condition and turns off that switch, thus isolating the fault without interrupting operation of the adjacent power switch. Because hysteresis is built into the thermal sense, the switch turns back on after the device has cooled approximately 10 degrees. The switch continues to cycle off and on until the fault is removed.

undervoltage lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2.5 V, a control signal turns off the power switch.

PARAMETER MEASUREMENT INFORMATION

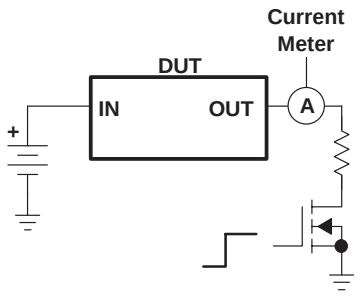


Figure 1. Current Limit Test Circuit

PARAMETER MEASUREMENT INFORMATION

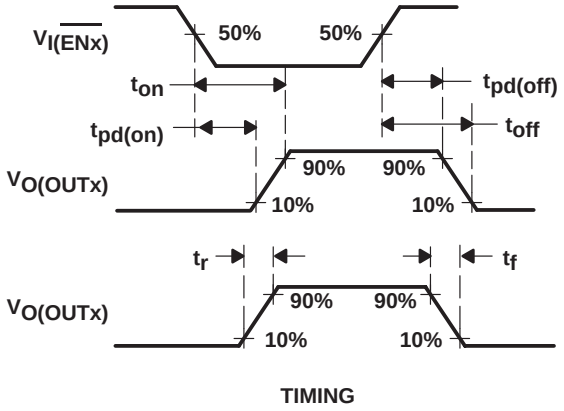


Figure 2. Timing and Internal Voltage Regulator Transition Waveforms

TYPICAL CHARACTERISTICS

SWITCH TURNON DELAY AND RISE TIME WITH 1-μF LOAD

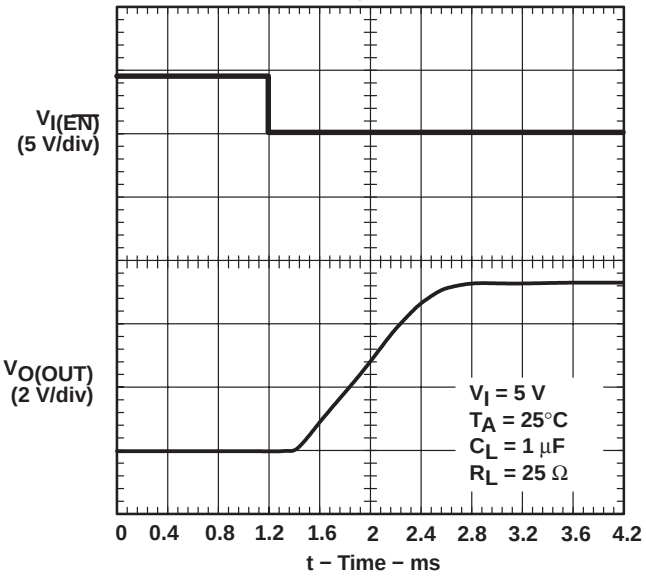


Figure 3

SWITCH TURNOFF DELAY AND FALL TIME WITH 1-μF LOAD

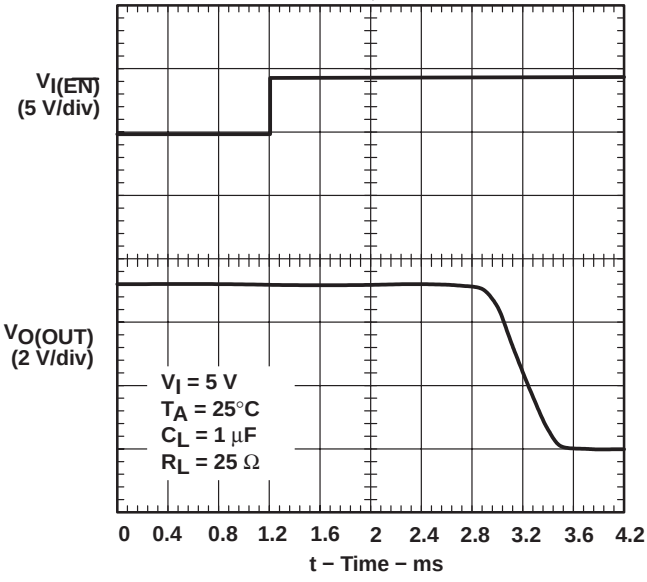


Figure 4

TYPICAL CHARACTERISTICS

SWITCH TURNON DELAY AND RISE TIME
WITH 120-μF LOAD

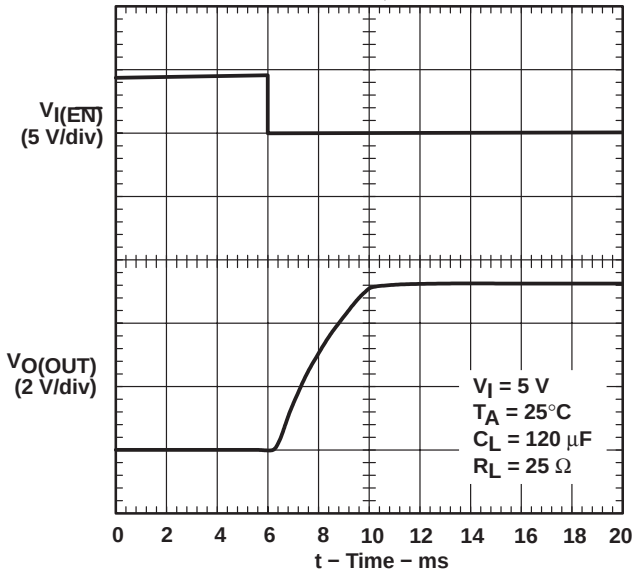


Figure 5

SWITCH TURNOFF DELAY AND FALL TIME
WITH 120-μF LOAD

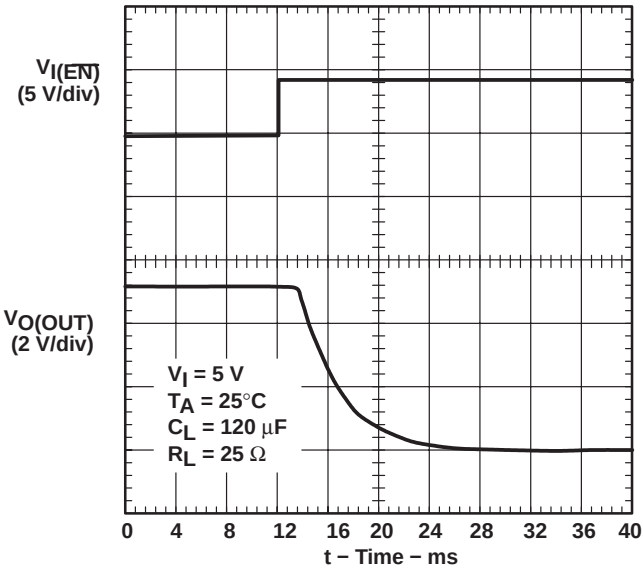


Figure 6

SHORT-CIRCUIT CURRENT, SWITCH
ENABLED INTO A SHORT

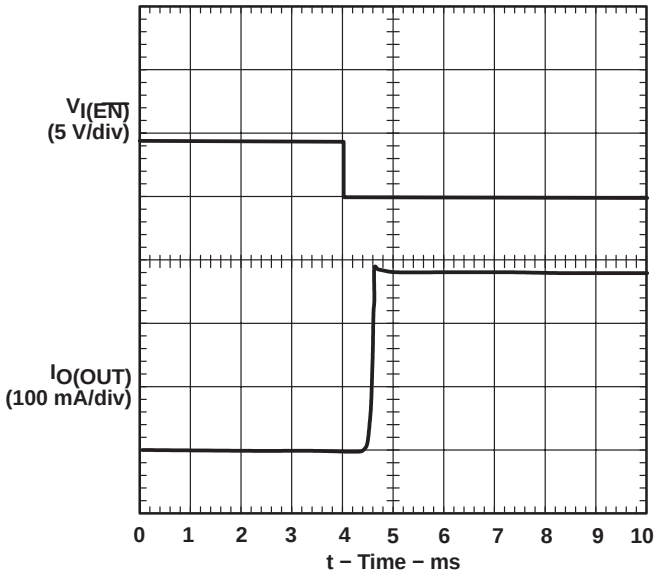


Figure 7

LDO TURNON DELAY AND RISE TIME
WITH 4.7-μF LOAD

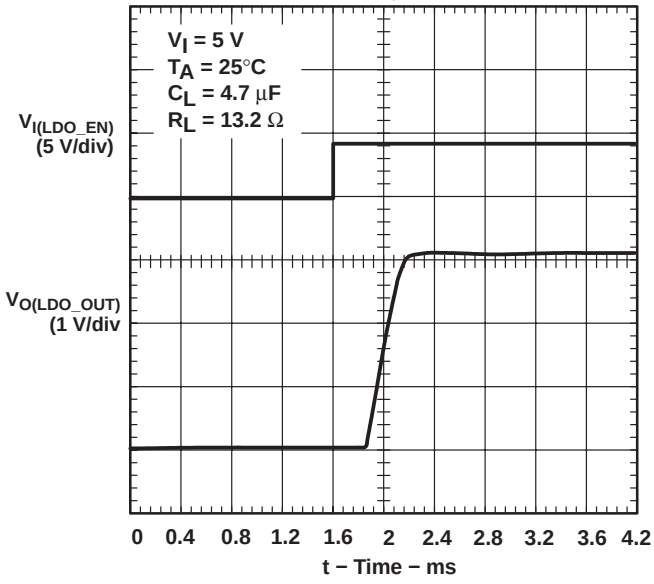


Figure 8

TYPICAL CHARACTERISTICS

LINE TRANSIENT RESPONSE

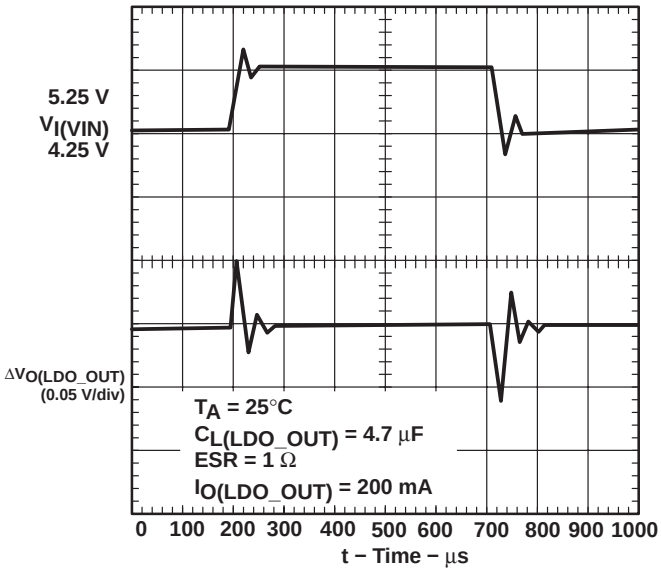


Figure 9

LOAD TRANSIENT RESPONSE

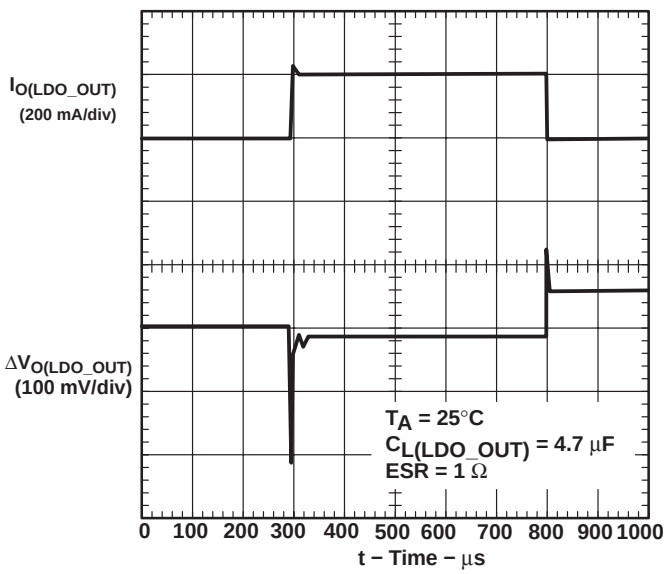


Figure 10

SUPPLY CURRENT vs JUNCTION TEMPERATURE

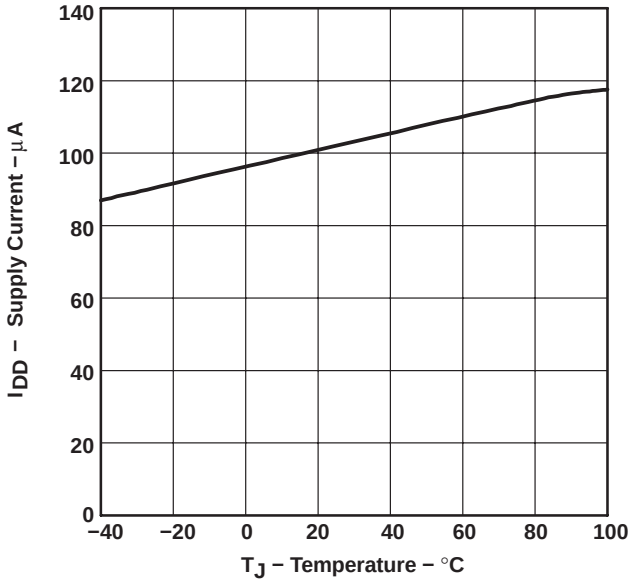


Figure 11

SUPPLY CURRENT vs SUPPLY VOLTAGE

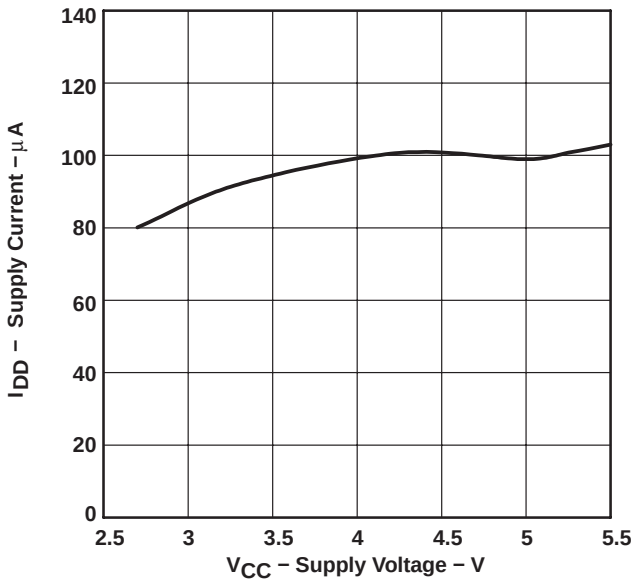


Figure 12

TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

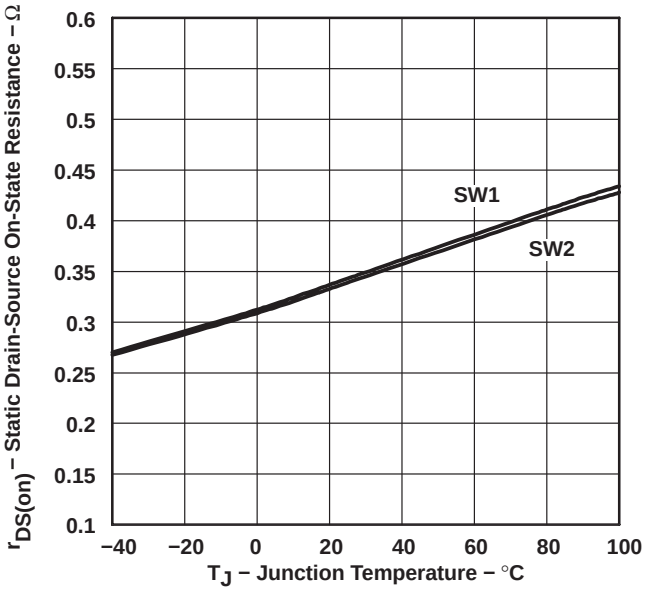


Figure 13

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
SUPPLY VOLTAGE

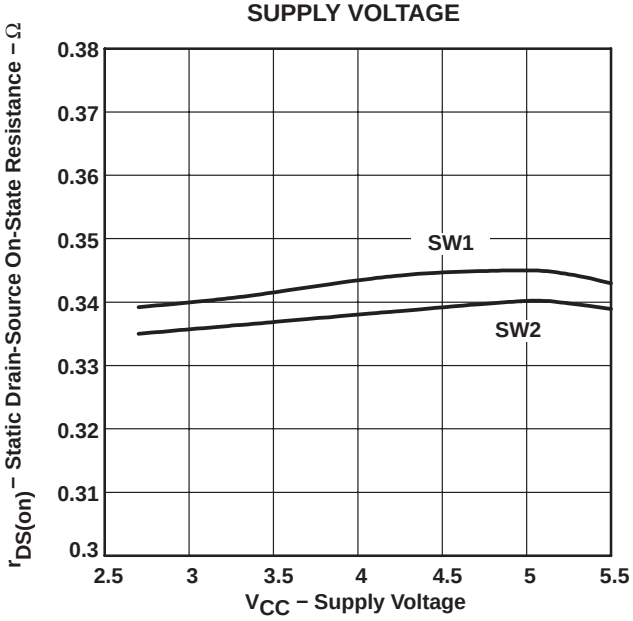


Figure 14

SHORT CIRCUIT CURRENT
vs
JUNCTION TEMPERATURE

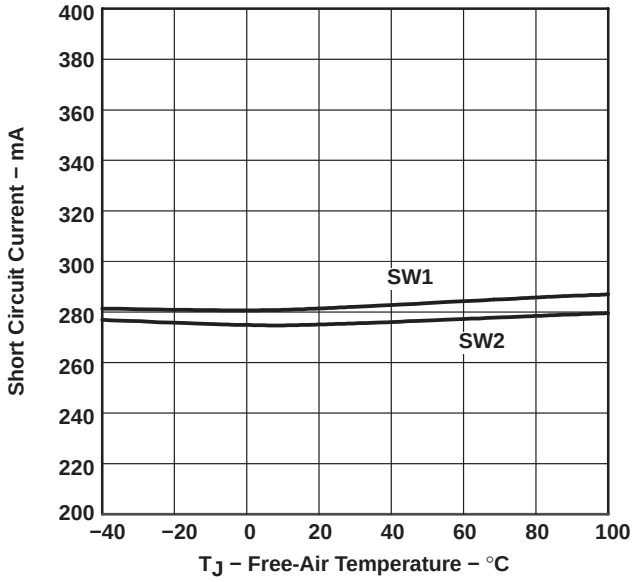


Figure 15

SHORT CIRCUIT CURRENT
vs
SUPPLY VOLTAGE

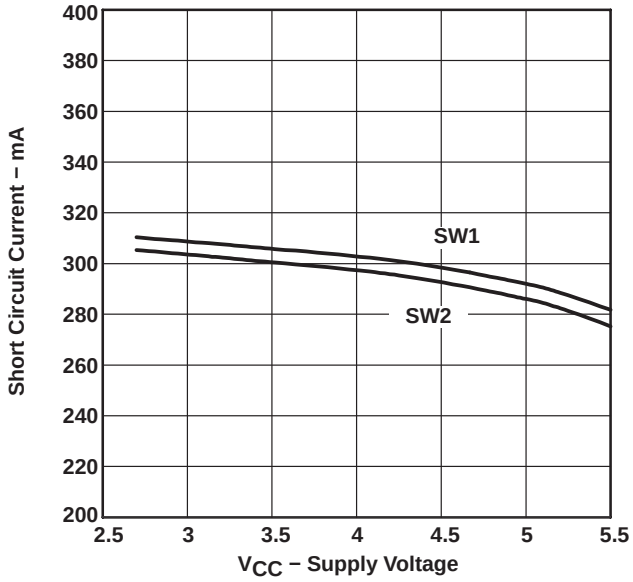


Figure 16

TYPICAL CHARACTERISTICS

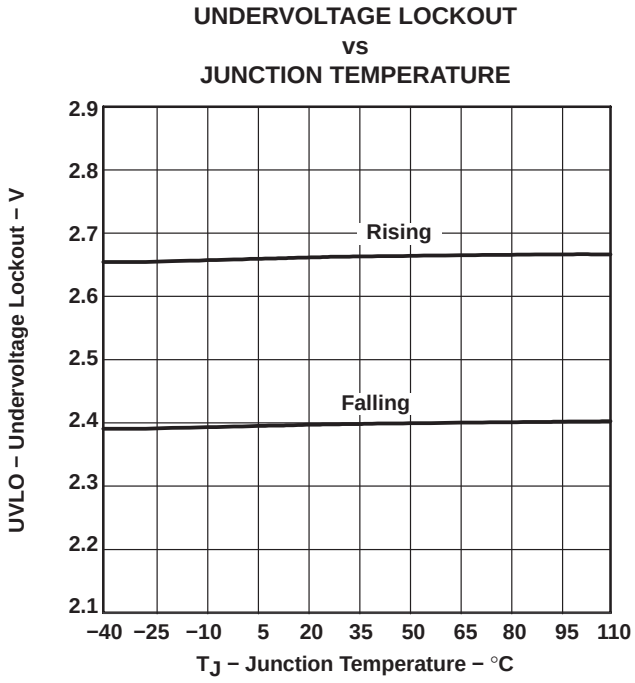


Figure 17

APPLICATION INFORMATION

external capacitor requirements on power lines

Ceramic bypass capacitors (0.01-μ to 0.1-μ) between VIN/SWIN1 and GND and SWIN2 and GND, close to the device, are recommended to improve load transient response and noise rejection.

Bulk capacitors (4.7-μF) between VIN/SWIN1 and GND and between SWIN2 and GND are also recommended, especially if load transients in the hundreds of milliamps with fast rise times are anticipated.

A 66-μF bulk capacitor is recommended from OUTx to ground, especially when the output load is heavy. This precaution helps reduce transients seen on the power rails. Additionally, bypassing the outputs with a 0.1-μF ceramic capacitor improves the immunity of the device to short-circuit transients.

LDO output capacitor requirements

Stabilizing the internal control loop requires an output capacitor connected between LDO_OUT and GND. The minimum recommended capacitance is a 4.7 μF with an ESR value between 200 mΩ and 10 Ω. Solid tantalum electrolytic, aluminum electrolytic and multilayer ceramic capacitors are all suitable, provided they meet the ESR requirements.

The adjustable LDO (for voltages lower than 3 V) requires a bypass capacitor across the feedback resistor as shown in Figure 18. The value of this capacitor is determined by using the following equation:

$$C_f = \frac{1}{(63.7e^3 \times 2 \times 3.14 \times R1)} - 4\ \text{pf} \quad (1)$$

where R1 is derived by programming the adjustable LDO (see programming the adjustable LDO regulator section shown below).

APPLICATION INFORMATION

programming the adjustable LDO regulator

The output voltage of the TPS2145 adjustable regulator is programmed using an external resistor divider as shown in Figure 18. The output voltage is calculated using:

$$\text{LDO\_OUT} = V_{ref}\left(1 + \frac{R1}{R2}\right) \quad (2)$$

where V_{ref} = 0.8 V typical (internal reference voltage).

Resistors R1 and R2 should be chosen for approximately 4-μA (minimum) divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as a minimum load is required to sink the LDO forward leakage and maintain regulation. The recommended design procedure is to choose R2 = 200 kΩ to set the divider current at 4-μA and then solve the LDO_OUT equation for R1.

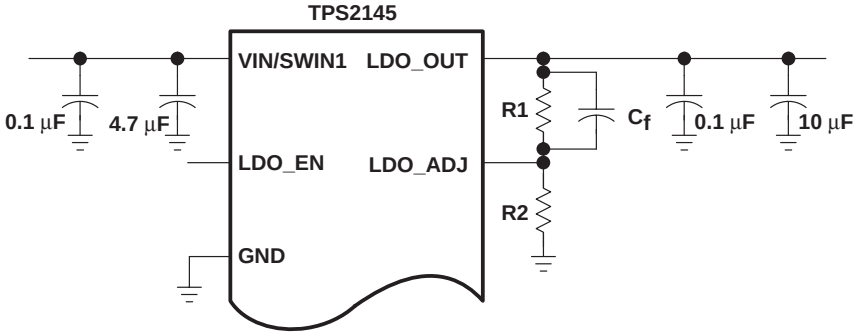


Figure 18. External Resistor Divider

OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	Cfb
3.3	625 kΩ	200 kΩ	NR†
3.0	550 kΩ	200 kΩ	NR†
2.5	425 kΩ	200 kΩ	2 pf
1.8	250 kΩ	200 kΩ	6 pf
1.5	175 kΩ	200 kΩ	10.3 pf
1.0	50 kΩ	200 kΩ	46 pf

† NR − Not required

overcurrent

A sense FET is used to measure current through the device. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output is shorted before the device is enabled or before VIN has been applied. The TPS2145 and TPS2147 sense the short and immediately switch to a constant-current output.

In the second condition, the short occurs while the device is enabled. At the instant the short occurs, very high currents may flow for a very short time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshold), the device switches into constant-current mode.

APPLICATION INFORMATION

overcurrent (continued)

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded. The TPS2145 and TPS2147 are capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

$\overline{OC}$ response

The $\overline{OCx}$ open-drain output is asserted (active low) when an overcurrent condition is encountered. The output will remain asserted until the overcurrent condition is removed. Connecting a heavy capacitive load to an enabled device can cause momentary false overcurrent reporting from the inrush current flowing through the device, charging the downstream capacitor. The TPS2145 and TPS2147 are designed to reduce false overcurrent reporting. An internal overcurrent transient filter eliminates the need for external components to remove unwanted pulses. Using low-ESR electrolytic capacitors on OUTx lowers the inrush current flow through the device during hot-plug events by providing a low-impedance energy source, also reducing erroneous overcurrent reporting.

power dissipation and junction temperature

The major source of power dissipation for the TPS2145 and TPS2147 comes from the internal voltage regulator and the N-channel MOSFETs. Checking the power dissipation and junction temperature is always a good design practice and it starts with determining the $r_{DS(on)}$ of the N-channel MOSFET according to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from the graphs shown in the Typical Characteristics section of this data sheet. Using this value, the power dissipation per switch can be calculated using:

$$P_D = r_{DS(on)} \times I^2 \quad (3)$$

Multiply this number by two to get the total power dissipation coming from the N-channel MOSFETs.

The power dissipation for the internal voltage regulator is calculated using:

$$P_D = \left(V_I - V_{O(min)}\right) \times I_O \quad (4)$$

The total power dissipation for the device becomes:

$$P_{D(total)} = P_{D(\text{voltage regulator})} + \left(2 \times P_{D(switch)}\right) \quad (5)$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A \quad (6)$$

Where:

T_A = Ambient Temperature °C

$R_{\theta JA}$ = Thermal resistance °C/W, equal to inverting the derating factor found on the power dissipation table in this data sheet.

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

APPLICATION INFORMATION

thermal protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force the TPS2145 and TPS2147 into constant-current mode at first, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels.

The protection circuit senses the junction temperature of the switch and shuts it off. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 10 degrees, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed.

The TPS2145 and TPS2147 implement a dual thermal trip to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition, the junction temperature will rise. Once the die temperature rises to approximately 120°C, the internal thermal-sense circuitry checks to determine which power switch is in an overcurrent condition and turns that power switch off, thus isolating the fault without interrupting operation of the adjacent power switch. Should the die temperature exceed the first thermal trip point of 120°C and reach 155°C, the device will turn off.

undervoltage lockout (UVLO)

An undervoltage lockout ensures that the device (LDO and switches) is in the off state at power up. The UVLO will also keep the device from being turned on until the power supply has reached the start threshold (see undervoltage lockout table), even if the switches are enabled. The UVLO will also be activated whenever the input voltage falls below the stop threshold as defined in the undervoltage lockout table. This function facilitates the design of hot-insertion systems where it is not possible to turn off the power switches before input power is removed. Upon reinsertion, the power switches will be turned on with a controlled rise time to reduce EMI and voltage overshoots.

universal serial bus (USB) applications

The universal serial bus (USB) interface is a multiplexed serial bus operating at either 12-Mb/s, or 1.5-Mb/s for USB 1.1, or 480 Mb/s for USB 2.0. The USB interface is designed to accommodate the bandwidth required by PC peripherals such as keyboards, printers, scanners, and mice. The four-wire USB interface was conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3-V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts/self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

The TPS2145 and TPS2147 are well suited for USB hub and peripheral applications. The internal LDO can be used to provide the 3.3-V power needed by the controller while the dual switches distribute power to the downstream functions.

APPLICATION INFORMATION

USB power-distribution requirements

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power-distribution features must be implemented.

- Hosts/self-powered hubs must:
  - Current-limit downstream ports
  - Report overcurrent conditions on USB V_{BUS}
- Bus-powered hubs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44 Ω and 10 μF)
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA

The feature set of the TPS2145 and TPS2147 allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-powered hubs, as well as the input ports for bus-powered functions.

USB applications

Figure 19 shows the TPS2147 being used in a USB bus-powered/self-powered peripheral design. The internal 3.3-V LDO is used to provide power for the USB function controller as well as to the 1.5-kΩ pullup resistor.

In bus-powered mode, switch 1 provides power to the 5-V circuitry. In self-powered mode, switch 2 provides power to the 5-V circuitry while the USB 5-V still provides power to the 3.3-V LDO (USB allows self-powered devices to draw up to 100 mA from V_{BUS}).

APPLICATION INFORMATION

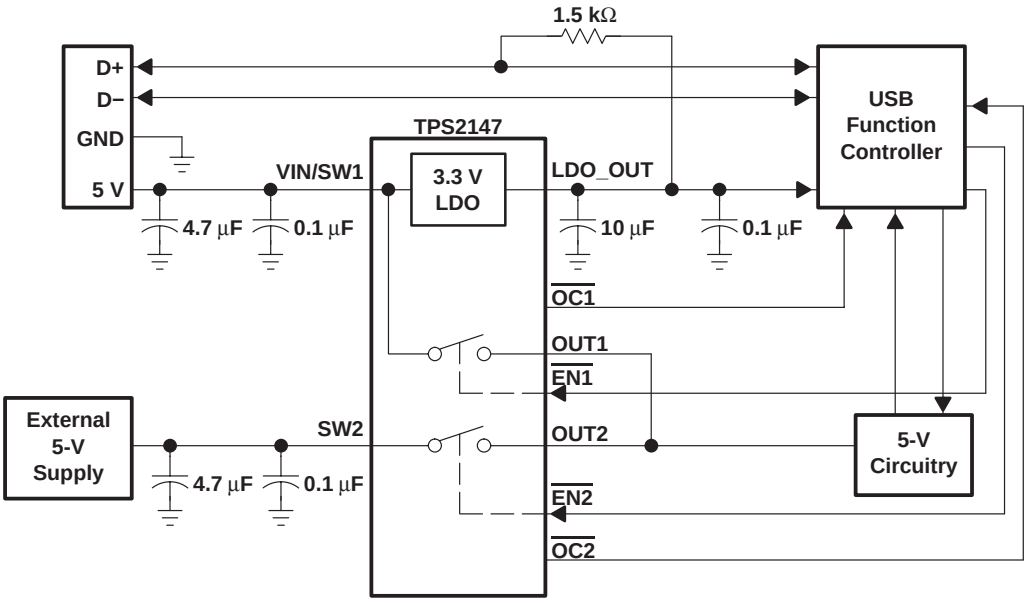


Figure 19. TPS2147 USB Bus-Powered/Self-Powered Peripheral Application

DSP applications

Figure 20 shows the TPS2145 in a DSP application. DSPs use a 1.8-V core voltage and a 3.3-V I/O voltage. In this type of application, the TPS2145 adjustable LDO is configured for a 1.8-V output specifically for the DSP core voltage.

The additional 3.3-V circuitry is powered through switch 1 of the TPS2145 only after the DSP is up and running. Switch 2 is used to provide power to additional circuitry operating from a different voltage source. This switch is also controlled by the DSP.

Figures 21 thru 23 show the TPS2145 in various DSP applications using a supply voltage supervisor (SVS) chip to control the enable for the 3.3 V powering up the DSP I/O circuitry.

APPLICATION INFORMATION

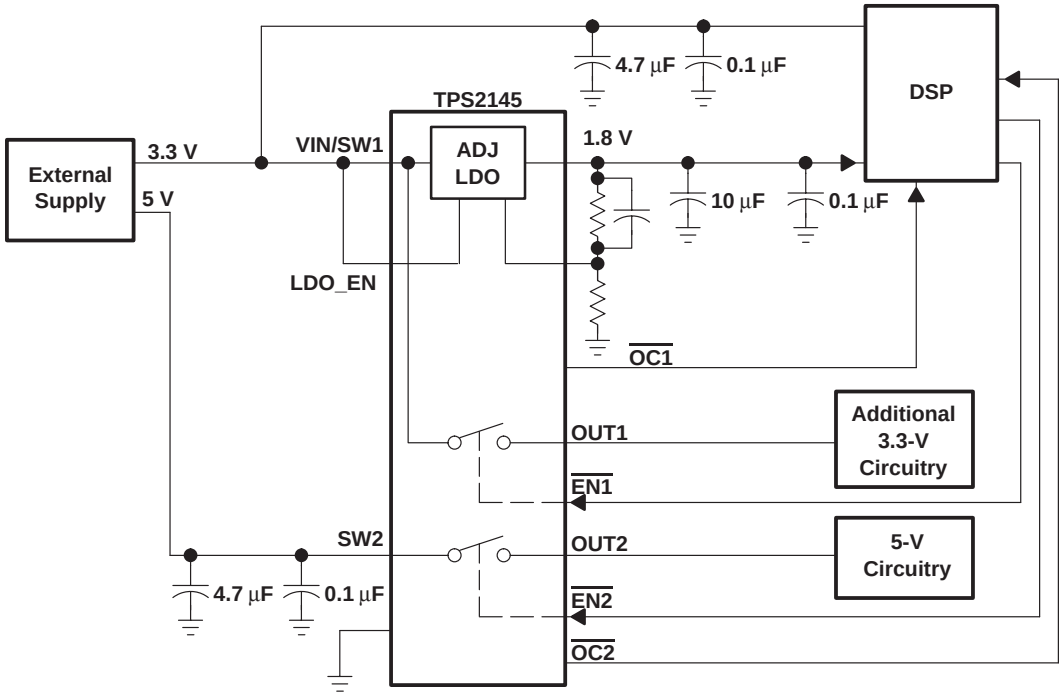


Figure 20. TPS2145 DSP Application

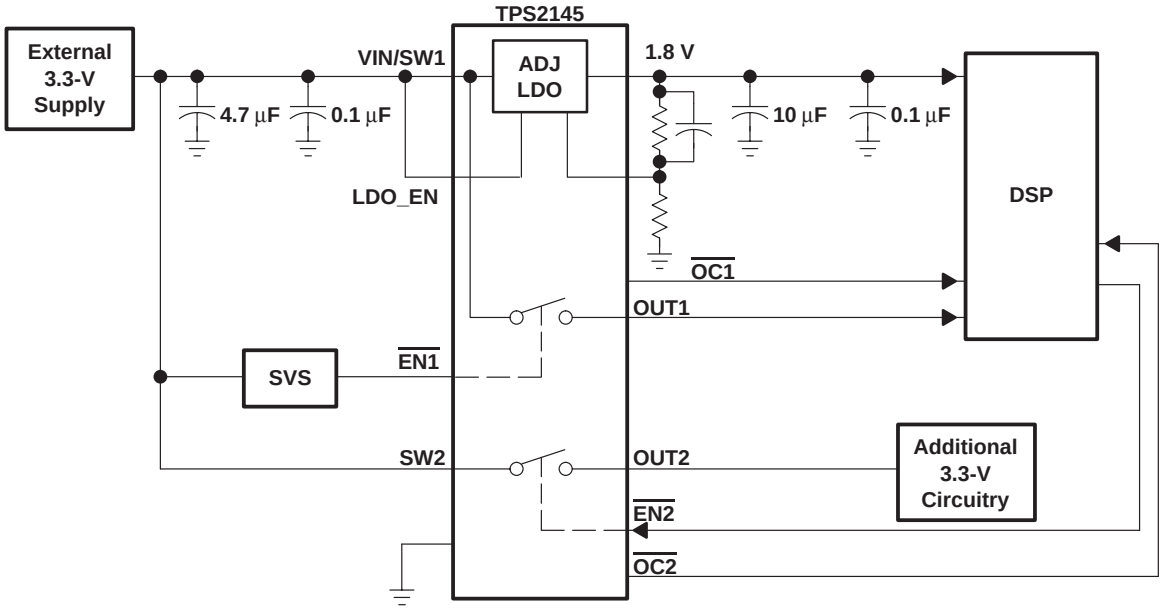


Figure 21. TPS2145 DSP With SVS Application

APPLICATION INFORMATION

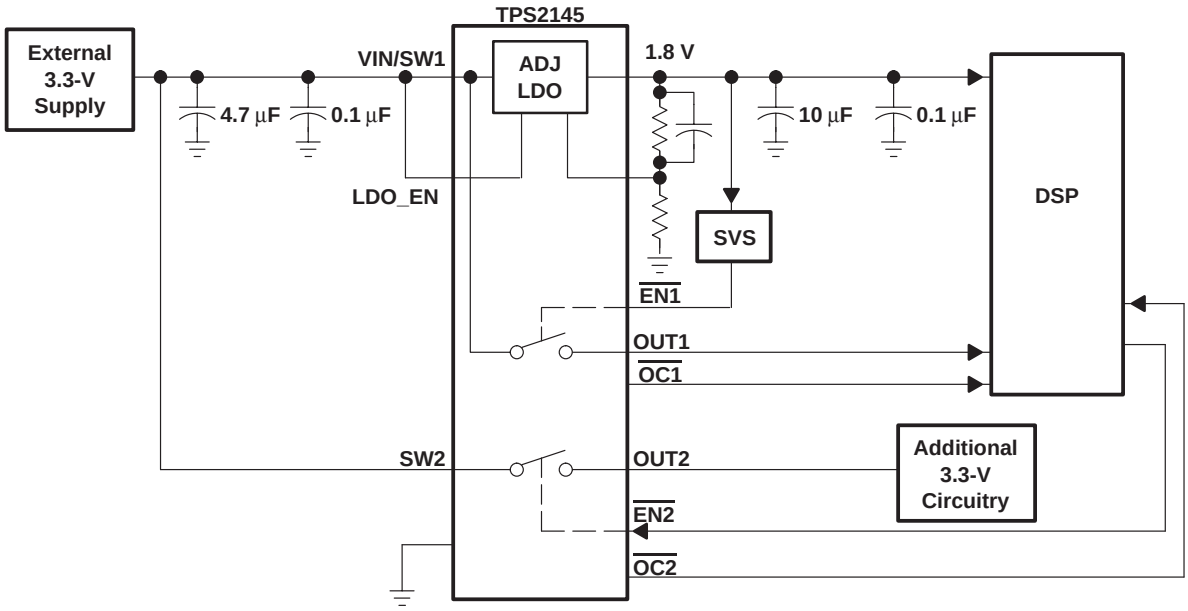


Figure 22. TPS2145 DSP With SVS Application

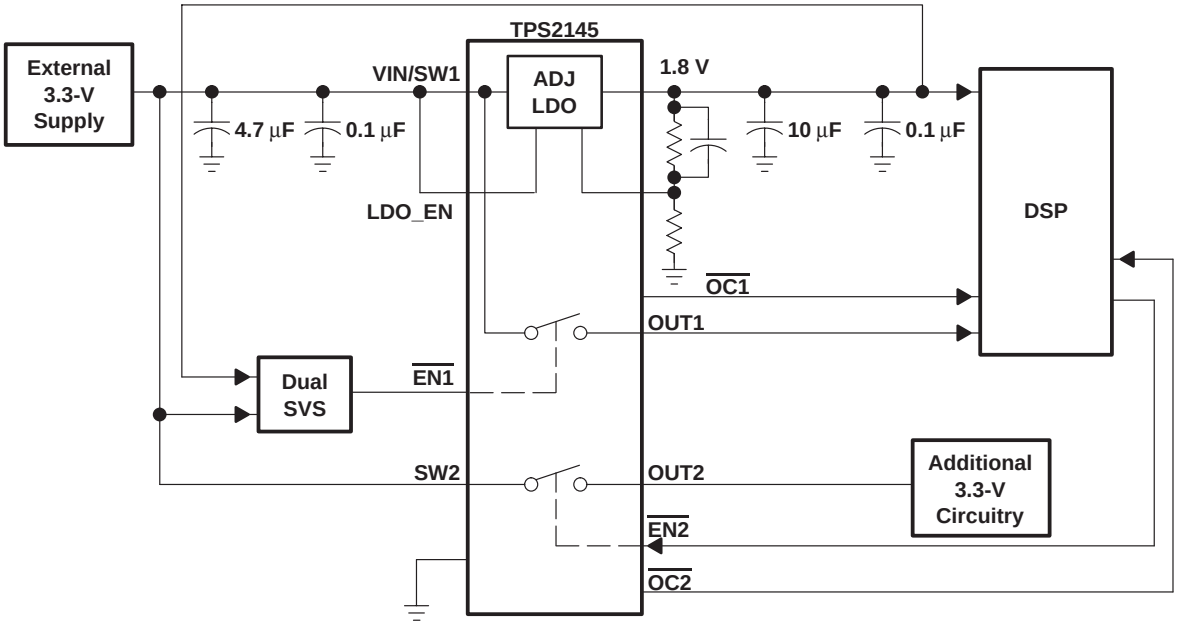


Figure 23. TPS2145 DSP With Dual SVS Application

APPLICATION INFORMATION

power supply sequencing

DSPs typically do not require specific power sequencing between the core supply and the I/O supply. However, systems should be designed to ensure that neither supply is powered up for extended periods of time if the other supply is below the proper operating voltage.

system level design consideration

System level design considerations, such as bus contention, may require supply sequencing to be implemented. In this case, the core supply should be powered up at the same time as, or prior to (and powered down after), the I/O buffers. This is to ensure that the I/O buffers receive valid inputs from the core before the output buffers are powered up, thus, preventing bus contention with other chips on the board.

power supply design consideration

For some DSP systems, the core supply may be required to provide a considerable amount of current until the I/O supply is powered up. This extra current condition is a result of uninitialized logic within the DSP(s). Decreasing the amount of time between the core supply power up and the I/O supply power up can minimize the effects of this current draw.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS2145IPWP	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD2145I	Samples
TPS2145IPWPG4	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD2145I	Samples
TPS2145IPWPR	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD2145I	Samples
TPS2145IPWPRG4	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD2145I	Samples
TPS2147IDGQ	ACTIVE	MSOP-PowerPAD	DGQ	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AWL	Samples
TPS2147IDGQG4	ACTIVE	MSOP-PowerPAD	DGQ	10	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AWL	Samples
TPS2147IDGQR	ACTIVE	MSOP-PowerPAD	DGQ	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AWL	Samples
TPS2147IDGQRG4	ACTIVE	MSOP-PowerPAD	DGQ	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AWL	Samples
TPS2155IPWP	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD2155I	Samples
TPS2155IPWPG4	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PD2155I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

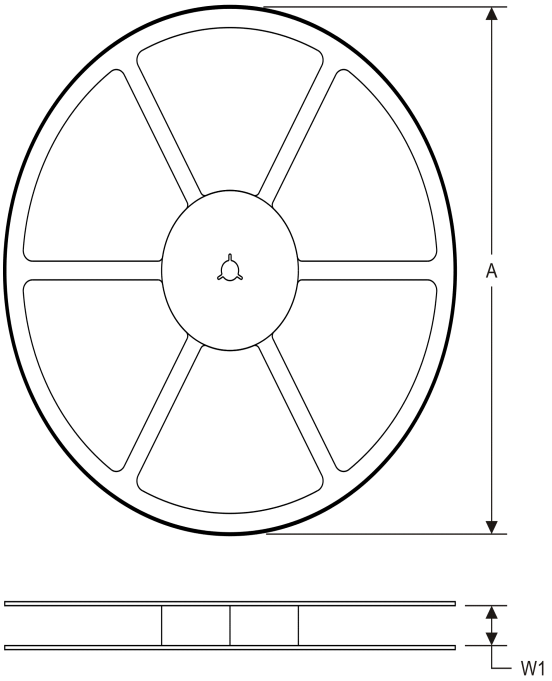
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

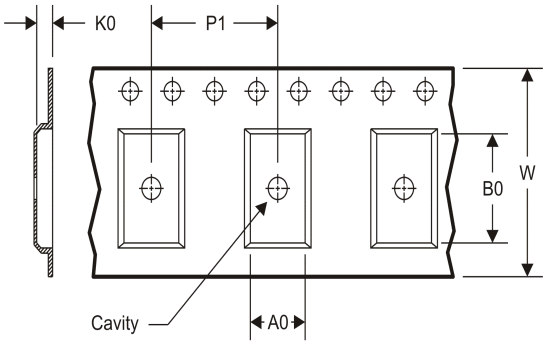
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



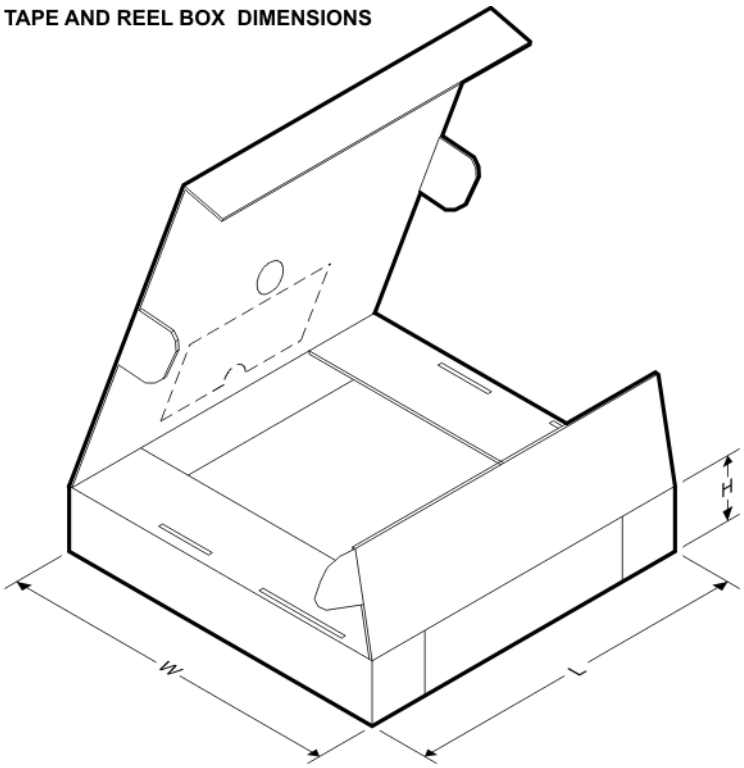
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2145IPWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS2147IDGQR	MSOP-Power PAD	DGQ	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

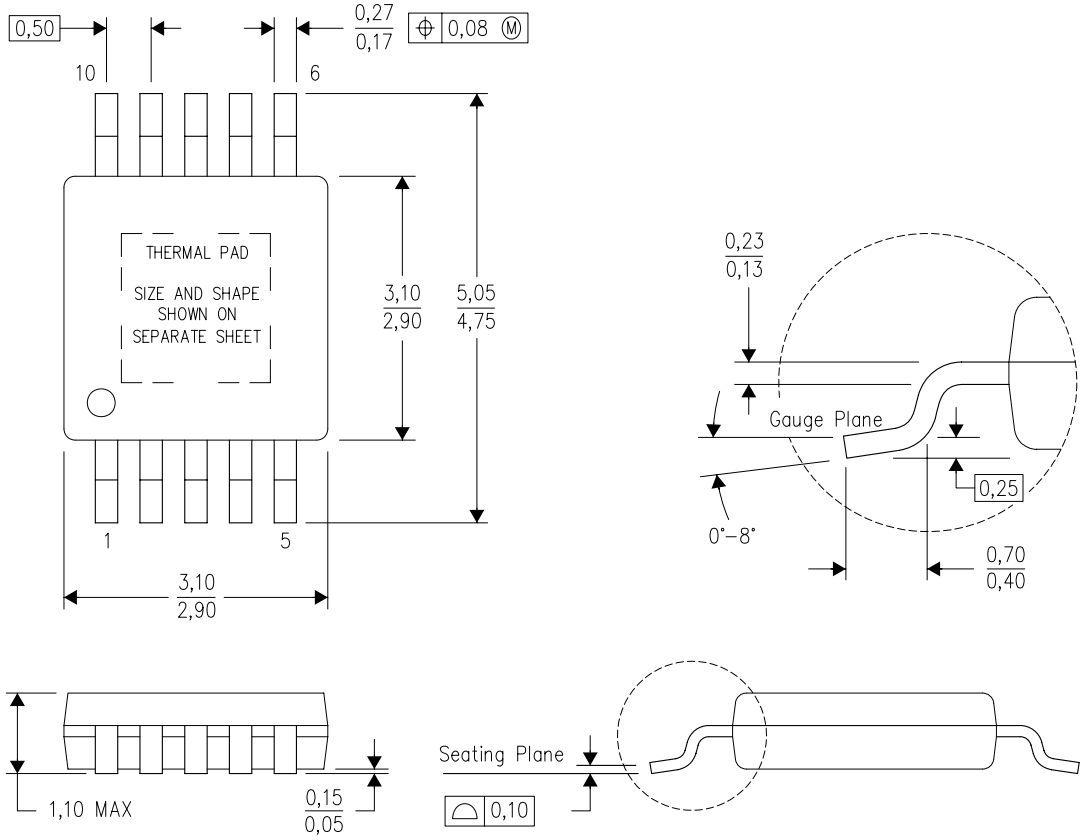
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2145IPWPR	HTSSOP	PWP	14	2000	367.0	367.0	35.0
TPS2147IDGQR	MSOP-PowerPAD	DGQ	10	2500	358.0	335.0	35.0

DGQ (S–PDSO–G10) PowerPAD™ PLASTIC SMALL OUTLINE



4073273/F 11/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation BA–T.

PowerPAD is a trademark of Texas Instruments.

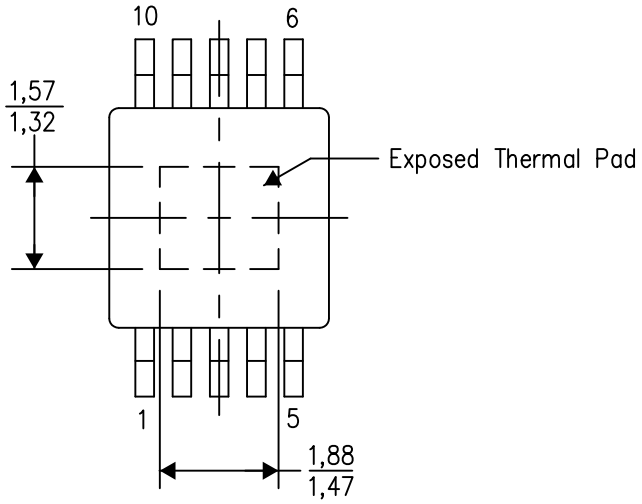
DGQ (S–PDSO–G10) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

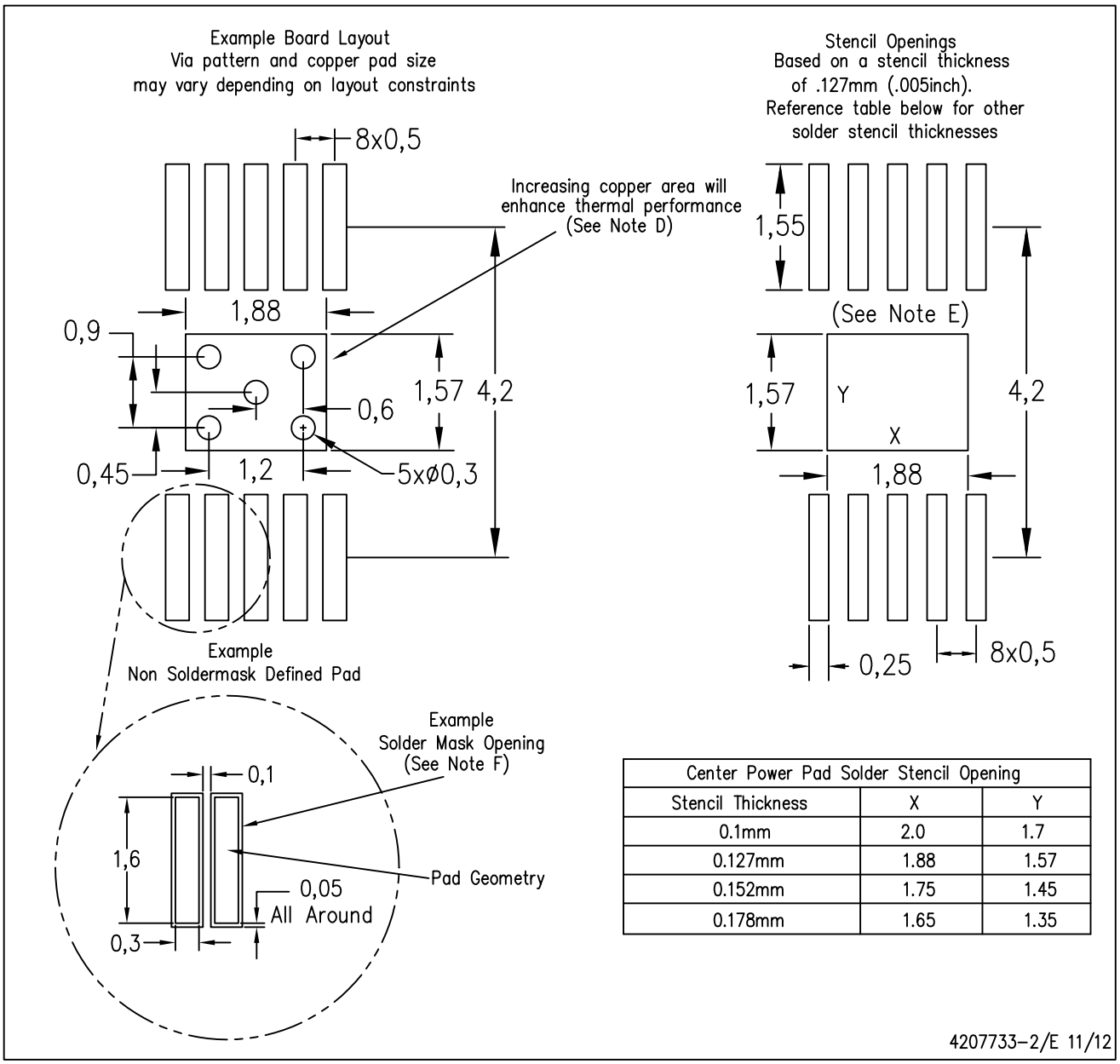
Exposed Thermal Pad Dimensions

4206324–2/G 05/13

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

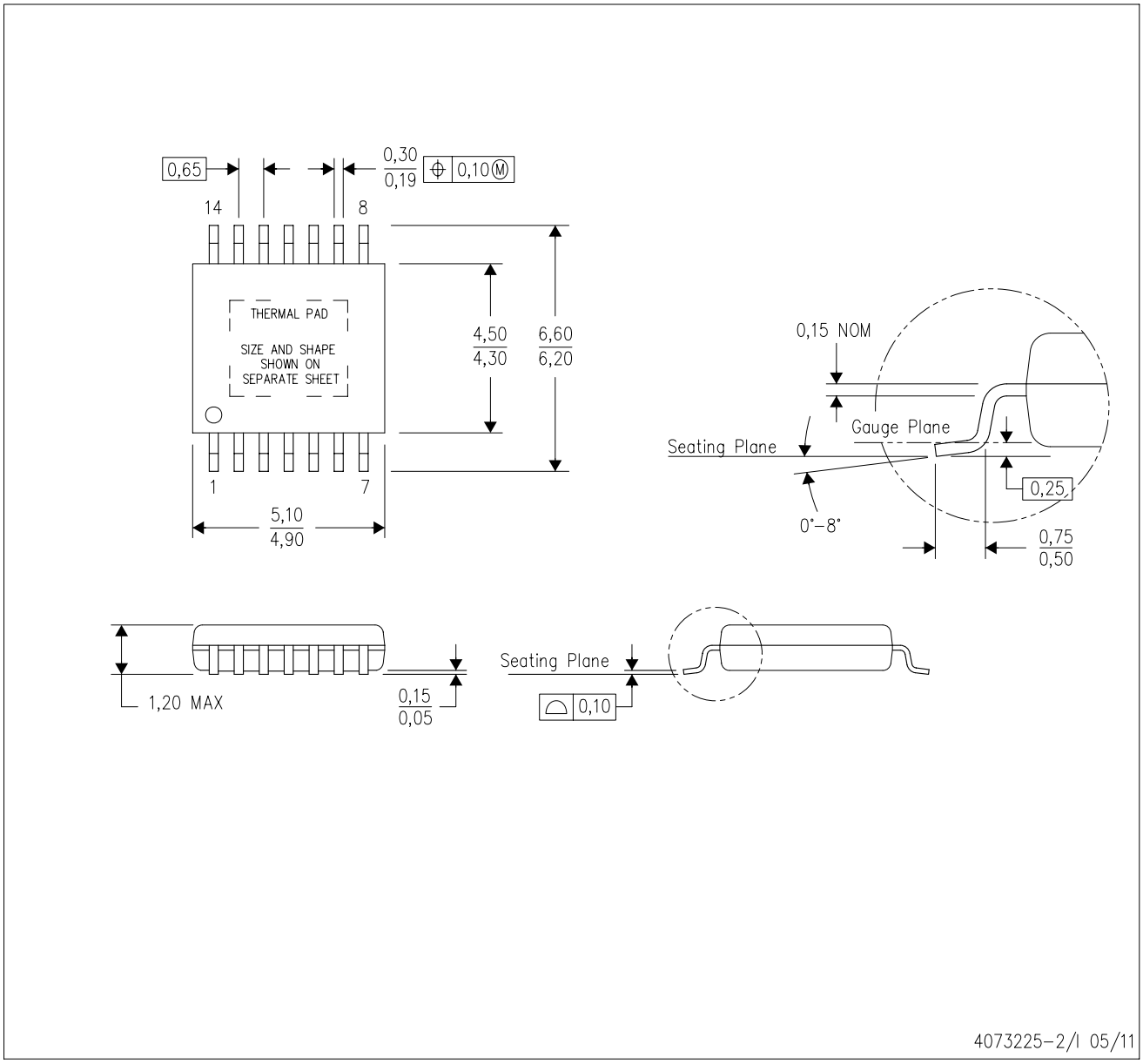
DGQ (S–PDSO–G10) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.88	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

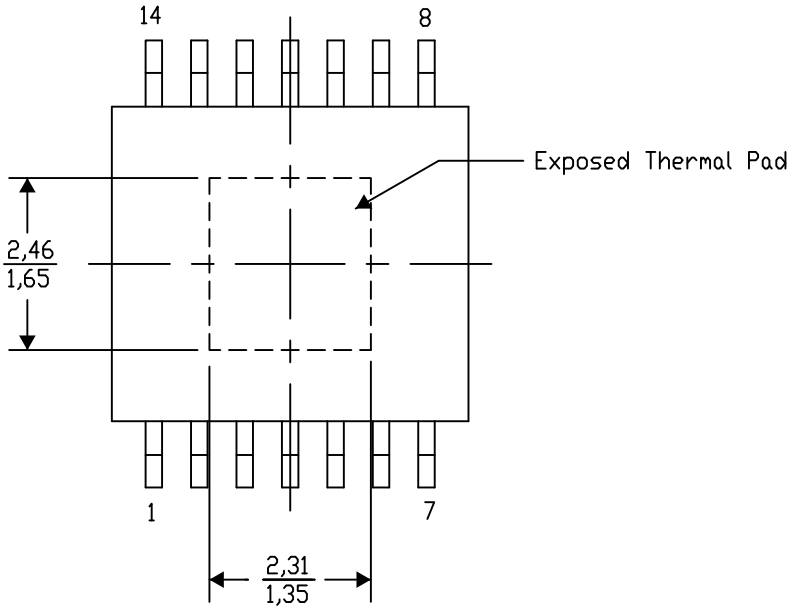
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

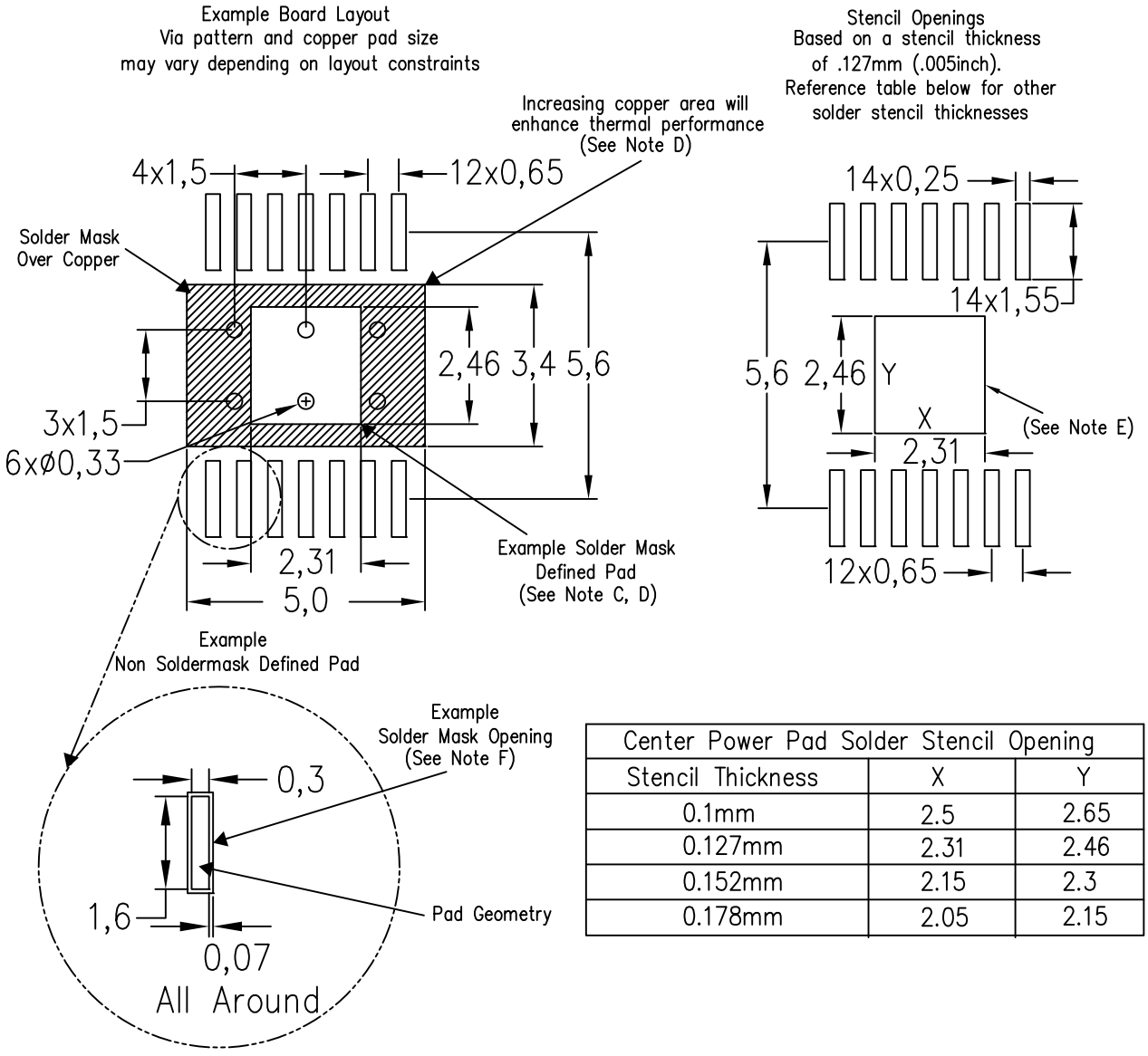
Exposed Thermal Pad Dimensions

4206332–2/AG 08/13

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–2/T 08/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

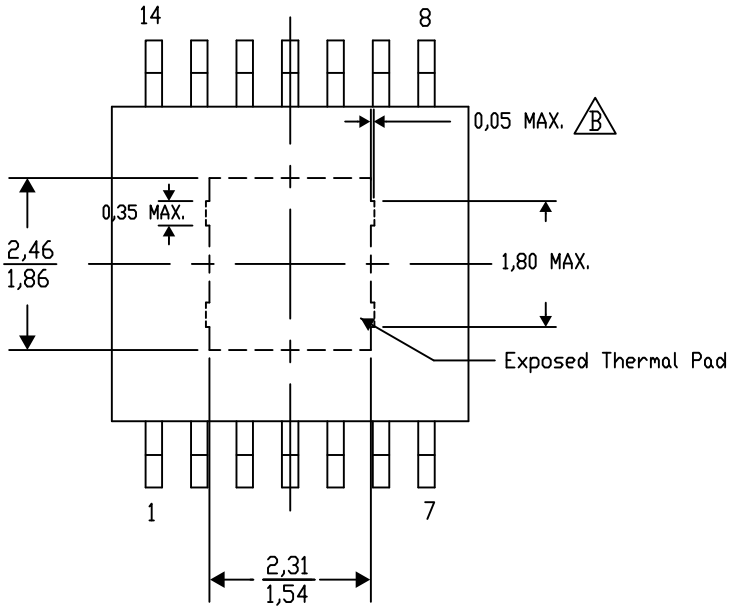
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–44/AG 08/13

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

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