To all our customers

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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HD74HC299

8-bit Universal Shift/Storage Register (with 3-state outputs)

ADE-205-488 (Z)
1st. Edition
Sep. 2000

Description

The HD74HC299 features multiplexed inputs/outputs to achieve full 8-bit data handling in a single 20-pin package. Due to the large output drive capability and 3-state feature, this device is ideally suited for interfacing with bus lines in a bus oriented system. Two function select inputs and two output control inputs are used to choose the mode of operation as listed in the function table. Synchronous parallel loading is accomplished by taking both function select lines S_0 and S_1 high. This places the 3-state outputs in a high impedance state, which permits data applied to the input/output lines to be clocked into the register. Reading out of the register can be done while the outputs are enabled in any mode. A direct overriding clear input is provided to clear the register whether the outputs are enabled or disabled.

Features

- High Speed Operation
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 2 to 6 V
- Low Input Current: 1 μA max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μA max (Ta = 25°C)

Function Table

	Inputs																	
		Function Select		Output Control			Serial		Inputs/Outputs								Outputs	
Mode	Clear	S_1	S_0	$\overline{G}_1$†	$\overline{G}_2$†	Clock	S_L	S_R	A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	Q_A'	Q_H'
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift	H	L	H	L	L	⎍	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
Right	H	L	H	L	L	⎍	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift	H	H	L	L	L	⎍	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
Left	H	H	L	L	L	⎍	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	⎍	X	X	a	b	c	d	e	f	g	h	a	h

Notes: 1. a to h; the level of steady-state input at inputs A through H, respectively. These data are loaded into the flip-flop outputs are isolated from the input/output terminals.

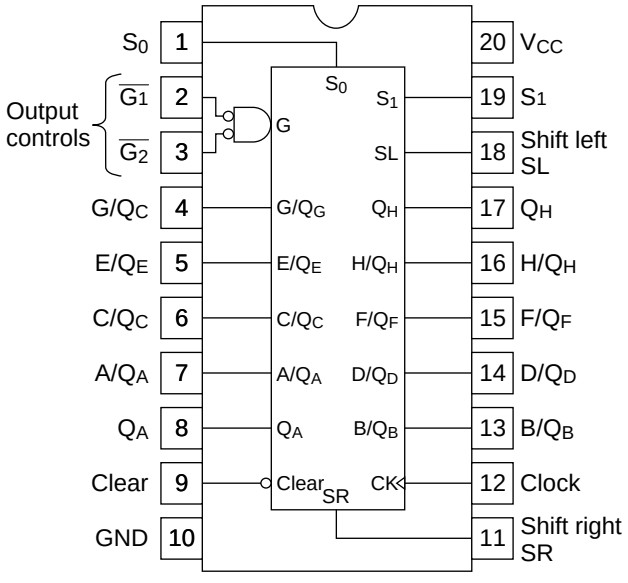
2. Q_{A0} to Q_{H0}; the level of Q_A through Q_H, respectively, before the indicated steady-state input conditions were established.

3. Q_{An} to Q_{Hn}; the level of Q_A through Q_H, respectively, before the most-recent ⎍ transition of the clock.

4. † = ; When one or both output controls are high the eight input/output terminals are desabled to the high-impedance state, however, sequential operation or clearing of the register is not affected.

5. When clear is low, outputs of Q_A' and Q_H' are low, in spite of other inputs.

Pin Arrangement

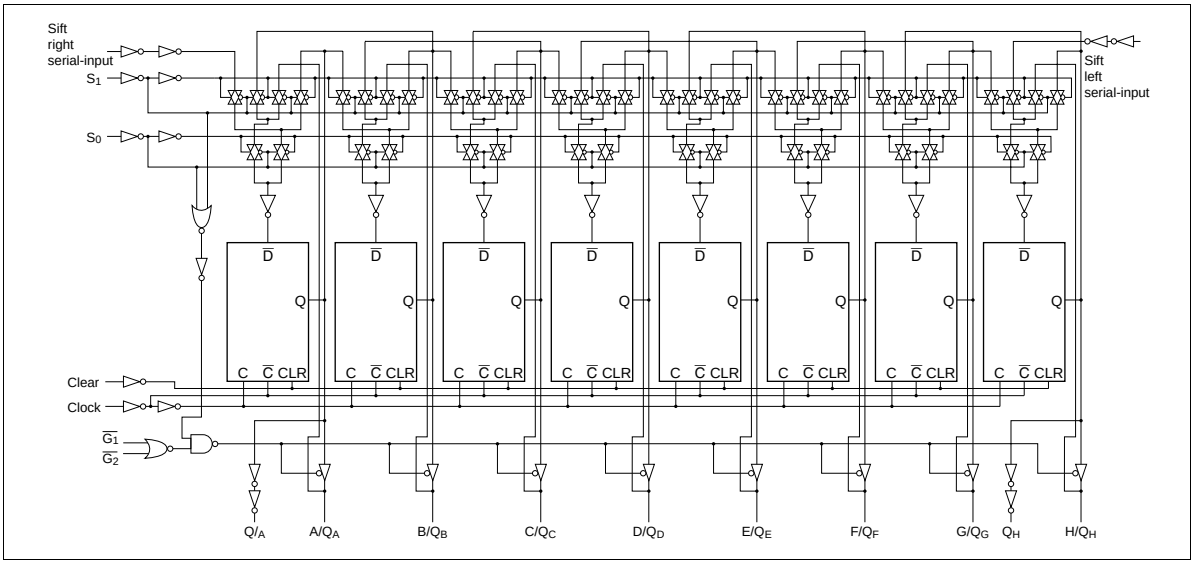


(Top view)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage range	V_{CC}	–0.5 to +7.0	V
Input voltage	V_{IN}	–0.5 to V_{CC} + 0.5	V
Output voltage	V_{OUT}	–0.5 to V_{CC} + 0.5	V
Output current	I_{OUT}	±35	mA
DC current drain per V_{CC}, GND	I_{CC}, I_{GND}	±75	mA
DC input diode current	I_{IK}	±20	mA
DC output diode current	I_{OK}	±20	mA
Power dissipation per package	P_T	500	mW
Storage temperature	Tstg	–65 to +150	°C

Block Diagram



DC Characteristics

Item	Symbol	V_{CC} (V)	Ta = 25°C Min	Typ	Max	Ta = –40 to +85°C Min	Max	Unit	Test Conditions	
Input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V_{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V_{IH} or V_{IL}	I_{OH} = –20 µA
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—		Q_A' & Q_H'	I_{OH} = –4 mA
		6.0	5.68	—	—	5.63	—		Outputs	I_{OH} = –5.2 mA
		4.5	4.18	—	—	4.13	—		A/Q_A thru	I_{OH} = –6 mA
		6.0	5.68	—	—	5.63	—		H/Q_H Outputs	I_{OH} = –7.8 mA
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V_{IH} or V_{IL}	I_{OL} = 20 µA
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33		Q_A' & Q_H'	I_{OH} = 4 mA
		6.0	—	—	0.26	—	0.33		Outputs	I_{OH} = 5.2 mA
		4.5	—	—	0.26	—	0.33		A/Q_A thru	I_{OH} = 6 mA
		6.0	—	—	0.26	—	0.33		H/Q_H Outputs	I_{OH} = 7.8 mA
Off-state output current	I_{OZ}	6.0	—	—	±0.5	—	±5.0	µA	Vin = V_{IH} or V_{IL}, Vout = V_{CC} or GND	
Input current	Iin	6.0	—	—	±0.1	—	±1.0	µA	Vin = V_{CC} or GND	
Quiescent supply current	I_{CC}	6.0	—	—	4.0	—	40	µA	Vin = V_{CC} or GND, Iout = 0 µA	

AC Characteristics (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

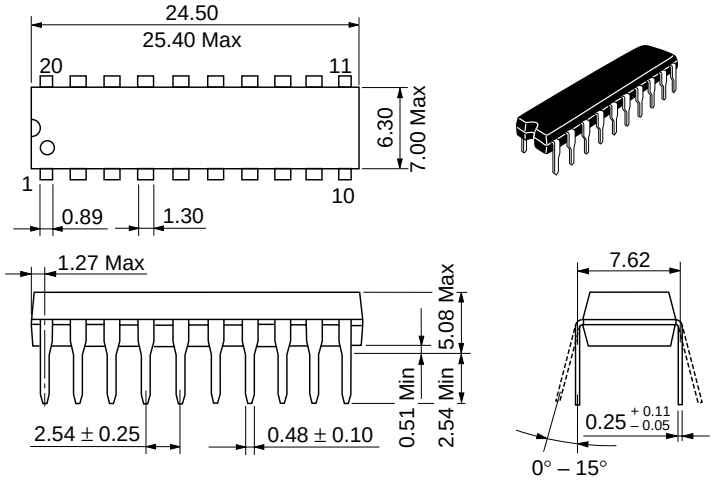
			Ta = 25°C			Ta = –40 to +85°C			
Item	**Symbol**	**V_{cc} (V)**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Maximum clock frequency	f_{max}	2.0	—	—	5	—	4	MHz	
		4.5	—	—	25	—	20		
		6.0	—	—	29	—	23		
Propagation delay time	t_{PLH} t_{PHL}	2.0	—	—	190	—	240	ns	Clock to Q_A' or Q_H'
		4.5	—	—	38	—	48		
		6.0	—	—	32	—	41		
	t_{PHL}	2.0	—	—	220	—	275	ns	Clear to Q_A' or Q_H'
		4.5	—	—	44	—	55		
		6.0	—	—	37	—	47		
	t_{PLH} t_{PHL}	2.0	—	—	190	—	240	ns	Clock to Q_A – Q_H
		4.5	—	—	38	—	48		
		6.0	—	—	32	—	41		
	t_{PHL}	2.0	—	—	220	—	275	ns	Clear to Q_A – Q_H
		4.5	—	—	44	—	55		
		6.0	—	—	37	—	47		
Output enable time	t_{ZH} t_{ZL}	2.0	—	—	160	—	200	ns	
		4.5	—	—	32	—	40		
		6.0	—	—	27	—	34		
Output disable time	t_{HZ} t_{LZ}	2.0	—	—	160	—	200	ns	
		4.5	—	—	32	—	40		
		6.0	—	—	27	—	34		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	Select
		4.5	20	—	—	25	—		
		6.0	17	—	—	21	—		
Hold time	t_h	2.0	5	—	—	5	—	ns	Select
		4.5	5	—	—	5	—		
		6.0	5	—	—	5	—		
Removal time	t_{rem}	2.0	50	—	—	65	—	ns	Clear
		4.5	10	—	—	13	—		
		6.0	9	—	—	11	—		
Pulse width	t_w	2.0	80	—	—	100	—	ns	
		4.5	16	—	—	20	—		
		6.0	14	—	—	17	—		

AC Characteristics (C_L = 50 pF, Input t_r = t_f = 6 ns) (cont)

			Ta = 25°C			Ta = –40 to +85°C			
Item	**Symbol**	**V_{cc} (V)**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Output rise/fall time	t_{TLH}	2.0	—	—	60	—	75	ns	A/Q_A thru H/Q_H outputs
	t_{THL}	4.5	—	—	12	—	15		
		6.0	—	—	10	—	13		
		2.0	—	—	75	—	95	ns	Q_A' & Q_H' outputs
		4.5	—	—	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	Cin	—	—	5	10	—	10	pF	

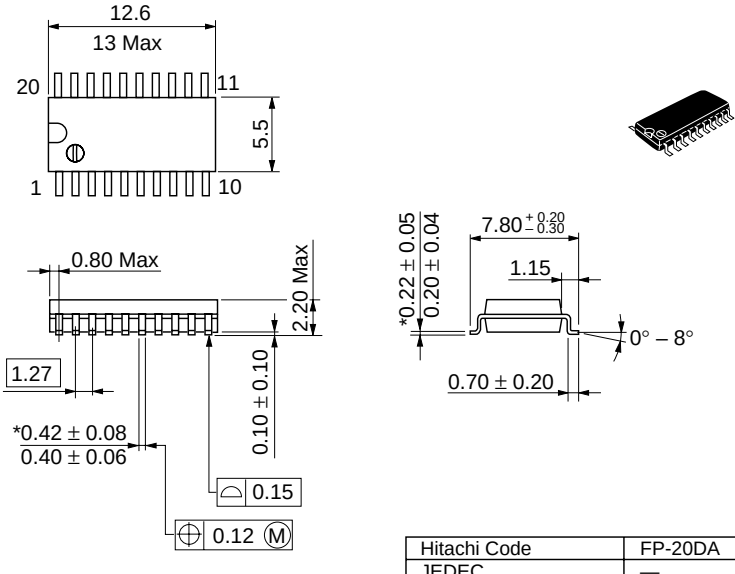
Package Dimensions

Unit: mm



Hitachi Code	DP-20N
JEDEC	—
EIAJ	Conforms
Mass (reference value)	1.26 g

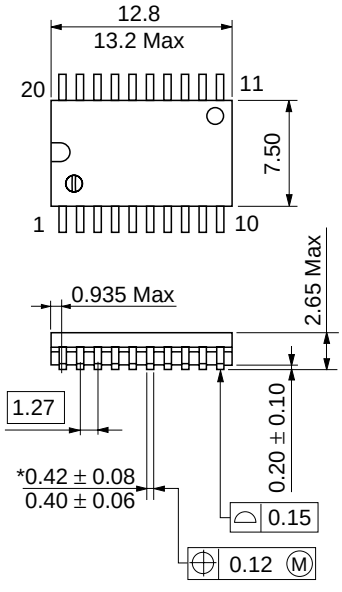
Unit: mm

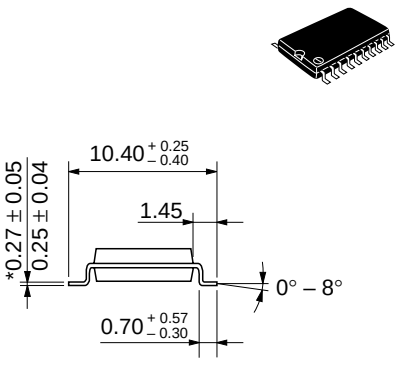


*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.31 g

Unit: mm





*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DB
JEDEC	Conforms
EIAJ	—
Mass (reference value)	0.52 g

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