CS5451

Six-Channel Delta-Sigma Analog-to-Digital Converter

Features

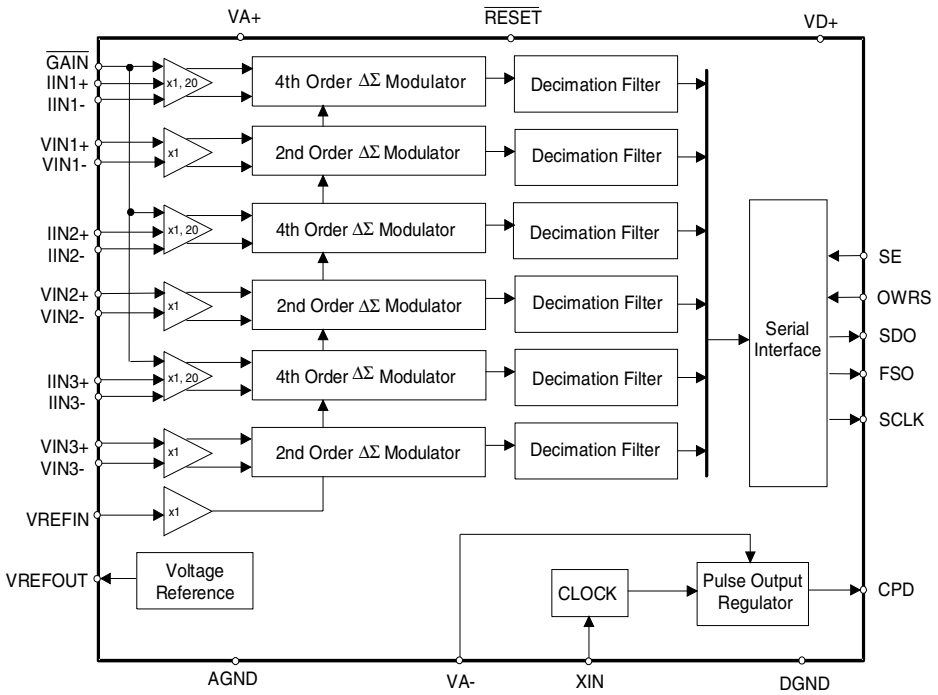
- Synchronous Sampling
- On-chip 1.2 V Reference (25 ppm/°C typ)
- Power Supply Configurations:
  - VA+ = +3 V; VA- = -2 V; VD+ = +3 V
  - Supply tolerances ±10%
- Power Consumption
  - 20 mW Typical at VD+ = +3 V
- Simple Four-wire Serial Interface
- Charge Pump Driver output generates negative power supply.
- Ground-Referenced Bipolar Inputs

Description

The CS5451 is a highly integrated Delta-Sigma (ΔΣ) Analog-to-Digital Converter (ADC) developed for the Power Measurement Industry. The CS5451 combines six ΔΣ ADCs, decimation filters, and a serial interface on a single chip. The CS5451 interfaces directly to a current transformer or shunt to measure current, and resistive divider or transformer to measure voltage. The product features a serial interface for communication with a micro-controller or DSP. The product is initialized and fully functional upon reset, and includes a Voltage Reference.

ORDERING INFORMATION:

CS5451-BS	-40°C to +85°C	28-pin SSOP



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

CIRRUS LOGIC
P.O. Box 17847, Austin, Texas 78760
(512) 445 7222 FAX: (512) 445 7581
http://www.cirrus.com

TABLE OF CONTENTS

LIST OF FIGURES

Contacting Cirrus Logic Support
For a complete listing of Direct Sales, Distributor, and Sales Representative contacts, visit the Cirrus Logic web site at:
http://www.cirrus.com/corporate/contacts/

1. CHARACTERISTICS AND SPECIFICATIONS

ANALOG CHARACTERISTICS (T_A = -40 °C to +85 °C; +2.7V < VA+ < +3.5V; +2.7V < VD+ < +3.5V; VA- = -2 V ±10%; External VREF+ = 1.2 V; XIN = 4.000 MHz; AGND, DGND = 0.0V.)(See Notes 1 and 2)

Parameter		Symbol	Min	Typ	Max	Unit
Accuracy (All Channels)						
Total Harmonic Distortion		THD	74	-	-	dB
Common Mode Rejection	(DC, 50, 60 Hz)	CMRR	80	-	-	dB
Common Mode + Signal on Input			VA-	-	VA+	V
Input Sampling Rate			-	XIN/4	-	Hz
Analog Inputs (Current Channels)						
Differential Input Voltage Range	Gain=20	IIN	-	±40	-	mV
[For example: (v_{IIN1+}) - (v_{IIN1-})]	Gain=1		-	±800	-	mV
Bipolar Offset	Gain=20	VOS	-	0.500	1	mV
	Gain=1	VOS	-	10	20	mV
Crosstalk (Channel-to-Channel)	(50, 60 Hz)		-	-	-120	dB
Input Capacitance	Gain = 20	IC	-	-	20	pF
	Gain = 1	IC	-	-	1	pF
Effective Input Impedance	(Note 3)					
	Gain=20	EII	50	-	-	kΩ
	Gain=1	EII	-	500	600	kΩ
Noise (Referred to Input)						
0-60 Hz	Gain=20		-	-	1	μV_{rms}
	Gain=1		-	-	20	μV_{rms}
0-1 kHz	Gain=20		-	-	2.5	μV_{rms}
	Gain=1		-	-	50	μV_{rms}
0-2 kHz	Gain=20		-	-	3.75	μV_{rms}
	Gain=1		-	-	75	μV_{rms}
Analog Inputs (Voltage Channels)						
Differential Input Voltage Range		VIN	-	±800	-	mV
[For example: (v_{VIN1+}) - (v_{VIN1-})]						
Bipolar Offset	Gain=1	VOS	-	20	25	mV
Crosstalk to any other channel at full-scale	(50, 60 Hz)		-	-	-120	dB
Input Capacitance		IC	-	-	0.2	pF
Effective Input Impedance	(Note 3)	EII	-	3	4	MΩ
Noise (Referred to Input)						
0-60 Hz			-	-	20	μV_{rms}
0-1 kHz			-	-	50	μV_{rms}
0-2 kHz			-	-	75	μV_{rms}
Dynamic Characteristics						
High Rate Filter Output Word Rate	OWRS = “0”	OWR	-	XIN/2048	-	Hz
	OWRS = “1”	OWR	-	XIN/1024	-	Hz

Notes: 1. Specifications guaranteed by design, characterization, and/or test.

2. Analog signals are relative to AGND and digital signals to DGND unless otherwise noted.

3. Effective Input Impedance (EII) varies with clock frequency (XIN) and Input Capacitance (IC)
EII = 1/(IC*XIN/4)

ANALOG CHARACTERISITCS (continued)

Parameter		Symbol	Min	Typ	Max	Unit
Reference Output						
Output Voltage		REFOUT	1.15	-	1.25	V
Temperature Coefficient			-	20	50	ppm/°C
Load Regulation	(Output Current 1µA Source or Sink)	ΔV_R	-	6	10	mV
Power Supply Rejection		PSRR	60	-	-	dB
Reference Input						
Input Voltage Range		VREF+	1.15	1.2	1.25	V
Input Capacitance			-	-	10	pF
Input CVF Current			-	-	1	µA
Power Supplies						
Power Supply Currents	I_{A+} I_{D+}	PSCA PSCD	- -	- -	3 4	mA mA
Power Consumption	(Note 4)	PC	-	-	27	mW
Power Supply Rejection (see Note 5)	(DC) (50, 60 Hz)	PSRR PSRR	50 60	- -	- -	dB dB

Notes: 4. All outputs unloaded. All inputs CMOS level.

5. Definition for PSRR: VREFIN tied to VREFOUT, VA+ = VD+ = 3V, AGND = DGND = 0V, VA- = -2V (using charge-pump circuit with CPD). In addition, a 106.07 mV rms (60 Hz) sinewave is imposed onto the VA+ and VD+ pins. The "+" and "-" input pins of both input channels are shorted to VA-. 2048 instantaneous digital output data words are collected for the channel under test. The rms value of the digital sinusoidal output signal is calculated, and this rms value is converted into the rms value of the sinusoidal voltage (measured in mV) that would need to be applied at the channel's inputs, in order to cause the same digital sinusoidal output. This voltage is then defined as Veq. PSRR is then (in dB):

$$PSRR = 20 \cdot \log\left\{\frac{106.07}{V_{eq}}\right\}$$

DIGITAL CHARACTERISTICS (T_A = -40 °C to +85 °C; +2.7V < VA+ < +3.5V; +2.7V < VD+ < +3.5V; VA- = -2 V ±10%; AGND, DGND = 0.0 V) (See Note 6)

Parameter		Symbol	Min	Typ	Max	Unit
High-Level Input Voltage		V_{IH}	0.6 VD+	-	VD+	V
Low-Level Input Voltage		V_{IL}	0.0	-	0.8	V
High-Level Output Voltage	I_{out} = -5.0 mA	V_{OH}	(VD+) - 1.0	-	-	V
Low-Level Output Voltage	I_{out} = 5.0 mA	V_{OL}	-	-	0.4	V
Input Leakage Current	(Note 7)	I_{in}	-	±1	±10	µA
3-State Leakage Current		I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance		C_{out}	-	9	-	pF

Notes: 6. All measurements performed under static conditions.

7. For OWRS and $\overline{GAIN}$ pins, input leakage current is 30 µA (Max).

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0.0 V)

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies	Positive Digital	VD+	2.7	3.0	3.5	V
	Positive Analog	VA+	2.7	3.0	3.5	V
	Negative Analog	VA-	-2.2	-2.0	-1.8	V
Voltage Reference Input		VREF+	-	1.2	-	V

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0.0 V; See Note 8.)

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies	Positive Digital	VD+	-0.3	-	+3.5	V
	Positive Analog	VA+	-0.3	-	+3.5	V
	Negative Analog	VA-	-2.5		-0.3	V
Input Current, Any Pin Except Supplies	(Note 9 and 10)	I_{IN}	-	-	±10	mA
Output Current		I_{OUT}	-	-	±25	mA
Power Dissipation	(Note 11)	PDN	-	-	500	mW
Analog Input Voltage	All Analog Pins	V_{INA}	VA- - 0.3	-	(VA+) + 0.3	V
Digital Input Voltage	All Digital Pins	V_{IND}	-0.3	-	(VD+) + 0.3	V
Ambient Operating Temperature		T_A	-40	-	85	°C
Storage Temperature		T_{stg}	-65	-	150	°C

Notes: 8. All voltages with respect to AGND.

9. Applies to all pins including continuous over-voltage conditions at the analog input (AIN) pins.

10. Transient current of up to 100 mA will not cause SCR latch-up. Maximum input current for a power supply pin is ±50 mA.

11. Total power dissipation, including all input currents and output currents.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS (T_A = -40 °C to +85 °C; VA+, VD+ = 3.0 V ±10%; VA- = -2 V ±10%; DGND = AGND = 0.0 V; Logic Levels: Logic 0 = 0.0 V, Logic 1 = VD+; CL = 50pF))

Parameter		Symbol	Min	Typ	Max	Unit
Master Clock Frequency	(Note 12)	XIN	3	4.000	5	MHz
Master Clock Duty Cycle		-	40	-	60	%
Rise Times	Any Digital Input (Note 13)	t_{rise}	-	-	1.0	µs
	Any Digital Output		-	50	-	ns
Fall Times	Any Digital Input (Note 13)	t_{fall}	-	-	1.0	µs
	Any Digital Output		-	50	-	ns
Serial Port Timing						
Serial Clock Frequency	(Note 12)					
	OWRS = "0"	SCLK	-	500	-	kHz
	OWRS = "1"	SCLK	-	1000	-	kHz
Serial Clock	Pulse Width High (Note 12)	t_1	-	0.5	-	SCLK
	Pulse Width Low (Note 10)	t_2	-	0.5	-	SCLK
SCLK falling to New Data Bit		t_3	-	-	50	ns
FSO Falling to SCLK Rising Delay	(Note 12)	t_4	-	0.5	-	SCLK
FSO Pulse Width	(Note 12)	t_5	-	1	-	SCLK
SE Rising to Output Enabled		t_6	-	-	50	ns
SE Falling to Output in Tri-state		t_7	-	-	50	ns

Notes: 12. Device parameters are specified with a 4.000 MHz clock, OWRS = 1.

13. Specified using 10% and 90% points on wave-form of interest. Output loaded with 50 pF.

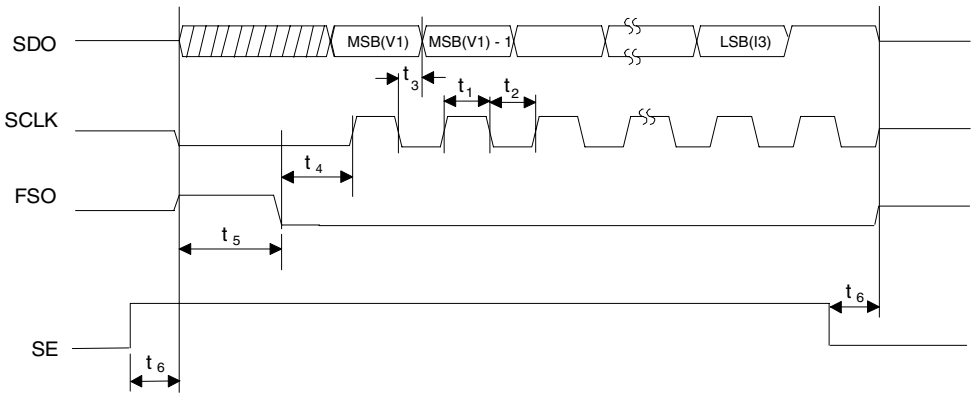


Figure 1. Serial Port Timing

2. GENERAL DESCRIPTION

The CS5451 is designed for 3-phase power meter applications and interfaces to a current transformers or shunt to measure current, and a resistive divider or transformer to measure voltage.

The CS5451 combines six ΔΣ modulators and decimation filters, three channels assigned for current input that have programmable input gain amplifiers, and three channels assigned for voltage input.

The CS5451 includes six decimation filters that output data at a 2000 Hz or 4000 Hz output word rate (OWR) when the input frequency at XIN = 4.096 MHz.

The device outputs data on a serial output port.

2.1 Theory of Operation

The CS5451 is designed to operate from a single +3V supply and provides a ±40 mV and ±800 mV input range for the current channels and ±800 mV range for the voltage channels. These voltages represent the maximum zero-to-peak voltage levels that can be presented to the inputs. The CS5451 is designed to accommodate common mode + signal levels from VA- to VA+. Figure 2 illustrates the CS5451 typical inputs and power supply connections.

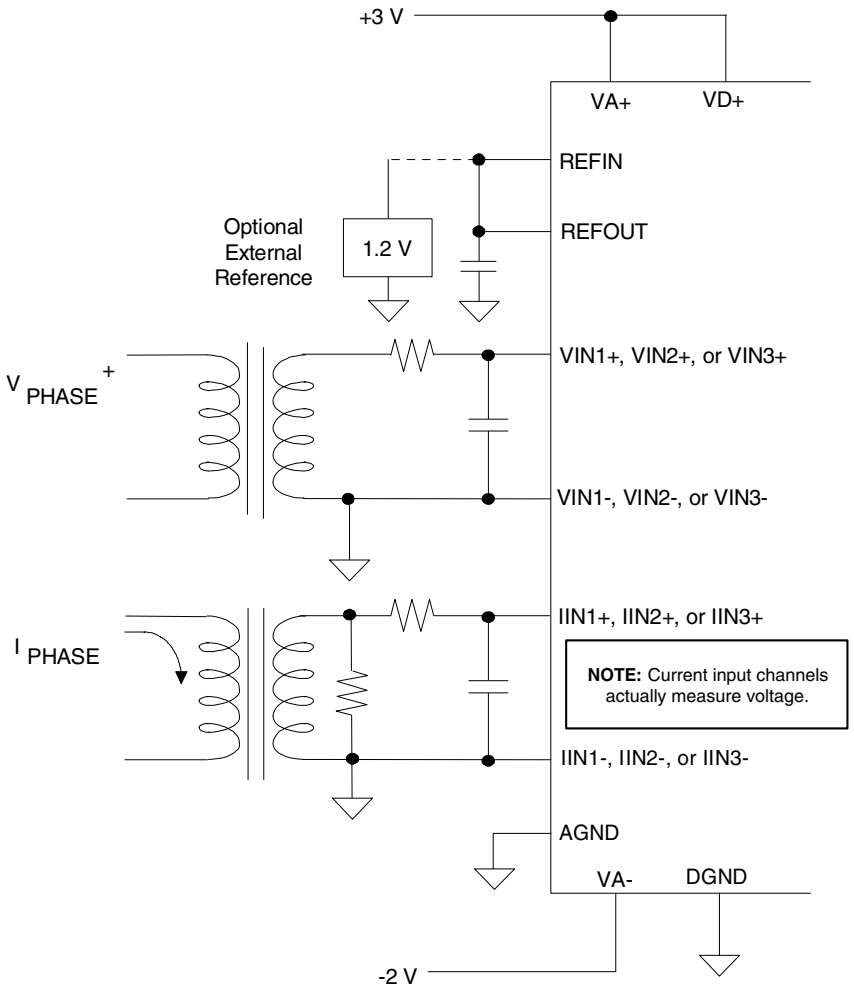


Figure 2. Typical Connection Diagram

2.2 Performing Measurements

The converter outputs are transferred in 16-bit signed (two's complement) data formats as a percentage of full scale. Table 1 below illustrates the ideal relationship between the differential voltage presented any one of the input channels and the corresponding output code. Note that for the current channels, the state of the $\overline{GAIN}$ input pin is assumed to driven low such that the PGA gain on the current channels is 1x. If the PGA gain of the current channels is set to 20x, a +40 mV differential voltage is presented across any pair of "IINk+" and "IINk-" pins (k = 1, 2, 3) would cause a (nominal) output code of 32767.

Differential Input Voltage (mV)	Output Code (hexadecimal)	Output Code (decimal)
+800	7FFF	32767
0.0122 to 0.0366	0001	1
-0.0122 to 0.0122	0000	0
-0.0122 to -0.0366	FFFF	-1
-800	8000	-32768

Table 1. Nominal Relationship for Differential Input Voltage vs. Output Code, for all channels. (Assume PGA gain is set to 1x.)

2.3 High Rate Digital Filters

If the OWRS pin is set to logic low, the high-rate filters are implemented as fixed $sinc^3$ filters with the following transfer function:

$$H(z) = \left(\frac{1 - z^{-256}}{1 - z^{-1}}\right)^3$$

This filter samples the modulator bit stream at XIN/8 Hz and decimates to XIN/2048 Hz.

If the OWRS pin is set to logic high, then the transfer function is

$$H(z) = \left(\frac{1 - z^{-128}}{1 - z^{-1}}\right)^3$$

The above filter samples the modulator bit stream at XIN/8 Hz and decimates to XIN/1024 Hz.

2.4 Serial Interface

The CS5451 communicates with a target device via a master serial data output port. Output data is provided on the SDO output synchronous with the SCLK output. A third output, FSO, is a framing signal used to signal the start of output data. These three outputs will be driven as long as the SE (serial

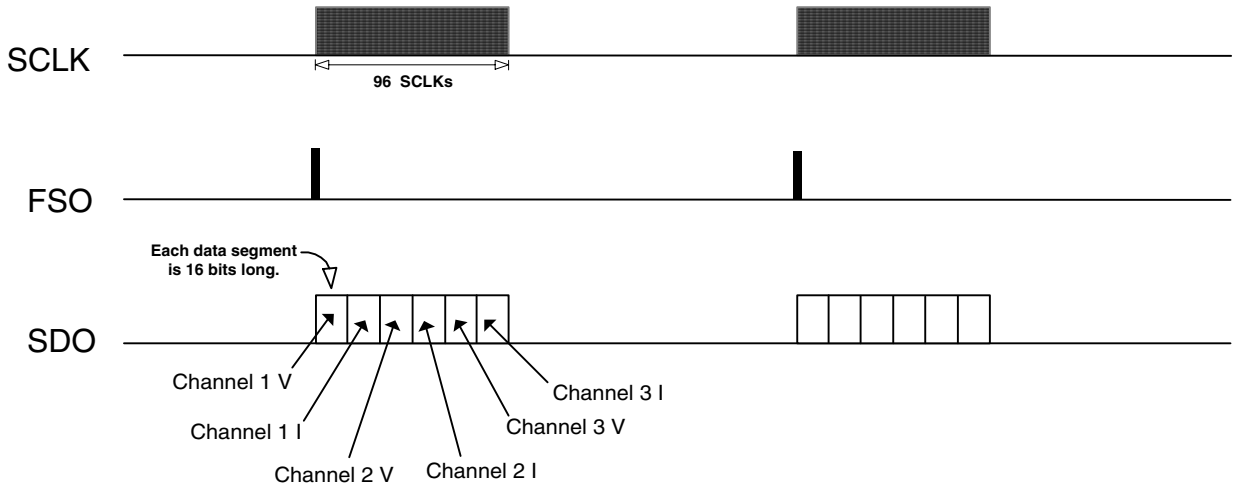


Figure 3. Serial Port Data Transfer

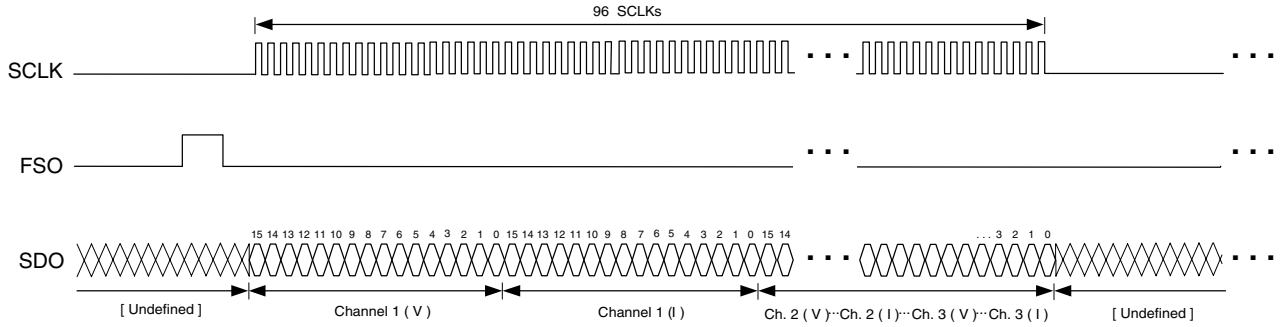


Figure 4. Close-up of One Data Frame

enable) input is held high. Otherwise, these outputs will be high impedance.

Data out (SDO) changes as a result of SCLK falling, and always outputs valid data with SCLK rising. When data is being transferred, the SCLK frequency is either 1/8 of the XIN input frequency (when OWRS is held low) or 1/4 of the XIN input frequency (when OWRS is held high). Any other time, SCLK is held low. (See Figures 3 and 4.)

The framing signal (FSO) output is normally low, but produces a high level pulse lasting one SCLK period when the instantaneous voltage/current data samples are about to be transmitted out of the serial interface (after each A/D conversion cycle). Note: SCLK is not active during FSO high.

For 96 SCLK periods after FSO falls, SCLK is active and SDO produces valid output. Six channels of 16 bit data are output, MSB first. Voltage and current measurements are output (in that order) for three phases. SCLK will then be held low until the next sample period.

2.5 System Initialization

When power to the CS5451 is applied, the chip must be held in a reset condition using the $\overline{\text{RESET}}$ input.

A hardware reset is initiated when the $\overline{\text{RESET}}$ pin is forced low with a minimum pulse width of 50 ns.

2.6 Analog Inputs

The analog inputs of the CS5451 are bipolar voltage inputs: Three voltage channel inputs VIN(1-3) and three current channel inputs IIN(1-3). The CS5451 accommodates a full scale range of ±40 mV or ±800 mV on the Current Channels and ±800 mV on the Voltage Channels.

2.7 Voltage Reference

The CS5451 is specified for operation with a +1.2 V reference between the VREFIN and AGND pins. The converter includes an internal 1.2 V reference (50 ppm/°C drift) that can be used by connecting the VREFOUT pin to the VREFIN pin of the device. If higher accuracy/stability is required, an external reference can be used.

2.8 Power Supply

The low, stable analog power consumption and superior supply rejection of the CS5451 allow for the use of a simple charge-pump negative supply generator. The use of a negative supply alleviates the need for level shifting of the analog inputs. The CPD pin and capacitor C1 provide the necessary analog supply current as shown in Figure 5. The Schottky diodes D1 and D2 are chosen for their low forward voltages and high-speed capabilities. The capacitor C2 provides the required charge storage and bypassing of the negative supply. The CPD output signal provides the charge pump driver sig-

nal. The frequency of the charge pump driver signal is synchronous to XIN. The nominal average frequency is 1 Mhz. The level on the VA- pin is fed back internally so that the CPD output will regulate the VA- level to -2/3 of VA+ level.

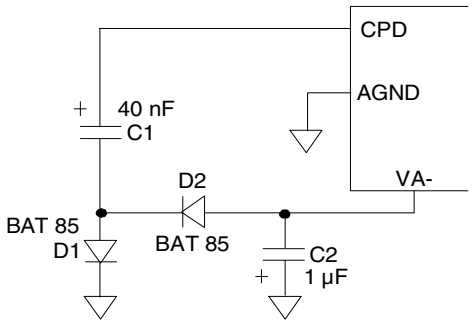


Figure 5. Generating VA- with a Charge Pump

Note the value of C1 in Figure 5. The 40 nF value is recommended when the input frequency presented to the XIN pin is 4.00 MHz. If the user decides to use an XIN frequency that is significantly different than 4.00 MHz (if the XIN frequency is increased/decreased by more than 5% of 4.00 MHz, then it is recommended that the user should alter the value of C1. The percentage change in the value of C1 (with respect to a reference value of 40 nF) should be inversely proportional to the percentage change in the XIN frequency. For example, if the XIN frequency is increased from 4.00 MHz to 4.5 MHz, this represents a percentage increase of 12.5%. Therefore, the value of C1 should be reduced by 12.5%, making the new value for C1 to be 35 nF. For more information about the operation of this type of charge pump circuit, the reader can refer to Cirrus Logic, Inc.'s application note *AN152: Using the CS5521/24/28, and CS5525/26 Charge Pump Drive for External Loads.*

2.9 PCB Layout

For optimal performance, the CS5460A should be placed entirely over an analog ground plane with both the VA- and DGND pins of the device connected to the analog plane. Place the analog-digital plane split immediately adjacent to the digital portion of the chip.

Note: Refer to the CDB5460A Evaluation Board for suggested layout details and Applications Note 18 for more detailed layout guidelines. Before layout, please call for our Free Schematic Review Service.

3. PIN DESCRIPTION

Serial Clock Output	**SCLK**	1	28	**VD+**	Digital Supply
Serial Data Output	**SDO**	2	27	**DGND**	Digital Ground
Frame Sync	**FSO**	3	26	**CPD**	Charge Pump Drive
Serial Port Enable	**SE**	4	25	**XIN**	Master Clock
Current Input Gain	**$\overline{\text{GAIN}}$**	5	24	**$\overline{\text{RESET}}$**	Reset
Analog Ground	**AGND**	6	23	**OWRS**	Output Word Rate Select
Reference Input	**VREFIN**	7	22	**VIN1+**	Differential Voltage Input 1
Reference Output	**VREFOUT**	8	21	**VIN1-**	Differential Voltage Input 1
Positive Analog Supply	**VA+**	9	20	**IIN1+**	Differential Current Input 1
Negative Analog Supply	**VA-**	10	19	**IIN1-**	Differential Current Input 1
Differential Voltage Input 3	**VIN3+**	11	18	**VIN2+**	Differential Voltage Input 2
Differential Voltage Input 3	**VIN3-**	12	17	**VIN2-**	Differential Voltage Input 2
Differential Current Input 3	**IIN3+**	13	16	**IIN2+**	Differential Current Input 2
Differential Current Input 3	**IIN3-**	14	15	**IIN2-**	Differential Current Input 2

Clock Generator

XIN - Master Clock Input

Control Pins and Serial Data I/O

SE - Serial Port Enable

When SE is low, the output pins of the serial port are 3-stated.

SDO - Serial Port Output

Data will be at a rate determined by SCLK.

FSO - Frame Signal Output

Framing signal output for data transfer from SDO pin.

SCLK - Serial Clock Output

A clock signal on this pin determines the output rate of data for SDO pin. Rate of SCLK is determined by XIN frequency and state of OWRS input pin.

$\overline{\text{RESET}}$ - Reset

When reset is taken low, all internal registers are set to their default states.

$\overline{\text{GAIN}}$ - Input Gain Control

Sets input gain for current channels. A logic high sets internal gain to 1, a logic low level sets the gain to 20. If no connection is made to this pin, it will default to logic low level (through internal 200K resistor to DGND).

OWRS - Output Word Rate Select

When OWRS is set to logic low, the output word rate (OWR) at SDO pin is XIN/2048 (Hz). When set to logic high, the OWR at SDO pin is XIN/1024 (Hz). If no connection is made to this pin, then OWRS will default to logic low level (through internal 200K resistor to DGND).

Measurement and Reference Input

IIN(1-3)+, IIN(1-3)- - Differential Current Inputs

Differential analog input pins for current channels.

VIN(1-3)+, VIN(1-3)- - Differential Voltage Inputs

Differential analog input pins for voltage channels.

VREFOUT - Voltage Reference Output

The on-chip voltage reference is output from this pin. The voltage reference has a nominal magnitude of 1.2 V and is referenced to the AGND pin on the converter.

VREFIN - Voltage Reference Input

The voltage input to this pin establishes the voltage reference for the on-chip modulator.

Power Supply Connections

VA+ - Positive Analog Supply

The positive analog supply is nominally +3 V ±10% relative to AGND.

VA- - Negative Analog Supply

The negative analog supply is nominally -2 V ±10% relative to AGND.

AGND - Analog Ground

The analog ground pin for input signals.

VD+ - Positive Digital Supply

The positive digital supply is nominally +3 V ±10% relative to DGND.

DGND - Digital Ground

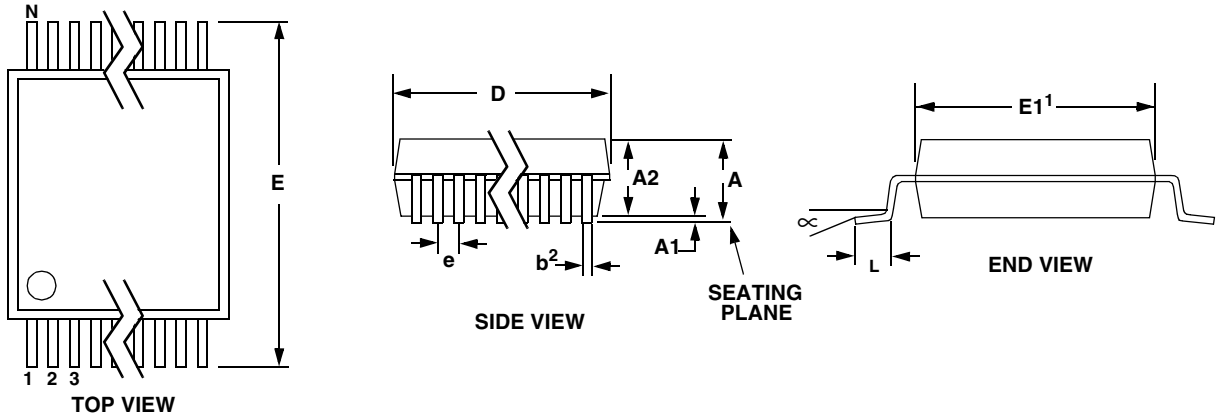
The digital ground is typically at the same level as AGND.

CPD - Charge Pump Drive

This output pin drives the external charge pump circuitry to create a negative supply voltage.

4. PACKAGE DIMENSIONS

28L SSOP PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.084	--	--	2.13	
A1	0.002	0.006	0.010	0.05	0.13	0.25	
A2	0.064	0.069	0.074	1.62	1.75	1.88	
b	0.009	--	0.015	0.22	--	0.38	2,3
D	0.390	0.4015	0.413	9.90	10.20	10.50	1
E	0.291	0.307	0.323	7.40	7.80	8.20	
E1	0.197	0.209	0.220	5.00	5.30	5.60	1
e	0.022	0.026	0.030	0.55	0.65	0.75	
L	0.025	0.0354	0.041	0.63	0.90	1.03	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-150

Notes: 1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.

3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.


SMART
Analog
™