

# SN54LS399, SN74LS399 QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

SDLS174 – OCTOBER 1976 – REVISED MARCH 1988

- **Single-Rail Outputs on 'LS399**
- **Selects One of Two 4-Bit Data Sources and Stores Data Synchronously with System Clock**
- **Applications:**
  - Dual Source for Operands and Constants in Arithmetic Processor; Can Release Processor Register Files for Acquiring New Data
  - Implement Separate Registers Capable of Parallel Exchange of Contents Yet Retain External Load Capability
  - Universal Type Register for Implementing Various Shift Patterns: Even Has Compound Left-Right Capabilities

## description

This monolithic quadruple two-input multiplexer with storage provides essentially the equivalent functional capabilities of two separate MSI functions (SN54LS157/SN74LS157 and SN54LS175/SN74LS175) in a single 16-pin package.

When the word-select input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is clocked to the output terminals on the positive-going edge of the clock pulse.

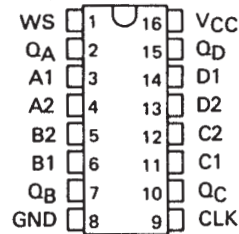
Typical power dissipation is 37 milliwatts. The SN54LS399 is characterized for operation over the full military range of -55°C to 125°C. The SN74LS399 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

| INPUTS      |       | OUTPUTS         |                 |                 |                 |
|-------------|-------|-----------------|-----------------|-----------------|-----------------|
| WORD SELECT | CLOCK | Q <sub>A</sub>  | Q <sub>B</sub>  | Q <sub>C</sub>  | Q <sub>D</sub>  |
| L           | ↑     | a1              | b1              | c1              | d1              |
| H           | ↑     | a2              | b2              | c2              | d2              |
| X           | L     | Q <sub>A0</sub> | Q <sub>B0</sub> | Q <sub>C0</sub> | Q <sub>D0</sub> |

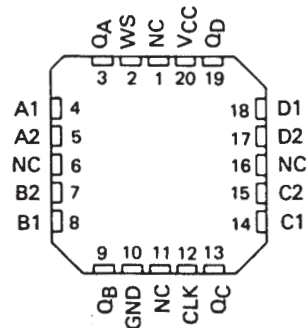
SN54LS399 . . . J OR W PACKAGE  
SN74LS399 . . . D OR N PACKAGE

(TOP VIEW)



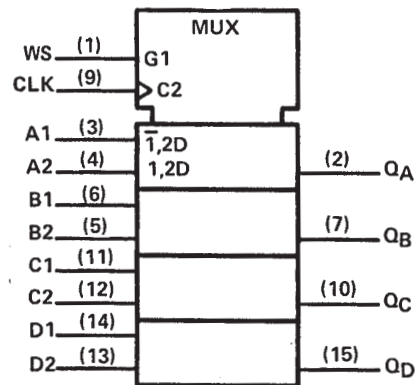
SN54LS399 . . . FK PACKAGE

(TOP VIEW)



NC – No internal connection

## logic symbol†



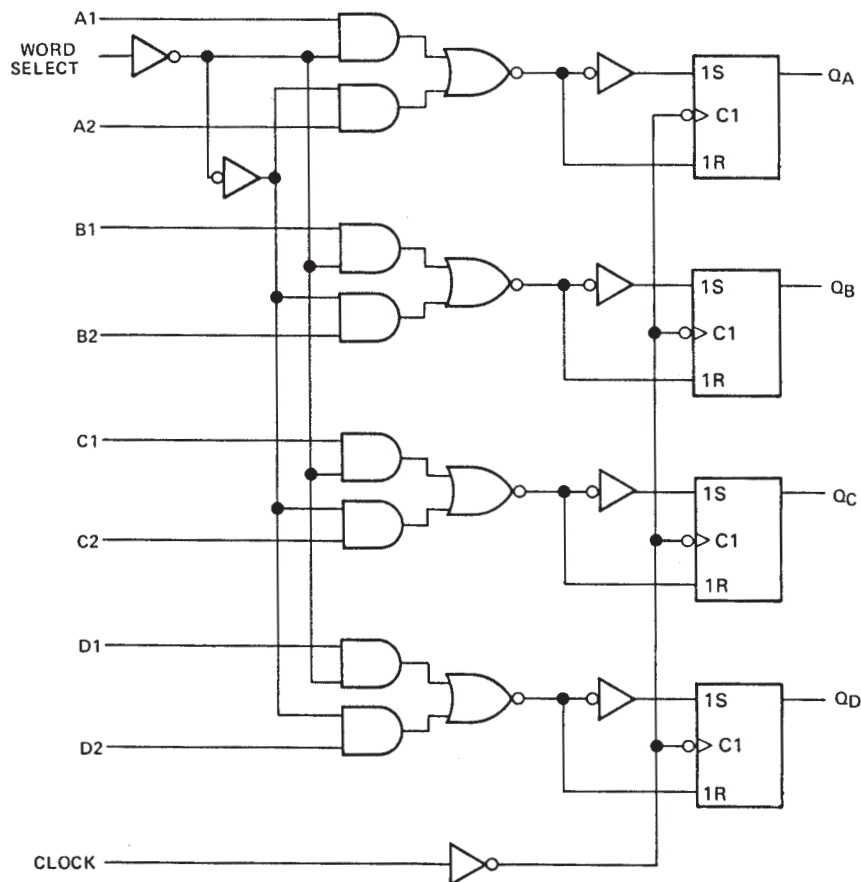
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

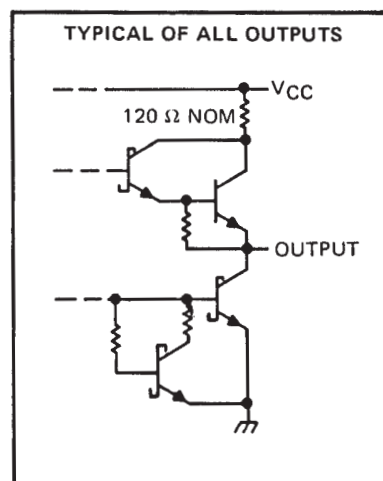
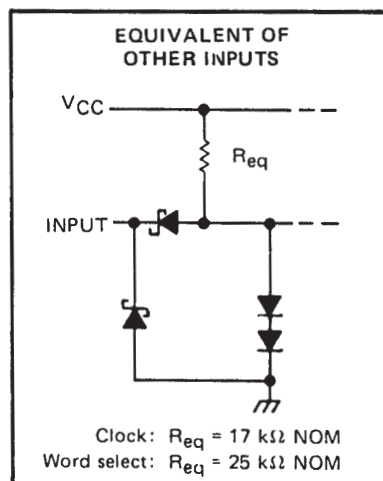
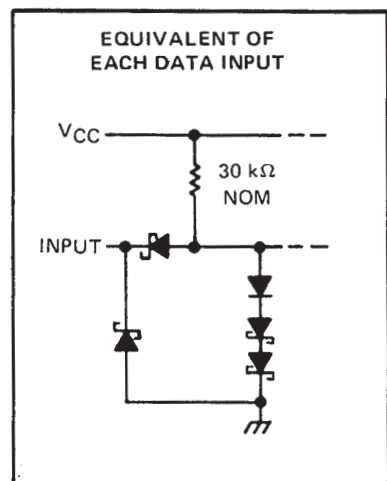
# SN54LS399, SN74LS399 QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

SDLS174 – OCTOBER 1976 – REVISED MARCH 1988

## logic diagram (positive logic)



## schematics of inputs and outputs



# SN54LS399, SN74LS399

## QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

SDLS174 – OCTOBER 1976 – REVISED MARCH 1988

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

|                                                 |                |
|-------------------------------------------------|----------------|
| Supply voltage, $V_{CC}$ (see Note 1)           | 7 V            |
| Input voltage                                   | 7 V            |
| Operating free-air temperature range: SN54LS399 | –55°C to 125°C |
| SN74LS399                                       | 0°C to 70°C    |
| Storage temperature range                       | –65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminals.

### recommended operating conditions

|                                                |             | SN54LS399 |     |      | SN74LS399 |     |      | UNIT    |
|------------------------------------------------|-------------|-----------|-----|------|-----------|-----|------|---------|
|                                                |             | MIN       | NOM | MAX  | MIN       | NOM | MAX  |         |
| Supply voltage, $V_{CC}$                       |             | 4.5       | 5   | 5.5  | 4.75      | 5   | 5.25 | V       |
| High-level output current, $I_{OH}$            |             |           |     | –400 |           |     | –400 | $\mu$ A |
| Low-level output current, $I_{OL}$             |             |           |     | 4    |           |     | 8    | mA      |
| Width of clock pulse, high or low level, $t_W$ |             | 20        |     |      | 20        |     |      | ns      |
| Setup time, $t_{su}$                           | Data        | 25        |     |      | 25        |     |      | ns      |
|                                                | Word select | 45        |     |      | 45        |     |      |         |
| Hold time, $t_h$                               | Data        | 0         |     |      | 0         |     |      | ns      |
|                                                | Word select | 0         |     |      | 0         |     |      |         |
| Operating free-air temperature, $T_A$          |             | –55       |     | 125  | 0         |     | 70   | °C      |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                                             | TEST CONDITIONS†       |                                                                | SN54LS399                 |      | SN74LS399 |     | UNIT |      |
|-------------------------------------------------------|------------------------|----------------------------------------------------------------|---------------------------|------|-----------|-----|------|------|
|                                                       |                        |                                                                | MIN                       | TYP‡ | MAX       | MIN |      | TYP‡ |
| V <sub>IH</sub> High-level input voltage              |                        |                                                                | 2                         |      | 2         |     | V    |      |
| V <sub>IL</sub> Low-level input voltage               |                        |                                                                |                           |      | 0.7       |     | 0.8  |      |
| V <sub>IK</sub> Input clamp voltage                   | V <sub>CC</sub> = MIN, | I <sub>I</sub> = −18 mA                                        |                           |      | −1.5      |     | −1.5 |      |
| V <sub>OH</sub> High-level output voltage             | V <sub>CC</sub> = MIN, | V <sub>IH</sub> = 2 V,<br>V <sub>IL</sub> = V <sub>ILmax</sub> | I <sub>OH</sub> = −400 μA |      | 2.5       | 3.4 | 2.7  | 3.4  |
| V <sub>OL</sub> Low-level output voltage              | V <sub>CC</sub> = MIN, | V <sub>IH</sub> = 2 V,<br>V <sub>IL</sub> = V <sub>ILmax</sub> | I <sub>OL</sub> = 4 mA    |      | 0.25      | 0.4 | 0.25 | 0.4  |
|                                                       |                        |                                                                | I <sub>OL</sub> = 8 mA    |      |           |     | 0.35 | 0.5  |
| I <sub>I</sub> Input current at maximum input voltage | V <sub>CC</sub> = MAX, | V <sub>I</sub> = 7 V                                           |                           |      | 0.1       |     | 0.1  |      |
| I <sub>IH</sub> High-level input current              | V <sub>CC</sub> = MAX, | V <sub>I</sub> = 2.7 V                                         |                           |      | 20        |     | 20   |      |
| I <sub>IL</sub> Low-level input current               | V <sub>CC</sub> = MAX, | V <sub>I</sub> = 0.4 V                                         |                           |      | −0.4      |     | −0.4 |      |
| I <sub>OS</sub> Short-circuit output current§         | V <sub>CC</sub> = MAX  |                                                                | −20                       |      | −100      |     | −20  | −100 |
| I <sub>CC</sub> Supply current                        | V <sub>CC</sub> = MAX, | See Note 2                                                     |                           |      | 7.3       |     | 13   |      |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time, duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open and all inputs except clock low,  $I_{CC}$  is measured after applying a momentary 4.5 V, followed by ground, to the clock input.

### switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$

| PARAMETER                                                  | TEST CONDITIONS                                     | MIN | TYP | MAX | UNIT |
|------------------------------------------------------------|-----------------------------------------------------|-----|-----|-----|------|
| $t_{PLH}$ Propagation delay time, low-to-high-level output | $C_L = 15 \text{ pF}$ , $R_L = 2 \text{ k}\Omega$ , |     | 18  | 27  | ns   |
| $t_{PHL}$ Propagation delay time, high-to-low-level output | See Note 3                                          |     | 21  | 32  |      |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 84154012A        | ACTIVE                | LCCC         | FK              | 20   | 1           | TBD                     | POST-PLATE       | N / A for Pkg Type           |
| 8415401EA        | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                     | A42              | N / A for Pkg Type           |
| 8415401EA        | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                     | A42              | N / A for Pkg Type           |
| 8415401FA        | ACTIVE                | CFP          | W               | 16   | 1           | TBD                     | A42              | N / A for Pkg Type           |
| 8415401FA        | ACTIVE                | CFP          | W               | 16   | 1           | TBD                     | A42              | N / A for Pkg Type           |
| SN54LS399J       | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                     | A42              | N / A for Pkg Type           |
| SN54LS399J       | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                     | A42              | N / A for Pkg Type           |
| SN74LS399DR      | OBSOLETE              | SOIC         | D               | 16   |             | TBD                     | Call TI          | Call TI                      |
| SN74LS399DR      | OBSOLETE              | SOIC         | D               | 16   |             | TBD                     | Call TI          | Call TI                      |
| SN74LS399N       | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SN74LS399N       | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SN74LS399N3      | OBSOLETE              | PDIP         | N               | 16   |             | TBD                     | Call TI          | Call TI                      |
| SN74LS399N3      | OBSOLETE              | PDIP         | N               | 16   |             | TBD                     | Call TI          | Call TI                      |
| SN74LS399NE4     | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SN74LS399NE4     | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SNJ54LS399FK     | ACTIVE                | LCCC         | FK              | 20   | 1           | TBD                     | POST-PLATE       | N / A for Pkg Type           |
| SNJ54LS399FK     | ACTIVE                | LCCC         | FK              | 20   | 1           | TBD                     | POST-PLATE       | N / A for Pkg Type           |
| SNJ54LS399J      | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                     | A42              | N / A for Pkg Type           |
| SNJ54LS399J      | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                     | A42              | N / A for Pkg Type           |
| SNJ54LS399W      | ACTIVE                | CFP          | W               | 16   | 1           | TBD                     | A42              | N / A for Pkg Type           |
| SNJ54LS399W      | ACTIVE                | CFP          | W               | 16   | 1           | TBD                     | A42              | N / A for Pkg Type           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is

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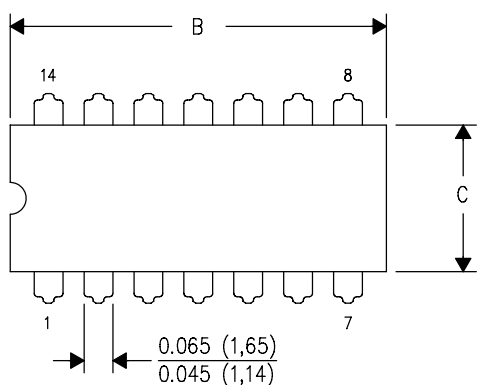
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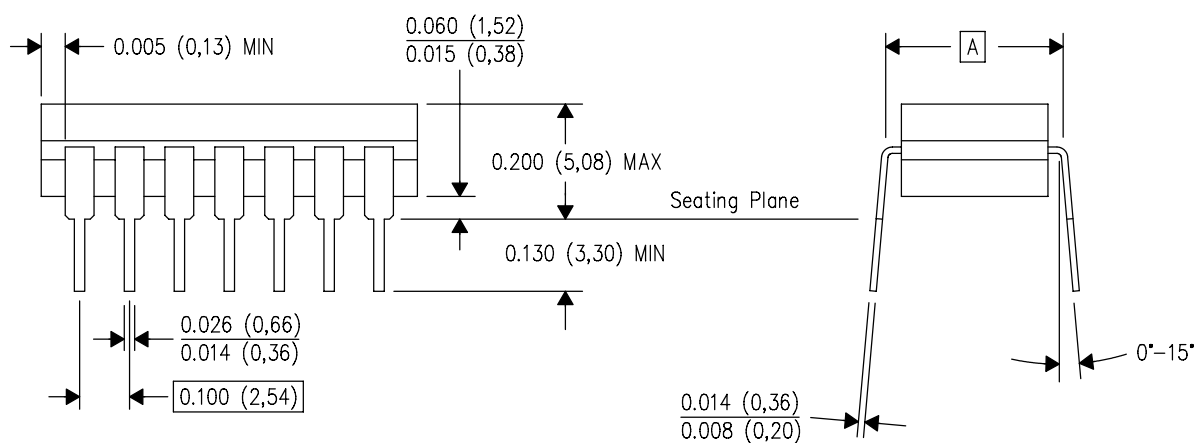
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



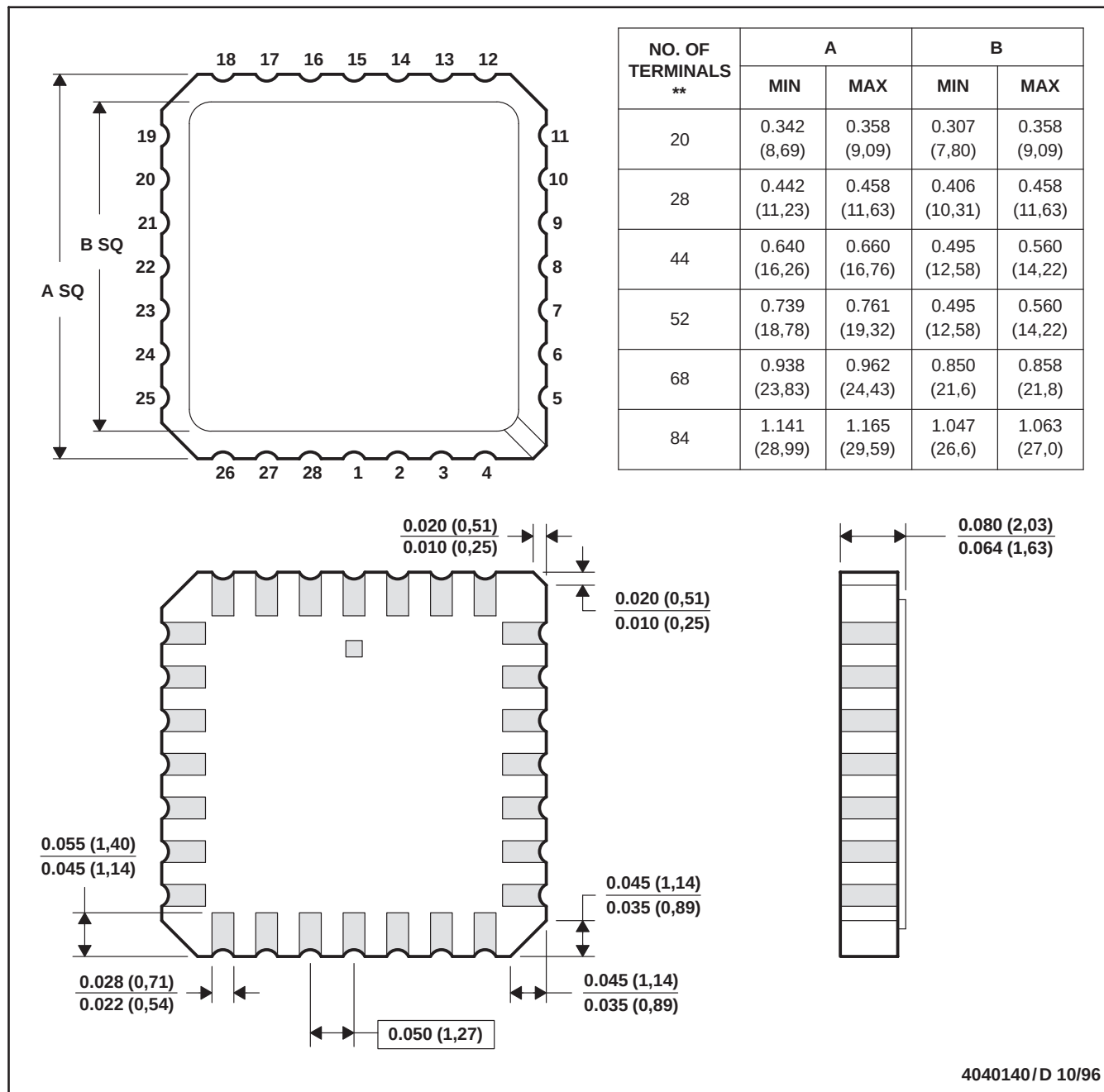
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

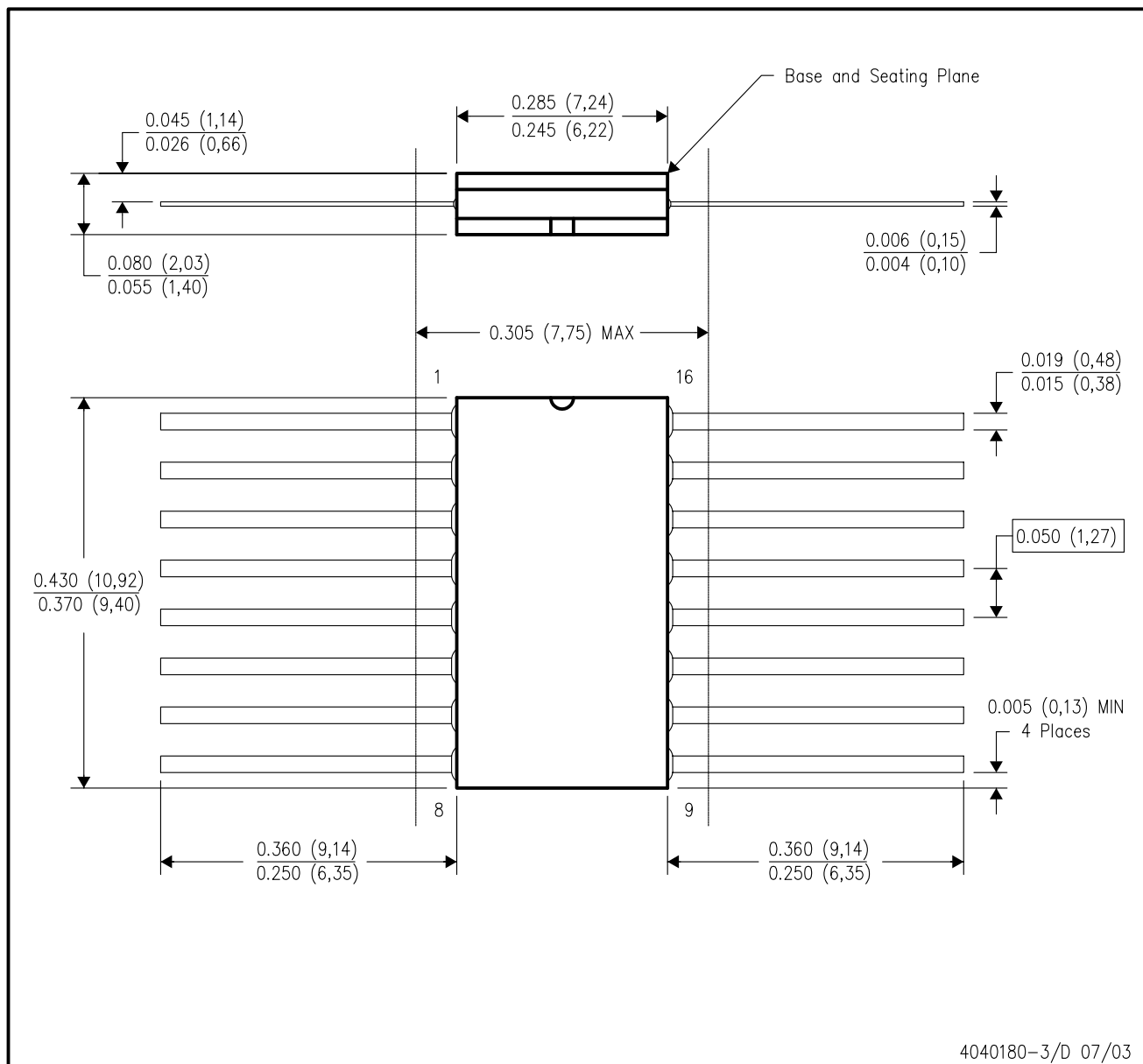
28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK

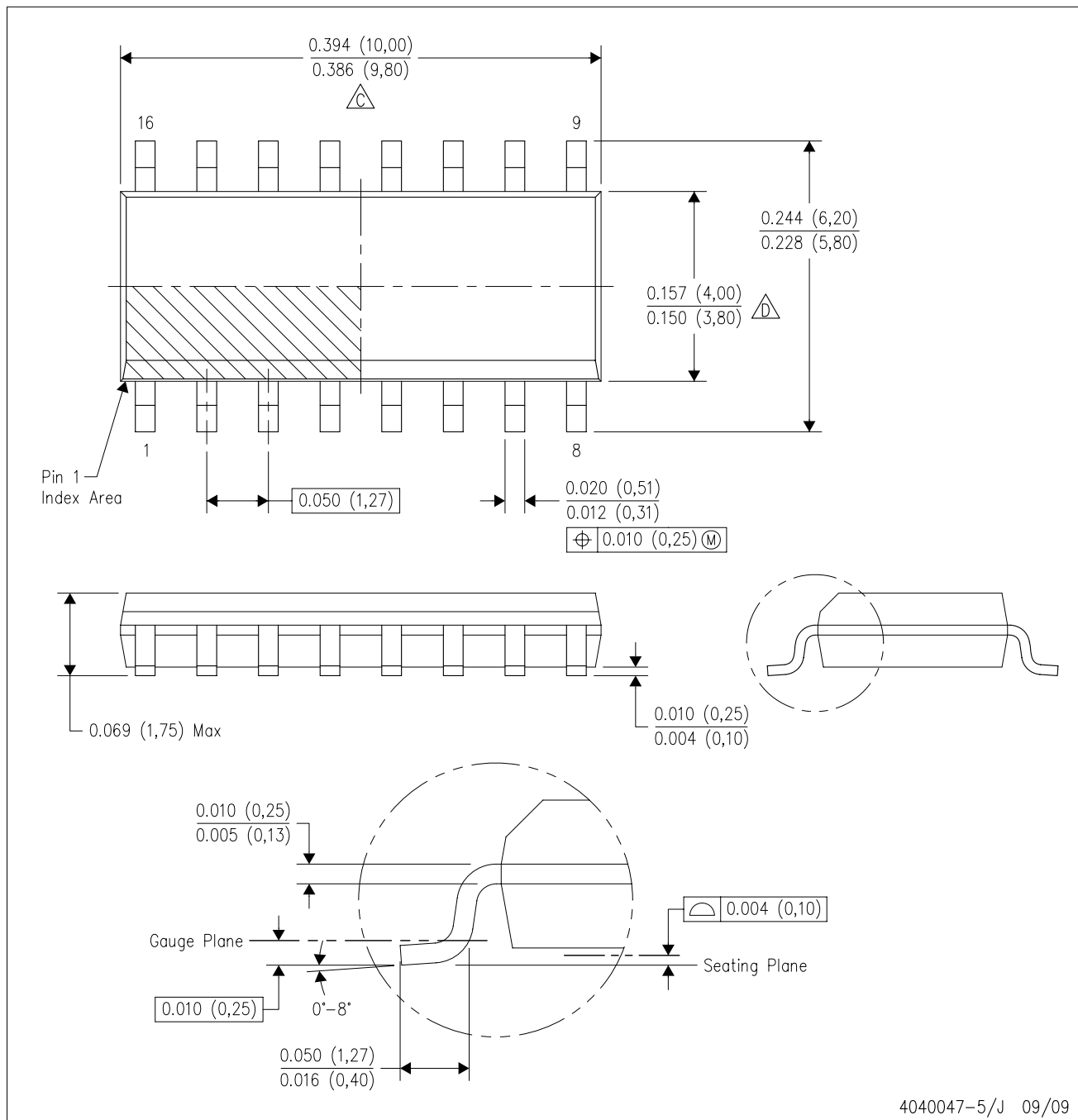


- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC



D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-5/J 09/09

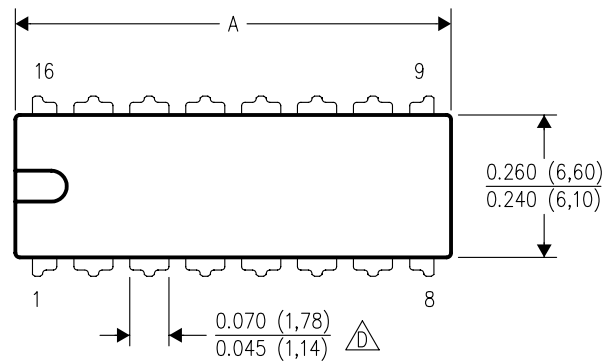
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AC.

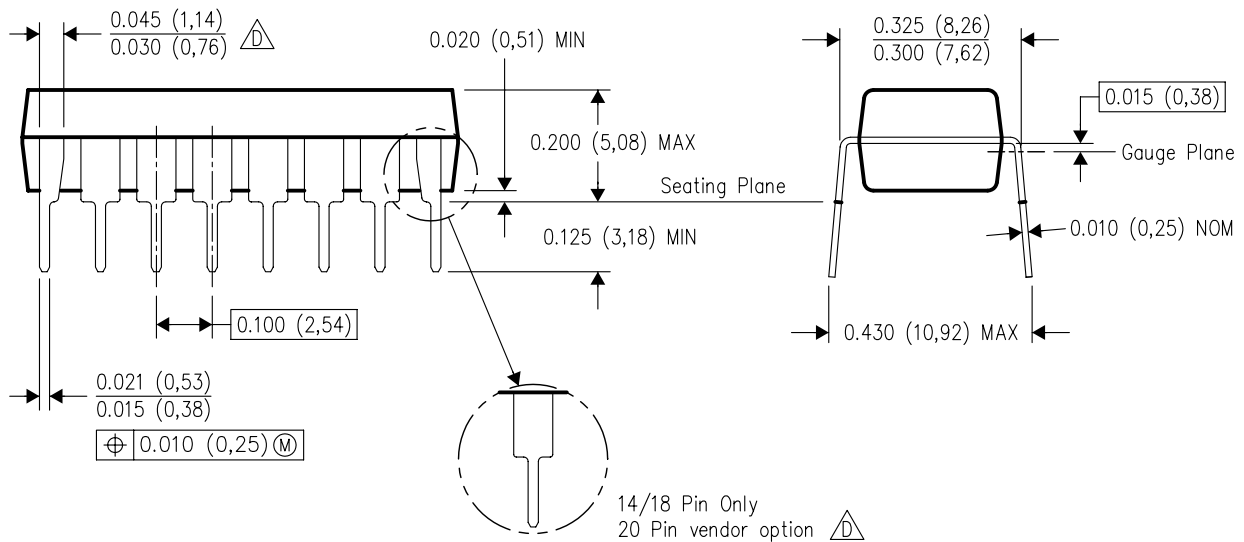
N (R-PDIP-T\*\*)

16 PINS SHOWN

# PLASTIC DUAL-IN-LINE PACKAGE



| DIM \ PINS **       | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 84154012A        | ACTIVE                | LCCC         | FK              | 20   | 1           | TBD                     | POST-PLATE       | N / A for Pkg Type           |
| 8415401EA        | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                     | A42              | N / A for Pkg Type           |
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| SN54LS399J       | ACTIVE                | CDIP         | J               | 16   | 1           | TBD                     | A42              | N / A for Pkg Type           |
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| SN74LS399DR      | OBSOLETE              | SOIC         | D               | 16   |             | TBD                     | Call TI          | Call TI                      |
| SN74LS399N       | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SN74LS399N       | ACTIVE                | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| SN74LS399N3      | OBSOLETE              | PDIP         | N               | 16   |             | TBD                     | Call TI          | Call TI                      |
| SN74LS399N3      | OBSOLETE              | PDIP         | N               | 16   |             | TBD                     | Call TI          | Call TI                      |
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| SNJ54LS399W      | ACTIVE                | CFP          | W               | 16   | 1           | TBD                     | A42              | N / A for Pkg Type           |
| SNJ54LS399W      | ACTIVE                | CFP          | W               | 16   | 1           | TBD                     | A42              | N / A for Pkg Type           |

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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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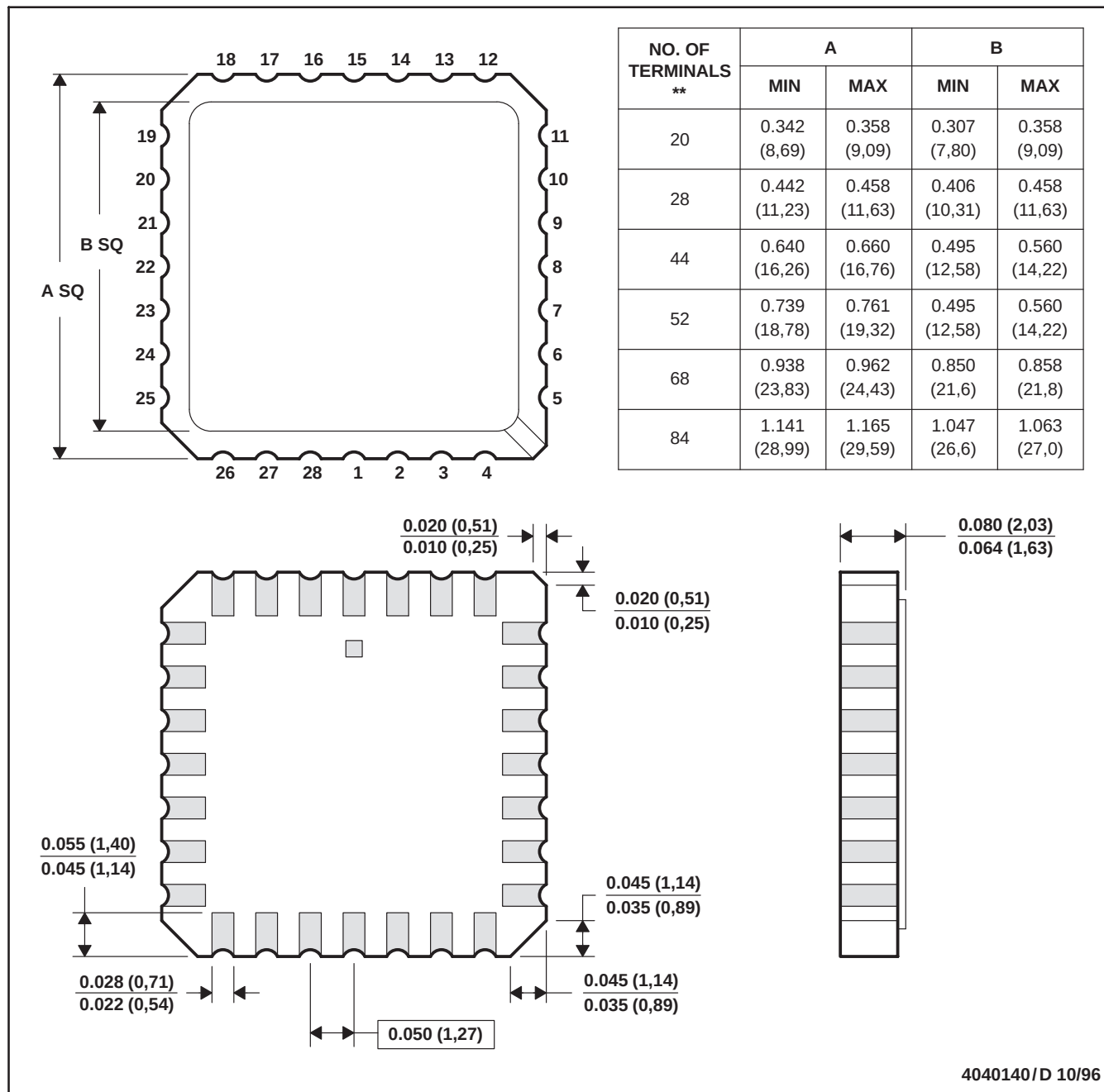
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FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

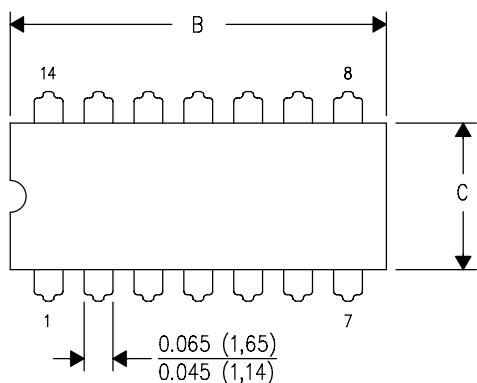


- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - The terminals are gold plated.
  - Falls within JEDEC MS-004

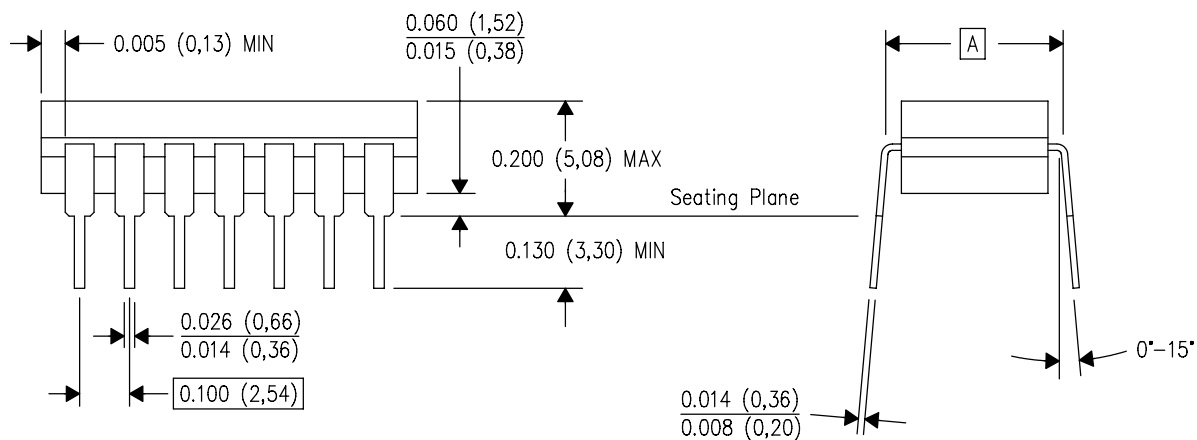
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |

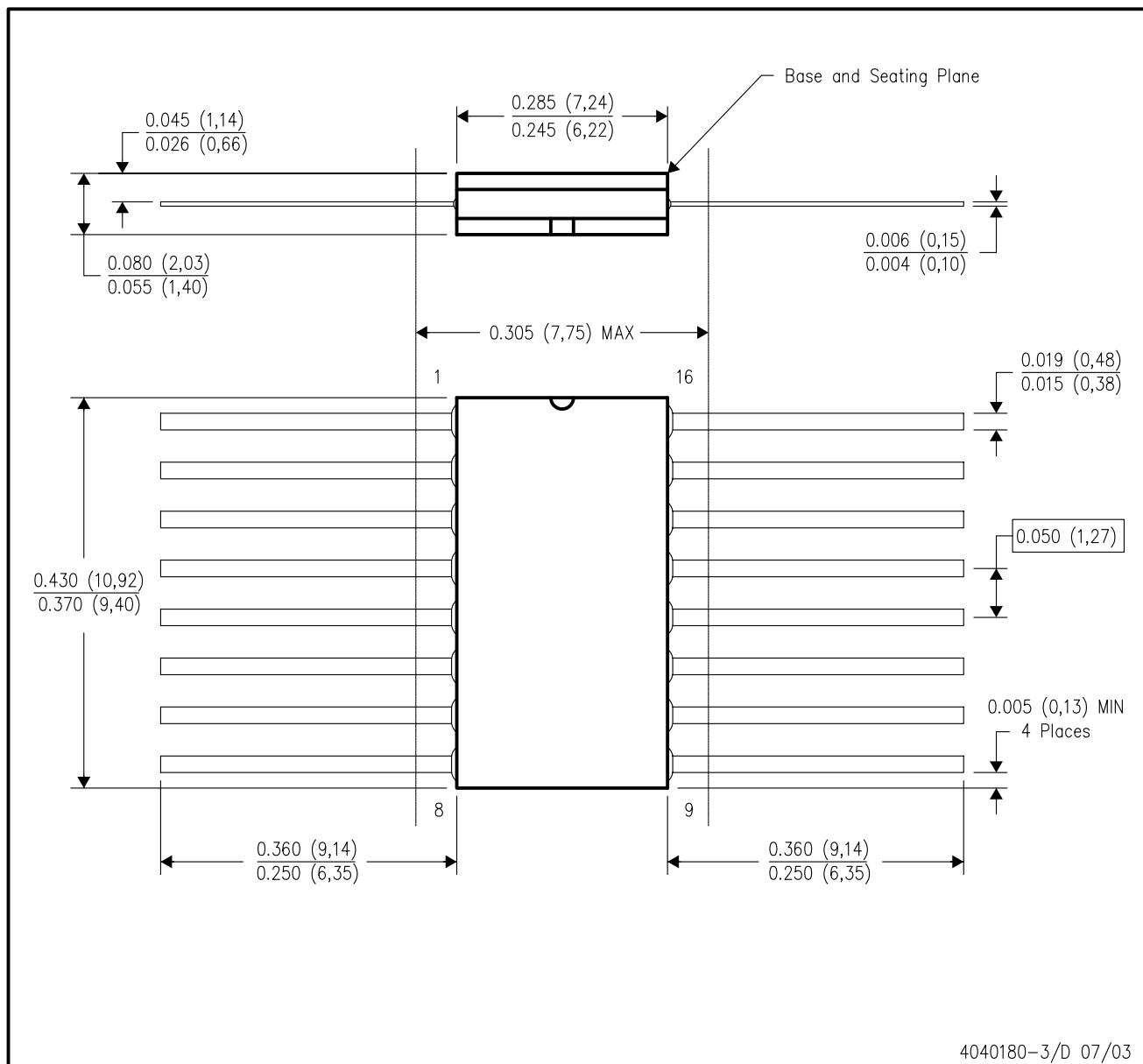


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

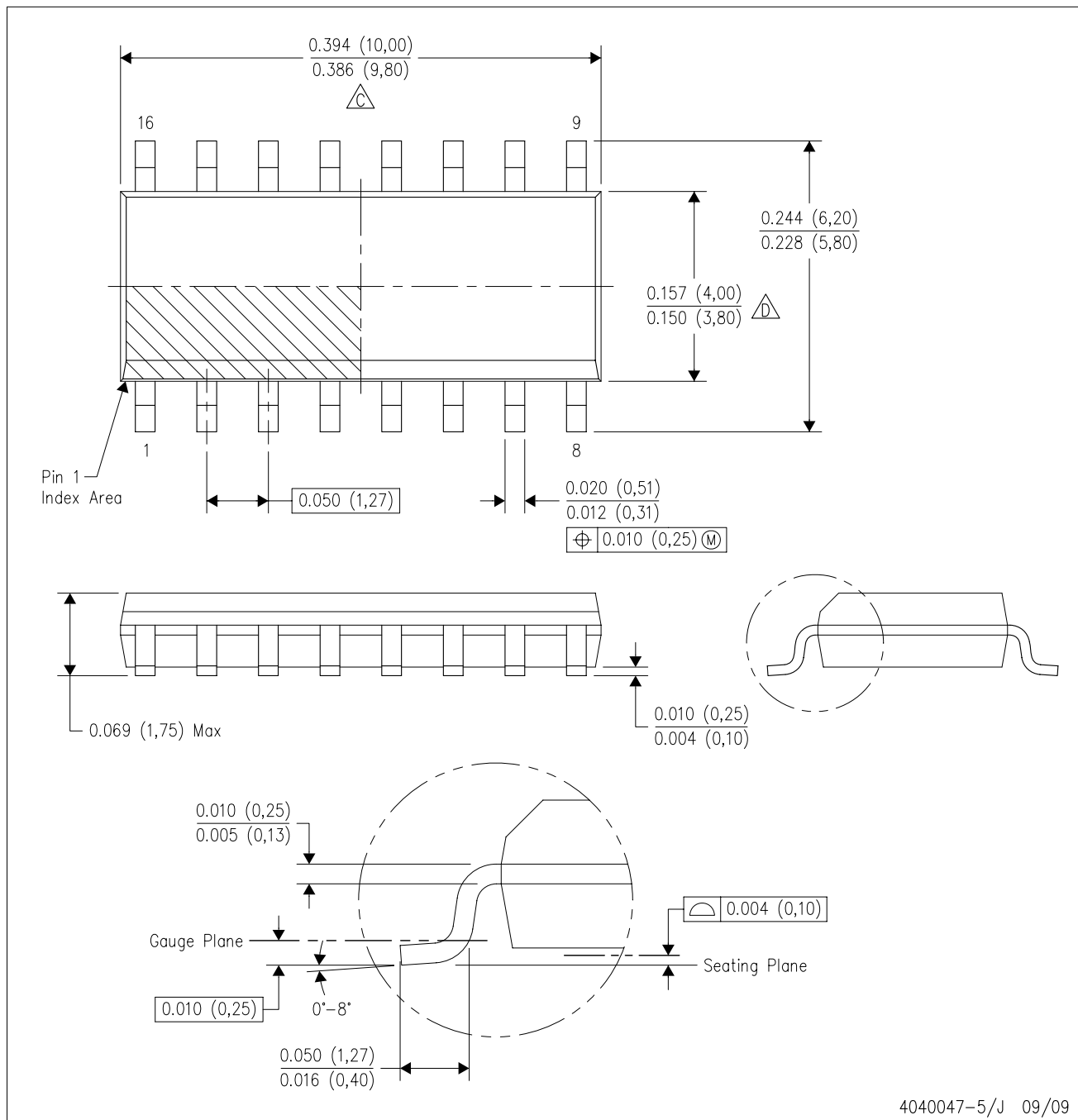
CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-5/J 09/09

NOTES:

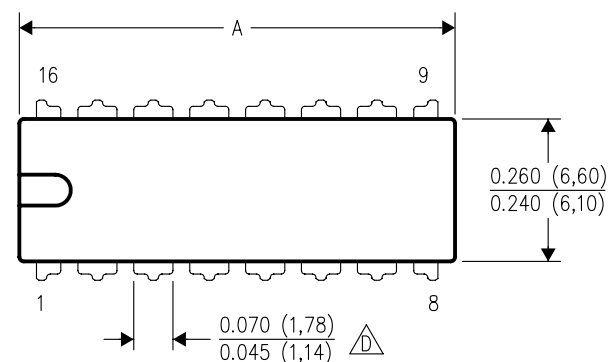
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AC.



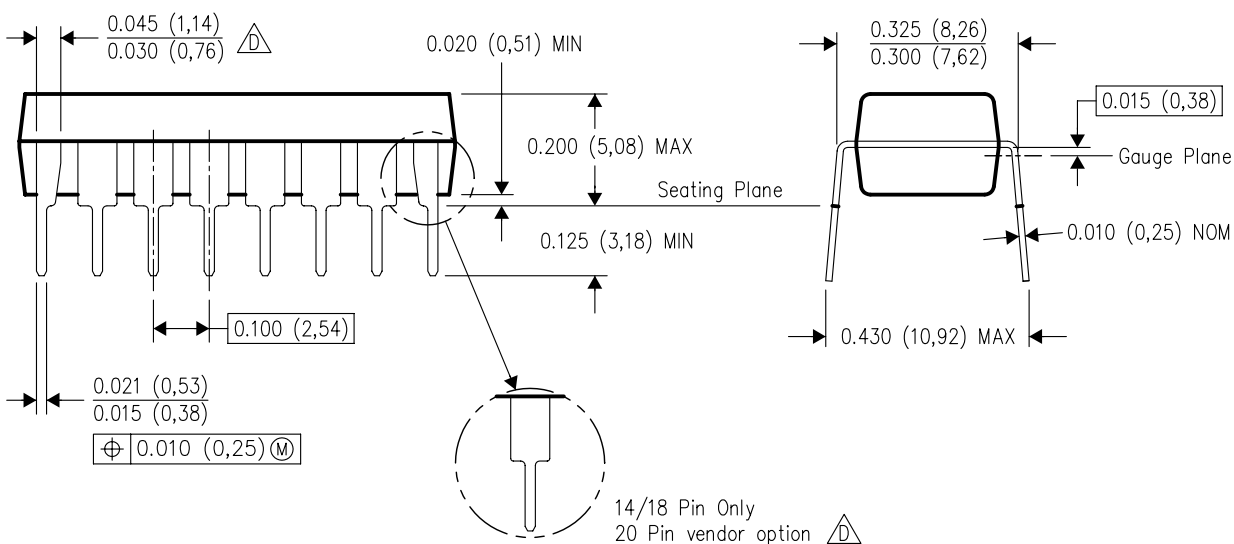
N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

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| Interface                   | <a href="http://interface.ti.com">interface.ti.com</a>             | Energy                     | <a href="http://www.ti.com/energy">www.ti.com/energy</a>                                 |
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