- **Members of the Texas Instruments** *Widebus*™ **Family**

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**

- **Flow-Through Architecture Optimizes PCB Layout**

- **Distributed V$_{CC}$ and GND Configuration Minimizes High-Speed Switching Noise**

- *EPIC*™ **(Enhanced-Performance Implanted CMOS) 1-μm Process**

- **500-mA Typical Latch-Up Immunity at 125°C**

- **Package Options Include Plastic Thin Shrink Small-Outline (DGG) Package, 300-mil Shrink Small-Outline (DL) Package Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Pin Spacings**

54AC16245 . . . WD PACKAGE
74AC16245 . . . DGG OR DL PACKAGE
(TOP VIEW)

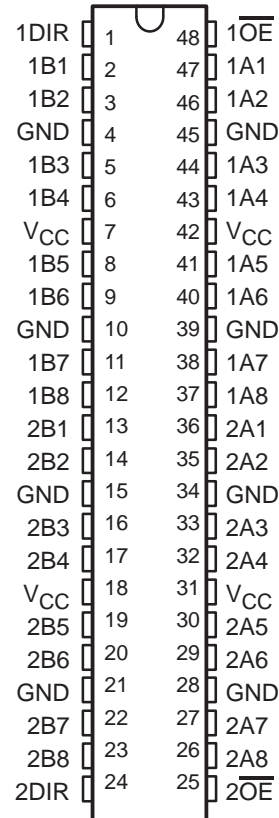|				
1DIR	1		48	1$\overline{OE}$
1B1	2		47	1A1
1B2	3		46	1A2
GND	4		45	GND
1B3	5		44	1A3
1B4	6		43	1A4
V$_{CC}$	7		42	V$_{CC}$
1B5	8		41	1A5
1B6	9		40	1A6
GND	10		39	GND
1B7	11		38	1A7
1B8	12		37	1A8
2B1	13		36	2A1
2B2	14		35	2A2
GND	15		34	GND
2B3	16		33	2A3
2B4	17		32	2A4
V$_{CC}$	18		31	V$_{CC}$
2B5	19		30	2A5
2B6	20		29	2A6
GND	21		28	GND
2B7	22		27	2A7
2B8	23		26	2A8
2DIR	24		25	2$\overline{OE}$

description

The 'AC16245 are 16-bit bus transceivers organized as dual-octal noninverting 3-state transceivers designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic level at the direction control (DIR) input. The output-enable input ($\overline{OE}$) can be used to disable the devices so that the buses are effectively isolated.

The 74AC16245 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54AC16245 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74AC16245 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

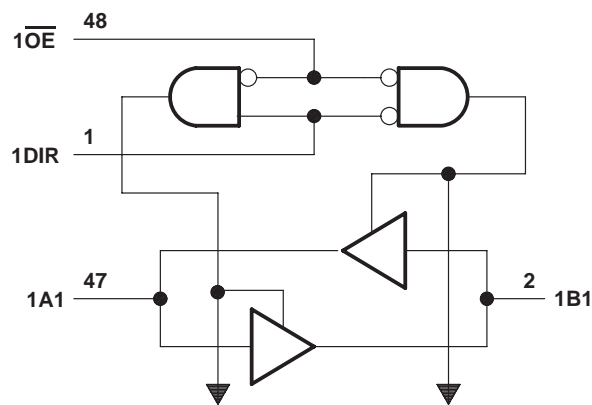| CONTROL INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to bus
H	X	Isolation

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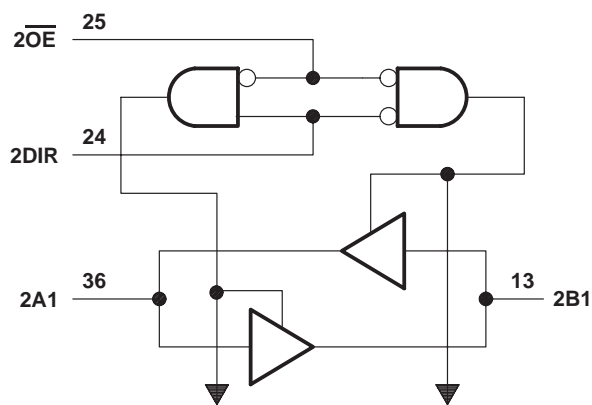
TEXAS INSTRUMENTS
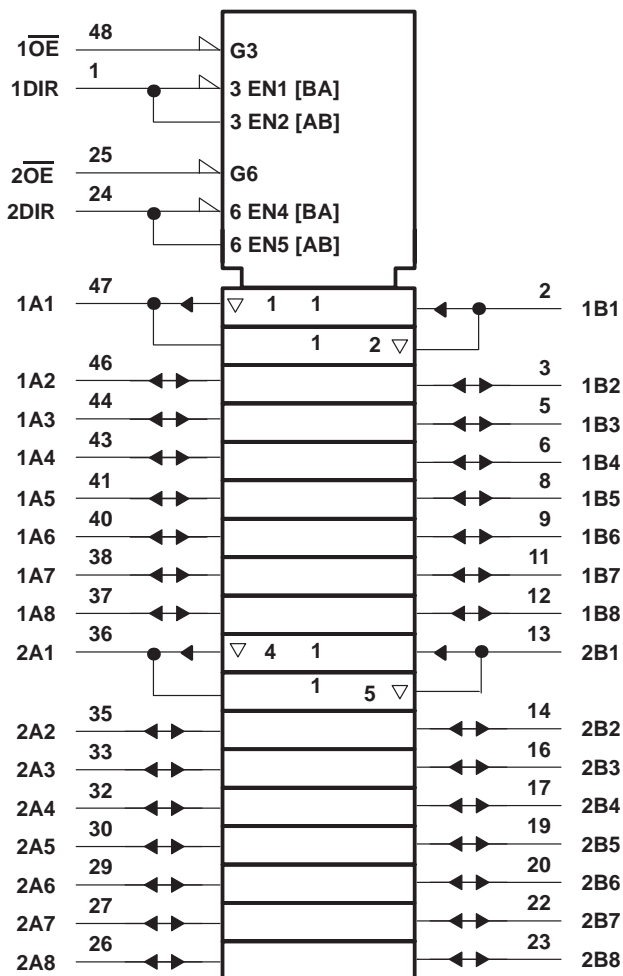
logic symbol[†]

[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

To Seven Other Transceivers

To Seven Other Transceivers

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POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) .... –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) .... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) .... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±50 mA
Continuous current through V_{CC} or GND .... ±400 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DGG package .... 0.85 W
DL package .... 1.2 W
Storage temperature range, T_{stg} .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

			54AC16245			74AC16245			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage (see Note 4)		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			2.1			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 5.5 V	3.85			3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9			0.9	V
		V_{CC} = 4.5 V			1.35			1.35	
		V_{CC} = 5.5 V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			–4			–4	mA
		V_{CC} = 4.5 V			–24			–24	
		V_{CC} = 5.5 V			–24			–24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12			12	mA
		V_{CC} = 4.5 V			24			24	
		V_{CC} = 5.5 V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		–55		125	–40		85	°C

NOTES: 3. All unused pins (input and I/O) must be held high or low to prevent them from floating.
4. All V_{CC} and GND pins must be connected to the proper voltage power supply.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	$T_A = 25°C$			54AC16245		74AC16245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$I_{OH} = -50\ \mu A$		3 V	2.9			2.9		2.9		V
			4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
	$I_{OH} = -4\ mA$		3 V	2.58			2.48		2.48		
	$I_{OH} = -24\ mA$		4.5 V	3.94			3.8		3.8		
			5.5 V	4.94			4.8		4.8		
	$I_{OH} = -75\ mA$†		5.5 V				3.85		3.85		
V_{OL}	$I_{OL} = 50\ \mu A$		3 V			0.1		0.1		0.1	V
			4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		0.1		0.1	
	$I_{OL} = 12\ mA$		3 V			0.36		0.44		0.44	
	$I_{OL} = 24\ mA$		4.5 V			0.36		0.44		0.44	
			5.5 V			0.36		0.44		0.44	
	$I_{OL} = 75\ mA$†		5.5 V					1.65		1.65	
I_I	$V_I = V_{CC}$ or GND		5.5 V			±0.1		±1		±1	μA
I_{OZ}	$V_I = V_{CC}$ or GND		5.5 V			±0.5		±5		±5	μA
I_{CC}	$V_I = V_{CC}$ or GND,	$I_O = 0$	5.5 V			8		80		80	μA
C_i	$V_I = V_{CC}$ or GND		5 V		4.5						pF
C_o	$V_I = V_{CC}$ or GND		5 V		16						

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3\ V \pm 0.3\ V$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25°C$			54AC16245		74AC16245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2.5	7.6	10.4	2.5	11.9	2.5	11.9	ns
t_{PHL}			3.1	9	12.3	3.1	13.5	3.1	13.5	
t_{PZH}	$\overline{OE}$	A or B	2.8	8.6	11.8	2.8	13.2	2.8	13.2	ns
t_{PZL}			3.9	12	16.2	3.9	18	3.9	18	
t_{PHZ}	$\overline{OE}$	A or B	5.3	8.4	10.4	5.3	11.2	5.3	11.2	ns
t_{PLZ}			4.4	7.7	9.7	4.4	10.3	4.4	10.3	

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\ V \pm 0.5\ V$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25°C$			54AC16245		74AC16245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	4.6	6.9	2	7.9	2	7.9	ns
t_{PHL}			2.5	5.2	7.9	2.5	8.9	2.5	8.9	
t_{PZH}	$\overline{OE}$	A or B	2.3	4.9	7.5	2.3	8.6	2.3	8.6	ns
t_{PZL}			3	6.2	9.5	3	10.7	3	10.7	
t_{PHZ}	$\overline{OE}$	A or B	5	7.2	9.1	5	9.8	5	9.8	ns
t_{PLZ}			4.2	6.2	8.1	4.2	8.7	4.2	8.7	

TEXAS INSTRUMENTS

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per latch	Outputs enabled	C_L = 50 pF, f = 1 MHz	43	pF
	Outputs disabled		8	

PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

VOLTAGE WAVEFORMS
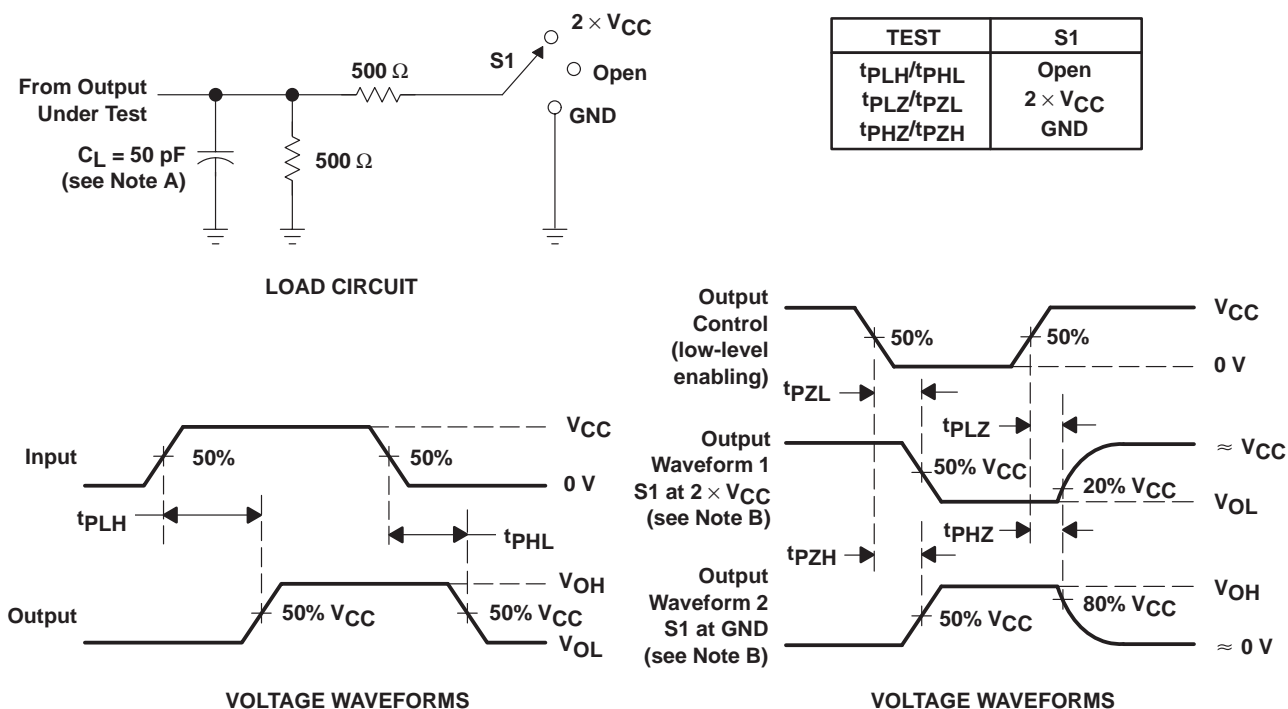
NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
      Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
   D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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