TJA1059

Dual high-speed CAN transceiver with Standby mode

Rev. 1 — 24 January 2014 Product data sheet

1. General description

The TJA1059 is a dual high-speed CAN transceiver that provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN-bus. The transceiver is designed for high-speed (up to 1 Mbit/s) CAN applications in the automotive and truck industries. It provides differential transmit and receive capabilities to (a microcontroller with) a CAN protocol controller.

The TJA1059 belongs to the third generation of high-speed CAN transceivers from NXP Semiconductors, offering significant improvements over first- and second-generation devices such as the TJA1040. It offers improved Electro Magnetic Compatibility (EMC) and ElectroStatic Discharge (ESD) performance, and also features:

- Ideal passive behavior to the CAN-bus when the supply voltage is off
- A very low-current Standby mode with bus wake-up capability on both channels
- Can be interfaced directly to microcontrollers with supply voltages from 3 V to 5 V
- Complies with global OEM requirements, allowing a one-fits-all approach

These features make the TJA1059 an excellent choice for all types of HS-CAN networks containing more than one HS-CAN interface requiring a low-power mode with wake-up capability via the CAN-bus, especially for Body Control and Gateway units.

2. Features and benefits

2.1 General

- Two TJA1049 HS-CAN transceivers combined monolithically in a single package
- Fully ISO 11898-2 and ISO 11898-5 compliant
- Suitable for 12 V and 24 V systems
- Low ElectroMagnetic Emission (EME) and high ElectroMagnetic Immunity (EMI)
- Excellent ElectroMagnetic Compatibility (EMC) performance, satisfying 'Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications', Version 1.3, May 2012.
- V_{IO} input allows for direct interfacing with 3 V to 5 V microcontrollers
- Leadless HVSON14 package (3.0 mm × 4.5 mm) with improved Automated Optical Inspection (AOI) capability
- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)

2.2 Predictable and fail-safe behavior

- Functional behavior predictable under all supply conditions

- Transceiver disengages from bus when not powered (zero load)
- Transmit Data (TXD) and bus dominant time-out functions
- Undervoltage detection on pins V_{CC} and V_{IO}
- Internal biasing of TXD1/TXD2 and STB1/STB2 input pins

2.3 Low-power management

- Very low-current Standby mode with host and bus wake-up capability
- Wake-up receiver powered by V_{IO}; allows shut down of V_{CC}

2.4 Protection

- High ESD handling capability on the bus pins
- Bus pins protected against transients in automotive environments
- Thermally protected
- High-voltage robustness on the bus pins

3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.75	-	5.25	V
I_{CC}	supply current	Standby mode	-	0.5	5	µA
		Normal mode				
		both channels recessive	-	-	20	mA
		one channel dominant	-	-	80	mA
		both channels dominant	-	90	140	mA
$V_{uvd(VCC)}$	undervoltage detection voltage on pin V_{CC}		3.5	-	4.5	V
V_{IO}	supply voltage on pin V_{IO}		2.85	-	5.25	V
I_{IO}	supply current on pin V_{IO}	Standby mode; $V_{TXD} = V_{IO}$	-	16.5	27	µA
		Normal mode				
		both channels recessive	-	-	55	µA
		one channel dominant	-	-	400	µA
		both channels dominant	-	-	600	µA
$V_{uvd(VIO)}$	undervoltage detection voltage on pin V_{IO}		1.3	2.0	2.7	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 at pins CANHx and CANLx	–6	-	+6	kV
V_{CANH}	voltage on pin CANH	pins CANH1 and CANH2; no time limit; DC limiting value	–58	-	+58	V
V_{CANL}	voltage on pin CANL	pins CANL1 and CANL2; no time limit; DC limiting value	–58	-	+58	V
T_{vj}	virtual junction temperature		–40	-	+150	°C

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TJA1059TK	HVSON14	plastic, thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 × 4.5 × 0.85 mm	SOT1086-2

5. Block diagram

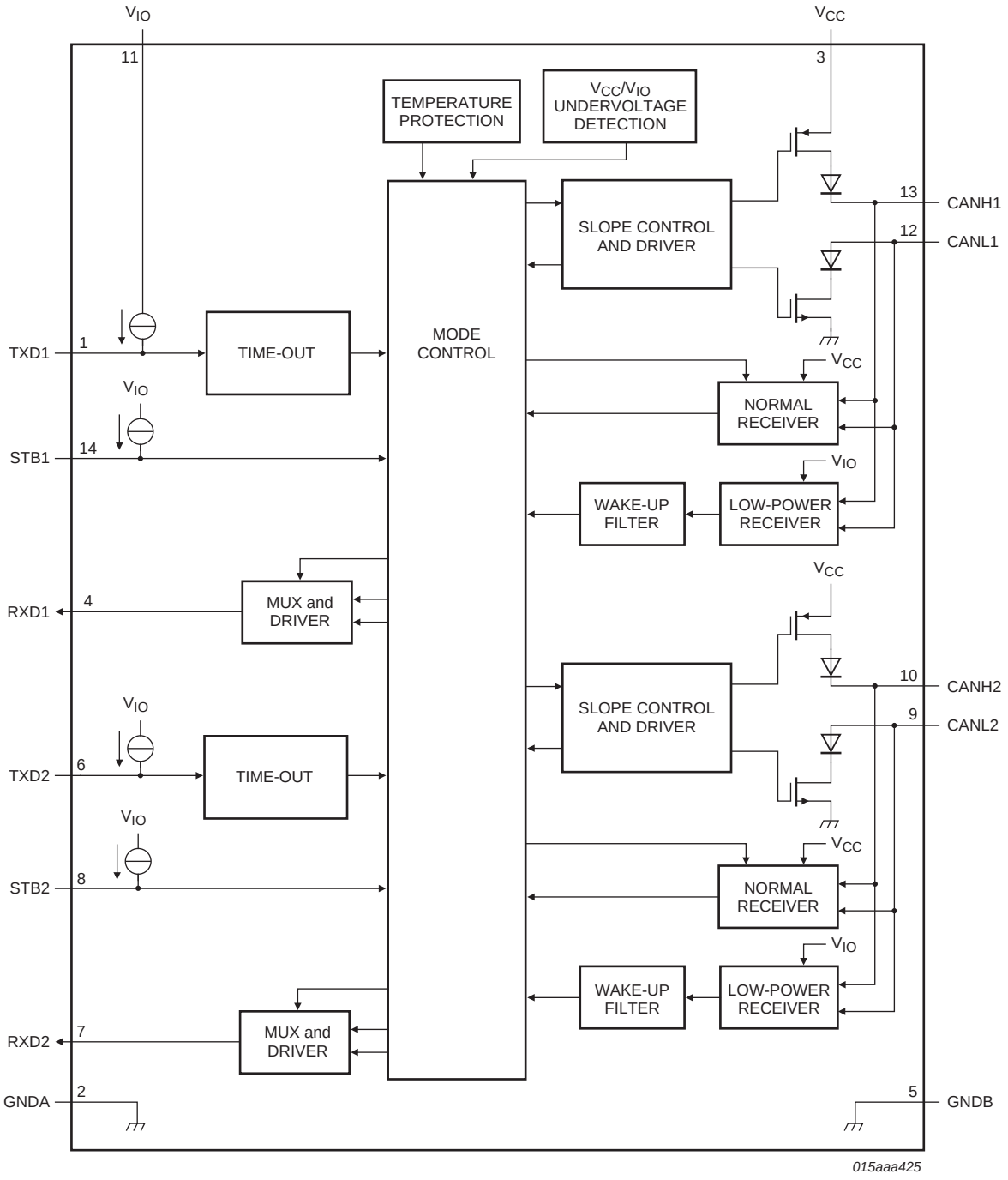


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

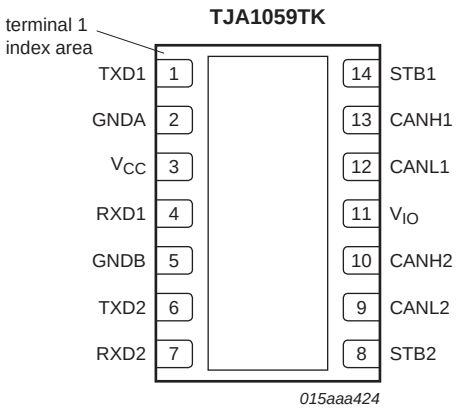


Fig 2. Pin configuration diagram

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
TXD1	1	transmit data input 1
GNDA	2[1]	ground
V_{CC}	3	transceiver supply voltage
RXD1	4	receive data output 1; reads out data from bus line1
GNDB	5[1]	ground
TXD2	6	transmit data input 2
RXD2	7	receive data output 2; reads out data from bus line 2
STB2	8	standby control input 2 (HIGH = Standby mode, LOW = Normal mode)
CANL2	9	LOW-level CAN-bus line 2
CANH2	10	HIGH-level CAN-bus line 2
V_{IO}	11	supply voltage for I/O level adapter
CANL1	12	LOW-level CAN-bus line 1
CANH1	13	HIGH-level CAN-bus line 1
STB1	14	standby control input 1 (HIGH = Standby mode, LOW = Normal mode)

[1] Pins 2 and 5 must be connected together externally in the application. The exposed die pad at the bottom of the package allows for enhanced heat dissipation and grounding from the package to the printed circuit board. Connect the exposed die pad to GND.

7. Functional description

The TJA1059 is a dual HS-CAN stand-alone transceiver with Standby mode and robust ESD handling capability. It combines the functionality of two TJA1040/TJA1049 transceivers with improved EMC and quiescent current performance. Improved slope control and high DC handling capability on the bus pins provide additional application flexibility.

7.1 Operating modes

The TJA1059 supports two operating modes per transceiver, Normal and Standby. The operating mode can be selected independently for each transceiver via pins STB1 and STB2 (see Table 4).

Table 4. Operating modes

Mode	Pin STB1/STB2	Pin RXD1/RXD2	
		LOW	HIGH
Normal	LOW	bus dominant	bus recessive
Standby	HIGH	wake-up request detected	no wake-up request detected

7.1.1 Normal mode

A LOW level on pin STB1/STB2 selects Normal mode. In this mode, the transceiver can transmit and receive data via the bus lines CANH1/CANL1 and CANH2/CANL2 (see Figure 1 for the block diagram). The differential receiver converts the analog data on the bus lines into digital data which is output on pin RXD1/RXD2. The slope of the output signals on the bus lines is controlled and optimized in a way that guarantees the lowest possible EME.

7.1.2 Standby mode

A HIGH level on pin STB1/STB2 selects Standby mode. In Standby mode, the transceiver is not able to transmit or correctly receive data via the bus lines. The transmitter and Normal-mode receiver blocks are switched off to reduce supply current, and only a low-power differential receiver monitors the bus lines for activity.

In Standby mode, the bus lines are biased to ground to minimize the system supply current. The low-power receiver is supplied by V_{IO} and can detect CAN-bus activity even if V_{IO} is the only supply voltage available. When pin RXD1/RXD2 goes LOW to signal a wake-up request, a transition to Normal mode is not triggered until STB1/STB2 is forced LOW.

A dedicated wake-up sequence (specified in ISO11898-5) must be received before the TJA1059 outputs the bus signals on RXD1/RXD2. This filtering is necessary to avoid spurious wake-up events due to a dominant clamped CAN-bus or dominant phases caused by noise or spikes on the bus.

A valid wake-up pattern consists of:

A dominant phase of at least $t_{wake(busdom)}$ followed by

A recessive phase of at least $t_{wake(busrec)}$ followed by

A dominant phase of at least $t_{wake(busdom)}$

The complete dominant-recessive-dominant pattern must be received within $t_{to(wake)bus}$ to be recognized as a valid wake-up pattern (see Figure 3). Pin RXD1/RXD2 remains recessive until the wake-up event has been triggered.

After a wake-up sequence has been detected, the TJA1059 remains in Standby mode with the bus signals reflected on RXD1/RXD2. Note that dominant or recessive phases lasting less than $t_{fltr(wake)bus}$ are not detected by the low-power differential receiver and will not be reflected on RXD1/RXD2 in Standby mode.

A wake-up event is not registered if any of the following events occur while a wake-up sequence is being transmitted:

- the TJA1059 switches to Normal mode
- the complete wake-up pattern was not received within $t_{to(wake)bus}$
- a V_{IO} undervoltage is detected ($V_{IO} < V_{uvd(VIO)}$; see Section 7.2.3)

If any of these events occur while a wake-up sequence is being received, the internal wake-up logic is reset. The complete wake-up sequence will need to be retransmitted to trigger a wake-up event.

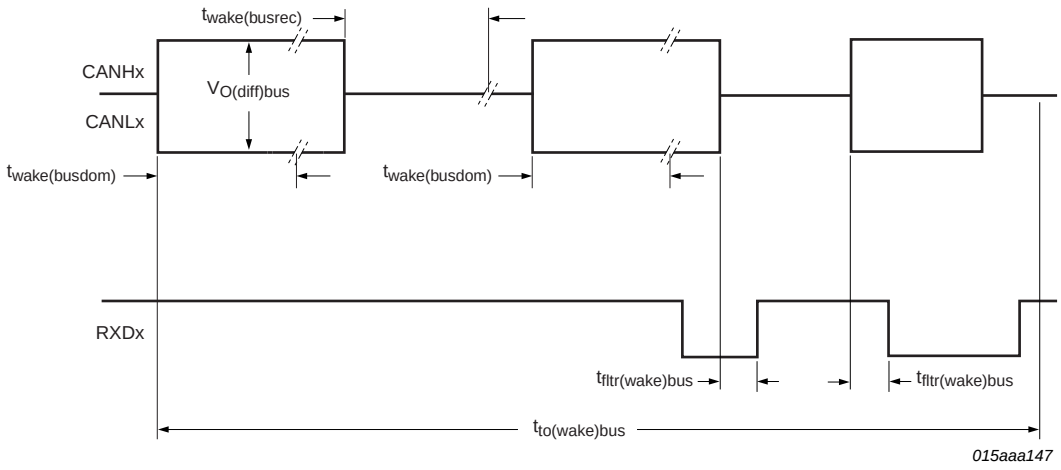


Fig 3. Wake-up timing

7.2 Fail-safe features

7.2.1 TXD dominant time-out function

A 'TXD dominant time-out' timer is started when pin TXD1/TXD2 is set LOW. If the LOW state on this pin persists for longer than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD1/TXD2 is set HIGH. The TXD dominant time-out time also defines the minimum possible bit rate of 40 kbit/s. The TJA1059 has two TXD dominant time-out timers that operate independently of each other.

7.2.2 Internal biasing of TXD1, TXD2, STB1 and STB2 input pins

Pins TXD1, TXD2, STB1 and STB2 have internal pull-ups to V_{IO}. The pull-ups ensure a safe, defined state if any of these pins are left floating. Pins GNDA and GNDB must be connected together in the application.

Pull-up currents flow in these pins in all states. Pins TXD1, TXD2, STB1 and STB2 should be held HIGH in Standby mode to minimize standby currents.

7.2.3 Undervoltage detection on pins V_{CC} and V_{IO}

Should V_{CC} drop below the V_{CC} undervoltage detection level, $V_{uvd(VCC)}$, both transceivers will switch to Standby mode. The logic state of pins STB1 and STB2 is ignored until V_{CC} has recovered.

Should V_{IO} drop below the V_{IO} undervoltage detection level, $V_{uvd(VIO)}$, the transceivers will switch off and disengage from the bus (zero load) until V_{IO} has recovered.

7.2.4 Overtemperature protection

The output drivers are protected against overtemperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature, $T_{j(sd)}$, both output drivers are disabled. When the virtual junction temperature drops below $T_{j(sd)}$ again, the output drivers will recover independently once TXD1/TXD2 have been reset to HIGH. Including the TXD1/TXD2 condition prevents output driver oscillation due to small variations in temperature.

7.3 V_{IO} supply pin

Pin V_{IO} should be connected to the microcontroller supply voltage (see Figure 5). This adjusts the signal levels of pins TXD1, TXD2, RXD1, RXD2, STB1 and STB2 to the I/O levels of the microcontroller. Pin V_{IO} also provides the internal supply voltage for the low-power differential receiver of the transceiver. It allows applications running in low-power mode to monitor the bus lines for activity, even if there is no supply voltage on pin V_{CC}.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to GND.

Symbol	Parameter	Conditions		Min	Max	Unit
V_x	voltage on pin x	no time limit; DC value				
		on pins CANH1, CANL1, CANH2 and CANL2		−58	+58	V
		on any other pin		−0.3	+7	V
V_{trt}	transient voltage	on pins CANH1, CANL1, CANH2 and CANL2	[1]	−150	+100	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2	[2]			
		on pins CANH1, CANL1, CANH2 and CANL2	[3]	−6	+6	kV
		HBM	[4]			
		on pins CANH1, CANL1, CANH2 and CANL2		−6	+6	kV
		at any other pin		−4	+4	kV
		MM	[5]			
		at any pin		−300	+300	V
		CDM	[6]			
		at corner pins		−750	+750	V
		at any pin		−500	+500	V
T_{vj}	virtual junction temperature		[7]	−40	+150	°C
T_{stg}	storage temperature			−55	+150	°C

[1] Verified by an external test house to ensure pins CANH1, CANL1, CANH2 and CANL2 can withstand ISO7637 part 1 and 2 automotive transient test pulses.

[2] IEC 61000-4-2 (150 pF, 330 Ω).

[3] ESD performance of pins CANH1, CANL1, CANH2 and CANL2 according to IEC 61000-4-2 (150 pF, 330 Ω) has been be verified by an external test house.

[4] Human Body Model (HBM): according to AEC-Q100-002 (100 pF, 1.5 kΩ).

[5] Machine Model (MM): according to AEC-Q100-003 (200 pF, 0.75 μH, 10 Ω).

[6] Charged Device Model (CDM): according to AEC-Q100-011 (field Induced charge; 4 pF).

[7] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(vj-a)}$, where $R_{th(vj-a)}$ is a fixed value to be used for the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	HVSON14; single-layer board	[1]	73	K/W
		HVSON14; four-layer board	[2]	42	K/W

[1] According to JEDEC JESD51-2 and JESD51-3 at natural convection on 1s board.

[2] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 μm) and thermal via array under the exposed pad connected to the first inner copper layer.

10. Static characteristics

Table 7. Static characteristics

T_{vj} = −40 °C to +150 °C, V_{CC} = 4.75 V to 5.25 V, V_{IO} = 2.85 V to 5.25 V and R_L = 60 Ω unless specified otherwise. All voltages are defined with respect to ground. Positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin V_{CC}						
V_{CC}	supply voltage		4.75	-	5.25	V
$V_{uvd(VCC)}$	undervoltage detection voltage on pin V_{CC}		3.5	-	4.5	V
I_{CC}	supply current	Standby mode; $V_{TXD} = V_{IO}$	-	0.5	5	µA
		Normal mode				
		both channels recessive	-	-	20	mA
		one channel dominant	-	-	80	mA
		both channels dominant	-	90	140	mA
I/O level adapter supply; pin V_{IO}						
V_{IO}	supply voltage on pin V_{IO}		2.85	-	5.25	V
$V_{uvd(VIO)}$	undervoltage detection voltage on pin V_{IO}		1.3	2.0	2.7	V
I_{IO}	supply current on pin V_{IO}	Standby mode; $V_{TXD} = V_{IO}$	-	16.5	27	µA
		Normal mode				
		both channels recessive	-	-	55	µA
		one channel dominant	-	-	400	µA
		both channels dominant	-	-	600	µA
Standby mode control input; pins STB1 and STB2						
V_{IH}	HIGH-level input voltage		$0.7V_{IO}$	-	V_{IO} + 0.3	V
V_{IL}	LOW-level input voltage		−0.3	-	$0.3V_{IO}$	V
I_{IH}	HIGH-level input current	V_{STB}[1] = V_{IO}	−5	-	+5	µA
I_{IL}	LOW-level input current	V_{STB} = 0 V	−15	-	−1	µA
CAN transmit data input; pins TXD1 and TXD2						
V_{IH}	HIGH-level input voltage		$0.7V_{IO}$	-	V_{IO} + 0.3	V
V_{IL}	LOW-level input voltage		−0.3	-	$0.3V_{IO}$	V
I_{IH}	HIGH-level input current	V_{TXD}[2] = V_{IO}	−5	-	+5	µA
I_{IL}	LOW-level input current	V_{TXD} = 0 V	−260	−150	−30	µA
C_i	input capacitance	[3]	-	5	10	pF
CAN receive data output; pins RXD1 and RXD2						
I_{OH}	HIGH-level output current	V_{RXD}[4] = V_{IO} − 0.4 V; $V_{IO} = V_{CC}$	−8	−3	−1	mA
I_{OL}	LOW-level output current	V_{RXD} = 0.4 V; bus dominant	1	-	12	mA
Bus lines; pins CANH1, CANL1, CANH2 and CANL2						
$V_{O(dom)}$	dominant output voltage	V_{TXD} = 0 V; t < $t_{to(dom)TXD}$				
		pin CANH1/CANH2	2.75	3.5	4.5	V
		pin CANL1/CANL2	0.5	1.5	2.25	V

Table 7. Static characteristics *...continued*

T_{vj} = −40 °C to +150 °C, V_{CC} = 4.75 V to 5.25 V, V_{IO} = 2.85 V to 5.25 V and R_L = 60 Ω unless specified otherwise. All voltages are defined with respect to ground. Positive currents flow into the IC.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{dom(TX)sym}$	transmitter dominant voltage symmetry	$V_{dom(TX)sym} = V_{CC} - V_{CANH}$ [5] $- V_{CANL}$ [6]		−400	-	+400	mV
$V_{O(dif)bus}$	bus differential output voltage	V_{TXD} = 0 V; $t < t_{to(dom)TXD}$ V_{CC} = 4.75 V to 5.25 V; R_L = 45 Ω to 65 Ω		1.5	-	3	V
		$V_{TXD} = V_{IO}$; recessive; no load		−50	-	+50	mV
$V_{O(rec)}$	recessive output voltage	Normal mode; $V_{TXD} = V_{IO}$; no load		2	$0.5V_{CC}$	3	V
		Standby mode; no load		−0.1	-	+0.1	V
$V_{th(RX)dif}$	differential receiver threshold voltage	Normal mode; $V_{cm(CAN)}$ = −12 V to +12 V	[7]	0.5	0.7	0.9	V
		Standby mode $V_{cm(CAN)}$ = −12 V to +12 V	[7]	0.4	0.7	1.15	V
$V_{hys(RX)dif}$	differential receiver hysteresis voltage	Normal mode; $V_{cm(CAN)}$ = −12 V to +12 V	[7]	100	-	300	mV
$I_{O(dom)}$	dominant output current	V_{TXD} = 0 V; $t < t_{to(dom)TXD}$; V_{CC} = 5 V					
		pin CANH1/CANH2; V_{CANH} = 0 V		−100	−70	−40	mA
		pin CANL1/CANL2; V_{CANL} = 5 V/40 V		40	70	100	mA
$I_{O(rec)}$	recessive output current	Normal mode; $V_{TXD} = V_{IO}$ $V_{CANH} = V_{CANL}$ = −40 V to +40 V		−5	-	+5	mA
I_L	leakage current	$V_{CC} = V_{IO}$ = 0 V or $V_{CC} = V_{IO}$ = shorted to ground via 47 kΩ; $V_{CANH} = V_{CANL}$ = 5 V		−5	-	+5	µA
R_i	input resistance			9	15	28	kΩ
ΔR_i	input resistance deviation	between pin CANH1/CANH2 and pin CANL1/CANL2		−3	-	+3	%
$R_{i(dif)}$	differential input resistance			19	30	52	kΩ
$C_{i(cm)}$	common-mode input capacitance		[3]	-	-	20	pF
$C_{i(dif)}$	differential input capacitance		[3]	-	-	10	pF
Temperature detection							
$T_{j(sd)}$	shutdown junction temperature		[3]	-	190	-	°C

[1] STB refers to the input signal on pin STB1 or pin STB2.

[2] TXD refers to the input signal on pin TXD1 or pin TXD2.

[3] Not tested in production.

[4] RXD refers to the output signal on pin RXD1 or pin RXD2.

[5] CANH refers to the input/output signal on pin CANH1 or pin CANH2.

[6] CANL refers to the input/output signal on pin CANL1 or pin CANL2.

[7] $V_{cm(CAN)}$ is the common mode voltage of CANH1/CANL1 and CANH2/CANL2.

11. Dynamic characteristics

Table 8. Dynamic characteristics

T_{vj} = −40 °C to +150 °C, V_{CC} = 4.75 V to 5.25 V, V_{IO} = 2.85 V to 5.25 V and R_L = 60 Ω unless specified otherwise. All voltages are defined with respect to ground;. Positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Transceiver timing; pins CANH1, CANH2, CANL1, CANL2, TXD1, TXD2, RXD1 and RXD2; see Figure 4 and Figure 6						
$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant	Normal mode	-	65	140	ns
$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive	Normal mode	-	90	140	ns
$t_{d(busdom-RXD)}$	delay time from bus dominant to RXD	Normal mode	-	60	140	ns
$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD	Normal mode	-	65	140	ns
$t_{PD(TXD-RXD)}$	propagation delay from TXD to RXD	Normal mode	60	-	250	ns
$t_{to(dom)TXD}$	TXD dominant time-out time	V_{TXD} = 0 V; Normal mode	0.5	2	5	ms
$t_{d(stb-norm)}$	standby to normal mode delay time		7	25	47	µs
$t_{wake(busdom)}$	bus dominant wake-up time	Standby mode	0.5	-	5	µs
$t_{wake(busrec)}$	bus recessive wake-up time	Standby mode	0.5	-	5	µs
$t_{to(wake)bus}$	bus wake-up time-out time		0.5	2	5	ms
$t_{fltr(wake)bus}$	bus wake-up filter time	Standby mode	0.5	1.5	5	µs

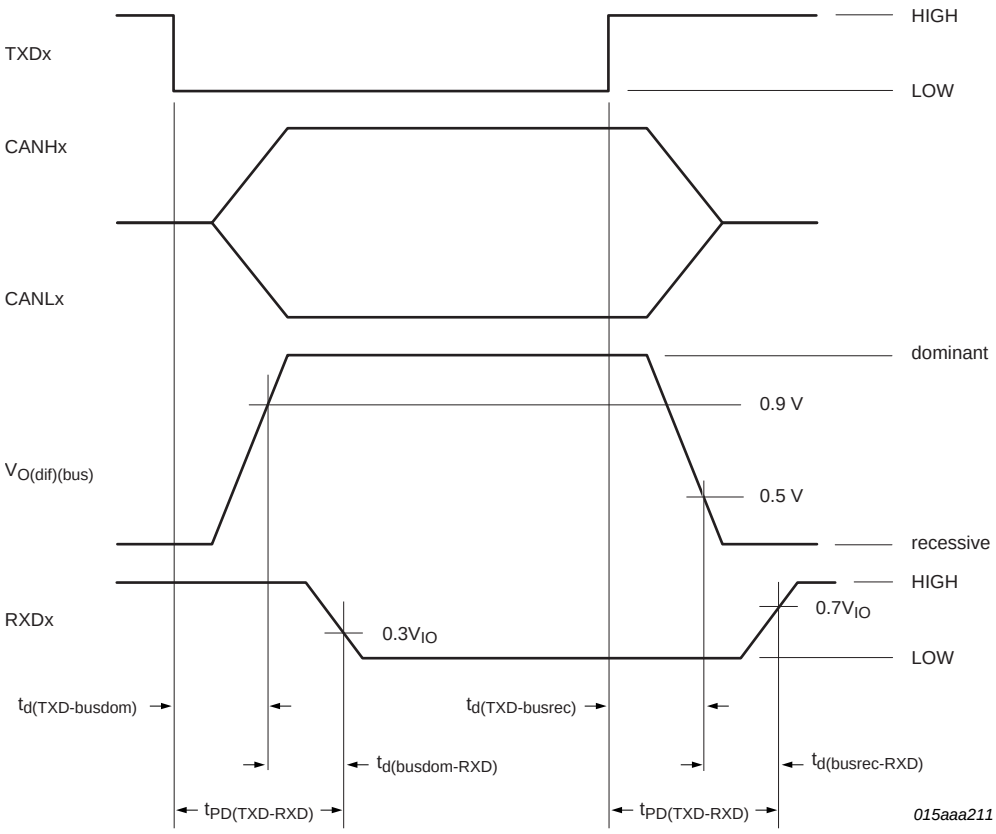
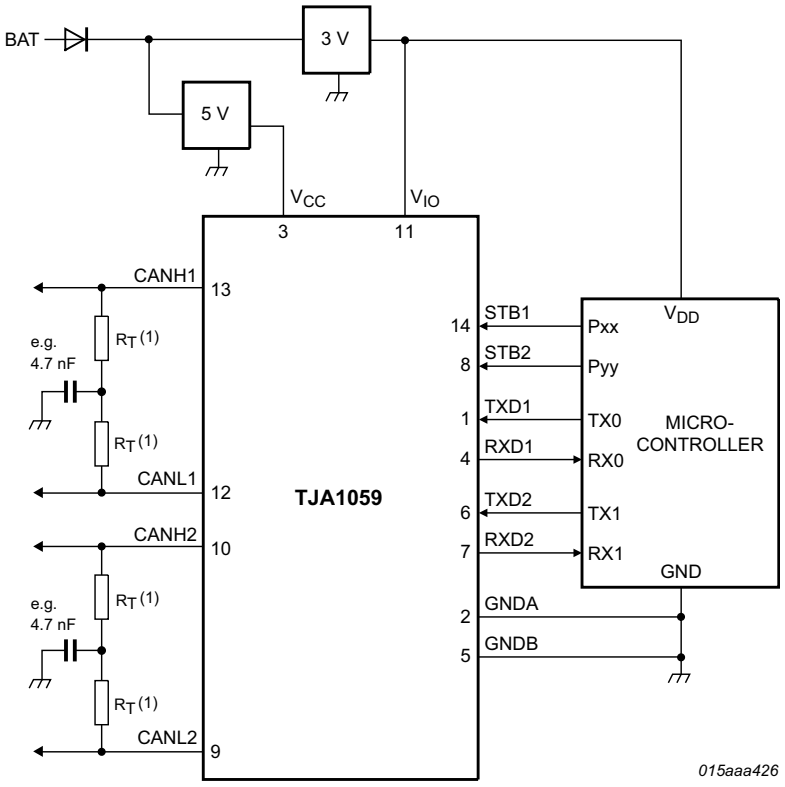


Fig 4. CAN transceiver timing diagram

12. Application information



(1) For bus line end nodes, R_T = 60 Ω in order to support the 'split termination concept'. For sub-nodes, an optional 'weak' termination of e.g. R_T = 1.3 kΩ can be used, if required by the OEM.

Fig 5. Typical application with 3 V microcontroller

13. Test information

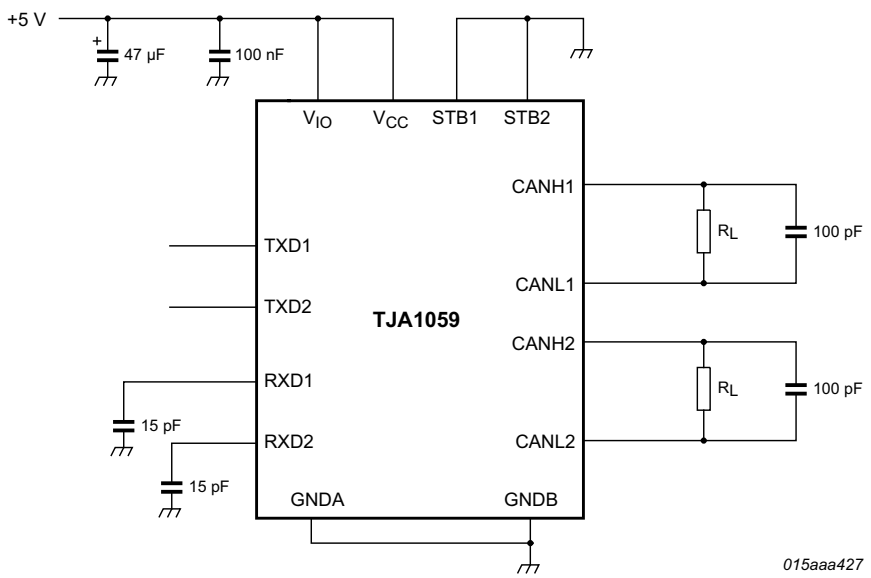


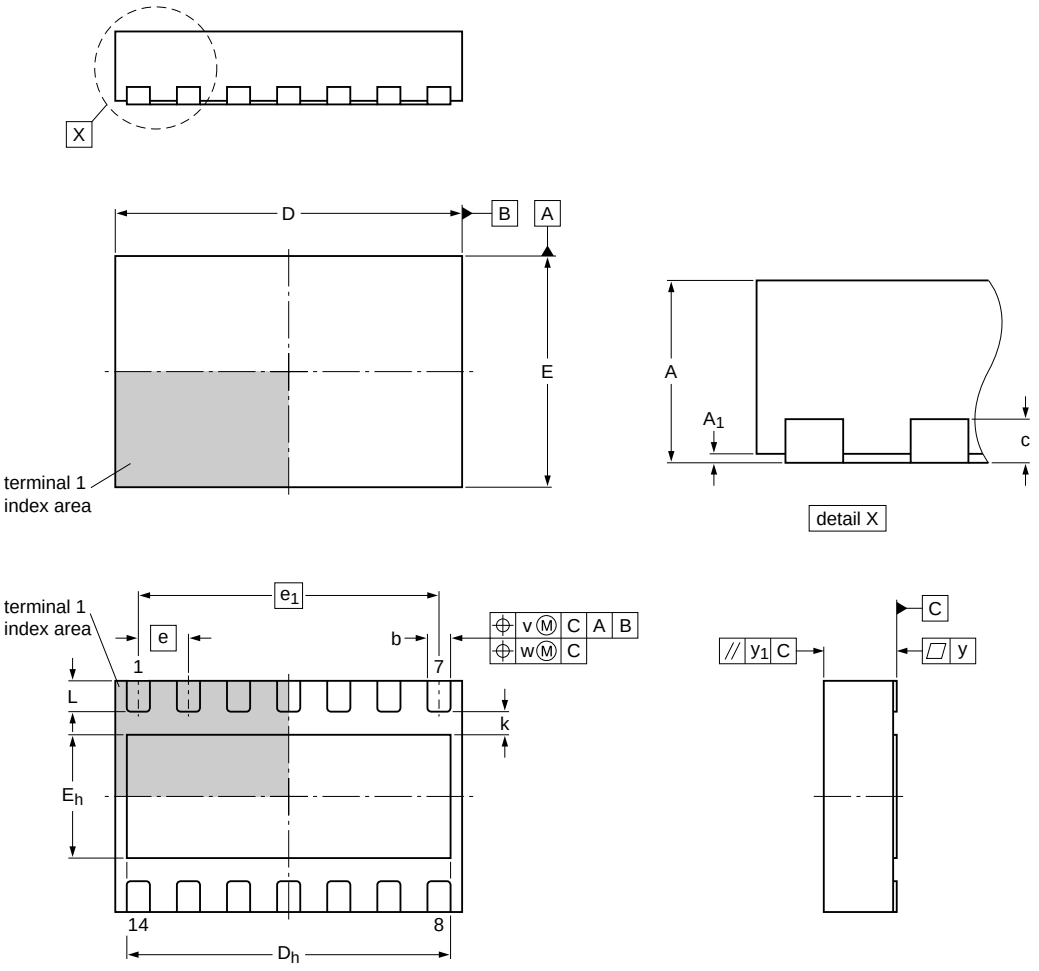
Fig 6. Timing test circuit for CAN transceiver

13.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 Rev-G - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

14. Package outline

HVSON14: plastic, thermal enhanced very thin small outline package; no leads; 14 terminals; body 3 x 4.5 x 0.85 mm **SOT1086-2**



Dimensions

Unit		A	A_1	b	c	D	D_h	E	E_h	e	e_1	k	L	v	w	y	y_1
mm	max	1.00	0.05	0.35		4.6	4.25	3.1	1.65			0.35	0.45				
	nom	0.85	0.03	0.32	0.2	4.5	4.20	3.0	1.60	0.65	3.9	0.30	0.40	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.29		4.4	4.15	2.9	1.55			0.25	0.35				

sot1086-2

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1086-2	- - -	MO-229	- - -			~~10-07-14~~ 10-07-15

Fig 7. Package outline SOT1086 (HVSON14)

15. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 8) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 9 and 10

Table 9. SnPb eutectic process (from J-STD-020D)

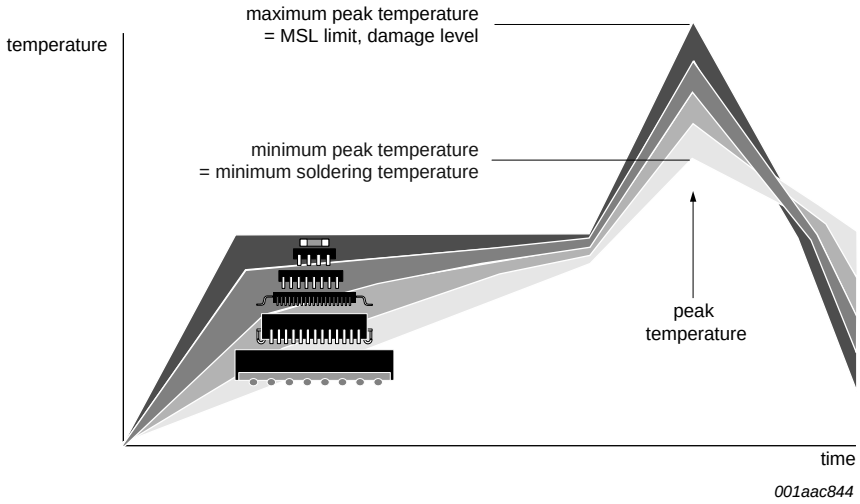
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 10. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 8.



MSL: Moisture Sensitivity Level

Fig 8. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17. Soldering of HVSON packages

Section 16 contains a brief introduction to the techniques most commonly used to solder Surface Mounted Devices (SMD). A more detailed discussion on soldering HVSON leadless package ICs can found in the following application notes:

- *AN10365 'Surface mount reflow soldering description"*
- *AN10366 "HVQFN application information"*

18. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TJA1059 v.1	20140124	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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