

R1LV0416D Series

4M SRAM (256-kword $\times$ 16-bit)

REJ03C0311-0100

Rev.1.00

May.24.2007

Description

The R1LV0416D is a 4-Mbit static RAM organized 256-kword $\times$ 16-bit, fabricated by Renesas's high-performance 0.15 μ m CMOS and TFT technologies. R1LV0416D Series has realized higher density, higher performance and low power consumption. The R1LV0416D Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. The R1LV0416D Series is packaged in a 44-pin thin small outline mount device, or a 48-ball fine pitch ball grid array.

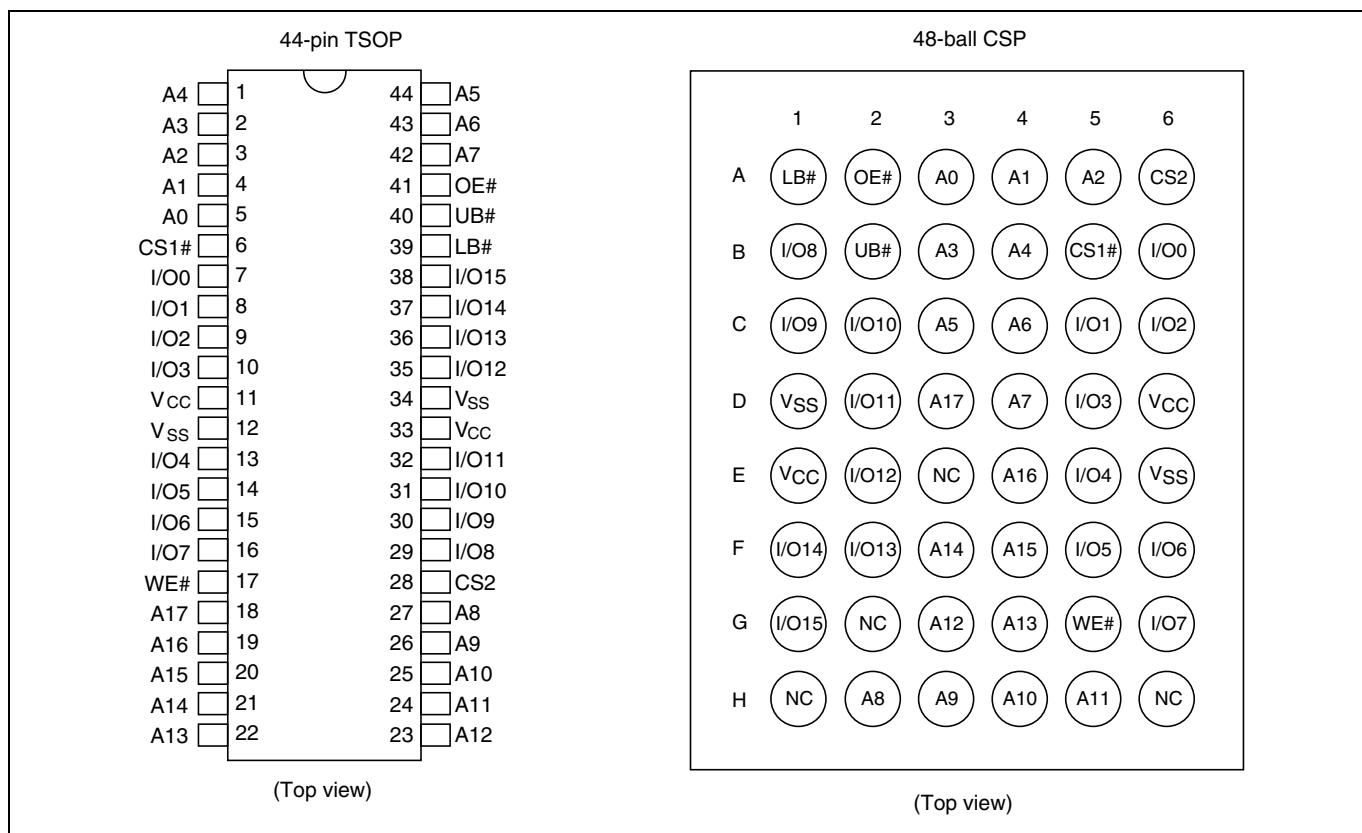
Features

- Single 3.0 V supply: 2.7 V to 3.6 V
- Fast access time: 55/70 ns (max)
- Power dissipation:
 - Standby: 3 μ W (typ) ($V_{CC} = 3.0$ V)
- Equal access and cycle times
- Common data input and output.
 - Three state output
- Battery backup operation.
 - 2 chip selection for battery backup
- Temperature Range: -40 to +85°C

Ordering Information

Type No.	Access time	Package
R1LV0416DSB-5SI	55 ns	400-mil 44-pin plastic TSOP II PTSB0044GA-A (44P3W-H)
R1LV0416DSB-7LI	70 ns	
R1LV0416DBG-5SI	55 ns	48-ball CSP with 0.75 mm ball pitch PTBG0048HB-A (48FHH)
R1LV0416DBG-7LI	70 ns	

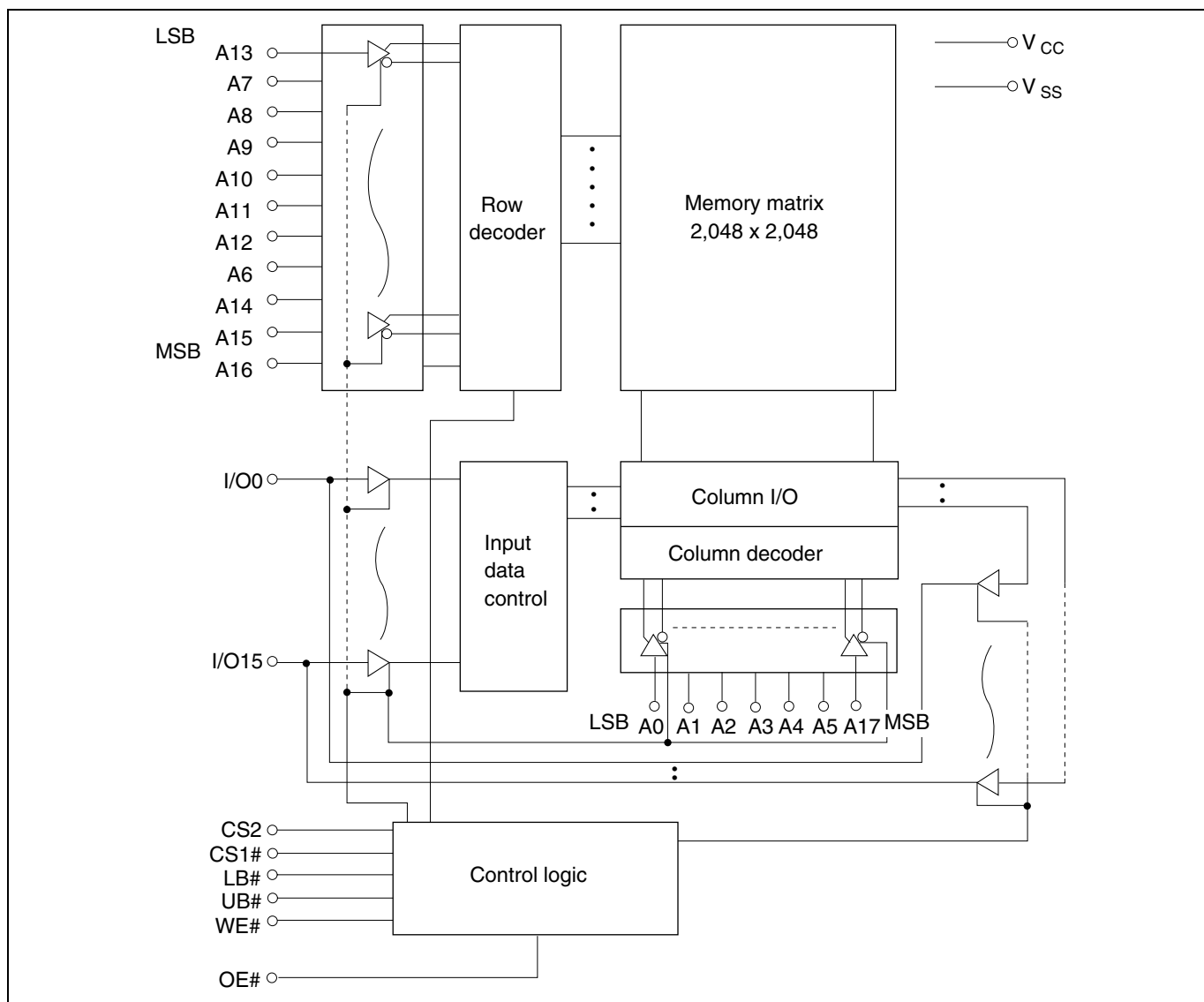
Pin Arrangement



Pin Description

Pin name	Function
A0 to A17	Address input
I/O0 to I/O15	Data input/output
CS1# ($\overline{\text{CS1}}$)	Chip select 1
CS2	Chip select 2
OE# ($\overline{\text{OE}}$)	Output enable
WE# ($\overline{\text{WE}}$)	Write enable
LB# ($\overline{\text{LB}}$)	Lower byte select
UB# ($\overline{\text{UB}}$)	Upper byte select
V _{cc}	Power supply
V _{ss}	Ground
NC	No connection

Block Diagram



Operation Table

CS1#	CS2	WE#	OE#	UB#	LB#	I/O0 to I/O7	I/O8 to I/O15	Operation
H	×	×	×	×	×	High-Z	High-Z	Standby
×	L	×	×	×	×	High-Z	High-Z	Standby
×	×	×	×	H	H	High-Z	High-Z	Standby
L	H	H	L	L	L	Dout	Dout	Read
L	H	H	L	H	L	Dout	High-Z	Lower byte read
L	H	H	L	L	H	High-Z	Dout	Upper byte read
L	H	L	×	L	L	Din	Din	Write
L	H	L	×	H	L	Din	High-Z	Lower byte write
L	H	L	×	L	H	High-Z	Din	Upper byte write
L	H	H	H	×	×	High-Z	High-Z	Output disable

Note: H: V_{IH} , L: V_{IL} , ×: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Terminal voltage on any pin relative to V_{SS}	V_T	-0.5* ¹ to $V_{CC} + 0.3$ * ²	V
Power dissipation	P_T	0.7	W
Operating temperature ¹	Topr	-40 to +85	°C
Storage temperature range	Tstg	-65 to +150	°C
Storage temperature range under bias	Tbias	-40 to +85	°C

Notes: 1. V_T min: -3.0 V for pulse half-width ≤ 30 ns.

2. Maximum voltage is +4.6 V.

DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	2.7	3.0	3.6	V	
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.2	—	$V_{CC} + 0.3$	V	
Input low voltage	V_{IL}	-0.3	—	0.6	V	1
Ambient temperature range	Ta	-40	—	+85	°C	

Note: 1. V_{IL} min: -3.0 V for pulse half-width ≤ 30 ns.

DC Characteristics

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current			$ I_{LI} $	—	—	1	μA	$V_{in} = V_{SS}$ to V_{CC}
Output leakage current			$ I_{LO} $	—	—	1	μA	CS1# = V_{IH} or CS2 = V_{IL} or OE# = V_{IH} or WE# = V_{IL} or LB# = UB# = V_{IH} , $V_{IO} = V_{SS}$ to V_{CC}
Operating current			I_{CC}	—	—	20	mA	CS1# = V_{IL} , CS2 = V_{IH} , Others = V_{IH}/V_{IL} , $I_{IO} = 0$ mA
Average operating current			I_{CC1}	—	—	25	mA	Min. cycle, duty = 100%, $I_{IO} = 0$ mA, CS1# = V_{IL} , CS2 = V_{IH} , Others = V_{IH}/V_{IL}
			I_{CC2}	—	—	5	mA	Cycle time = 1 μs , duty = 100%, $I_{IO} = 0$ mA, CS1# ≤ 0.2 V, CS2 $\geq V_{CC} - 0.2$ V $V_{IH} \geq V_{CC} - 0.2$ V, $V_{IL} \leq 0.2$ V
Standby current			I_{SB}	—	0.1* ¹	0.3	mA	CS2 = V_{IL}
Standby current	-5SI	to +85°C	I_{SB1}	—	—	10	μA	$V_{in} \geq 0$ V
		to +70°C	I_{SB1}	—	—	8	μA	(1) $0\text{ V} \leq \text{CS2} \leq 0.2\text{ V}$ or
		to +40°C	I_{SB1}	—	—	3	μA	(2) CS1# $\geq V_{CC} - 0.2\text{ V}$,
		to +25°C	I_{SB1}	—	1* ¹	2.5	μA	CS2 $\geq V_{CC} - 0.2\text{ V}$ or
	-7LI	to +85°C	I_{SB1}	—	—	20	μA	(3) LB# = UB# $\geq V_{CC} - 0.2\text{ V}$,
		to +70°C	I_{SB1}	—	—	16	μA	CS2 $\geq V_{CC} - 0.2\text{ V}$,
		to +40°C	I_{SB1}	—	—	10	μA	CS1# $\leq 0.2\text{ V}$
		to +25°C	I_{SB1}	—	1* ¹	10	μA	Average values
Output high voltage			V_{OH}	2.4	—	—	V	$I_{OH} = -1\text{ mA}$
			V_{OH2}	$V_{CC} - 0.2$	—	—	V	$I_{OH} = -100\text{ }\mu A$
Output low voltage			V_{OL}	—	—	0.4	V	$I_{OL} = 2\text{ mA}$
			V_{OL2}	—	—	0.2	V	$I_{OL} = 100\text{ }\mu A$

Note: 1. Typical values are at $V_{CC} = 3.0$ V, $T_a = +25^\circ C$ and specified loading, and not guaranteed.

Capacitance

($T_a = +25^\circ C$, $f = 1.0$ MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	C_{in}	—	—	8	pF	$V_{in} = 0$ V	1
Input/output capacitance	C_{IO}	—	—	10	pF	$V_{IO} = 0$ V	1

Note: 1. This parameter is sampled and not 100% tested.

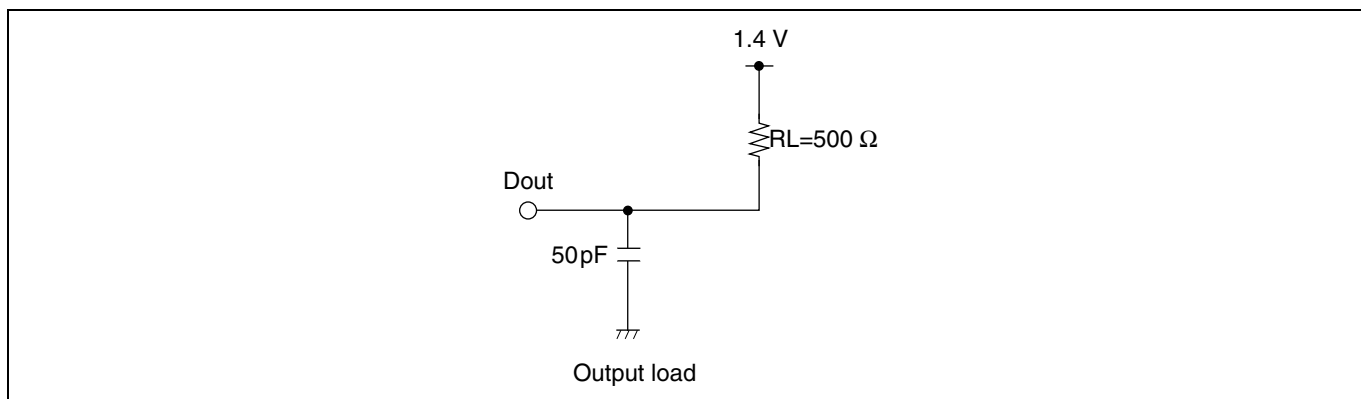
AC Characteristics

($T_a = -40$ to $+85^{\circ}\text{C}$, $V_{CC} = 2.7$ V to 3.6 V)

Test Conditions

Input pulse levels: $V_{IL} = 0.4$ V, $V_{IH} = 2.4$ V

- Input rise and fall time: 5 ns
- Input/output timing reference levels: 1.4 V
- Output load: See figures (Including scope and jig)



Read Cycle

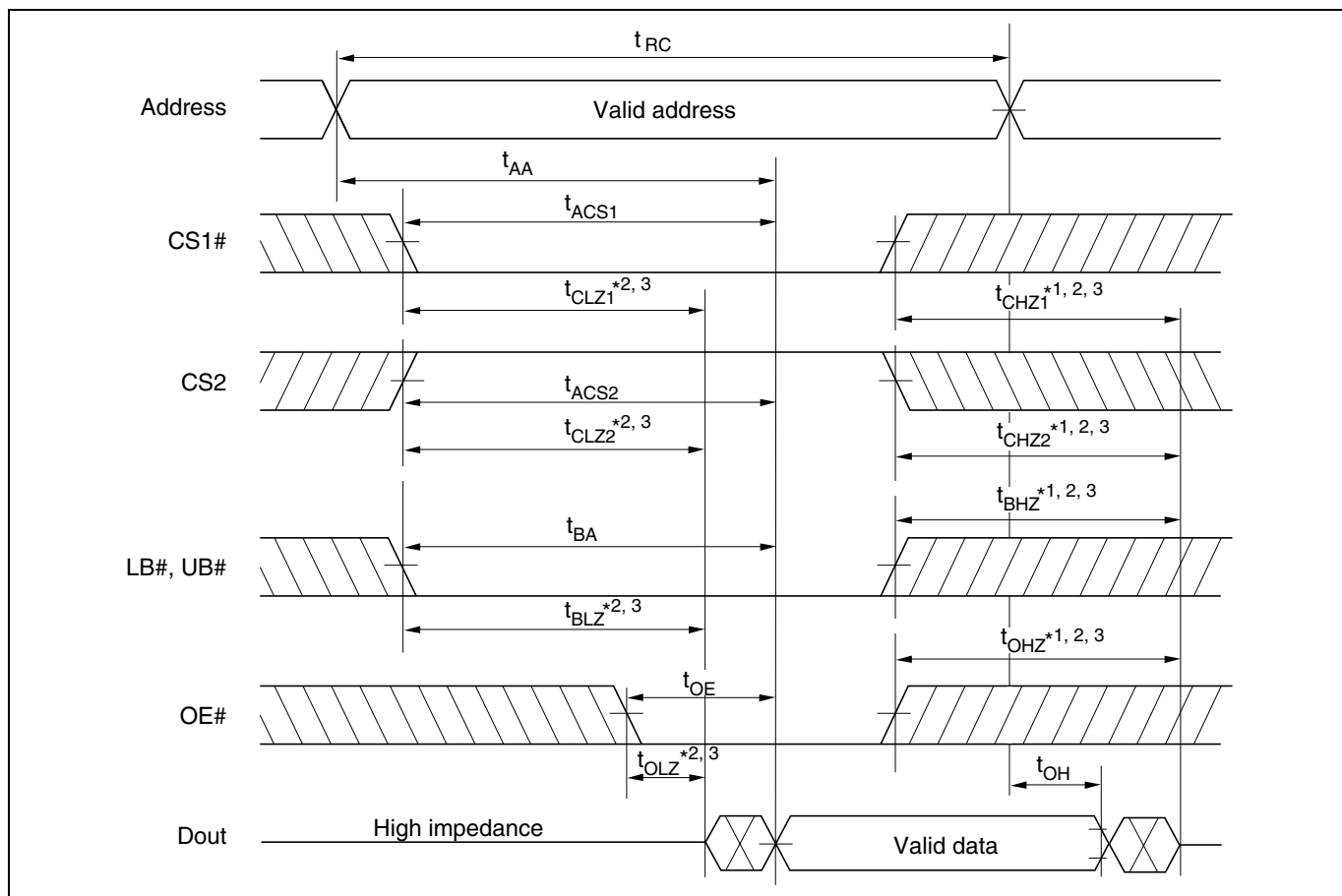
Parameter	Symbol	R1LV0416D				Unit	Notes
		-5SI		-7LI			
		Min	Max	Min	Max		
Read cycle time	t _{RC}	55	—	70	—	ns	
Address access time	t _{AA}	—	55	—	70	ns	
Chip select access time	t _{ACS1}	—	55	—	70	ns	
	t _{ACS2}	—	55	—	70	ns	
Output enable to output valid	t _{OE}	—	35	—	40	ns	
Output hold from address change	t _{OH}	10	—	10	—	ns	
LB#, UB# access time	t _{BA}	—	55	—	70	ns	
Chip select to output in low-Z	t _{CLZ1}	10	—	10	—	ns	2, 3
	t _{CLZ2}	10	—	10	—	ns	2, 3
LB#, UB# disable to low-Z	t _{BLZ}	5	—	5	—	ns	2, 3
Output enable to output in low-Z	t _{OLZ}	5	—	5	—	ns	2, 3
Chip deselect to output in high-Z	t _{CHZ1}	0	20	0	25	ns	1, 2, 3
	t _{CHZ2}	0	20	0	25	ns	1, 2, 3
LB#, UB# disable to high-Z	t _{BHZ}	0	20	0	25	ns	1, 2, 3
Output disable to output in high-Z	t _{OHZ}	0	20	0	25	ns	1, 2, 3

Write Cycle

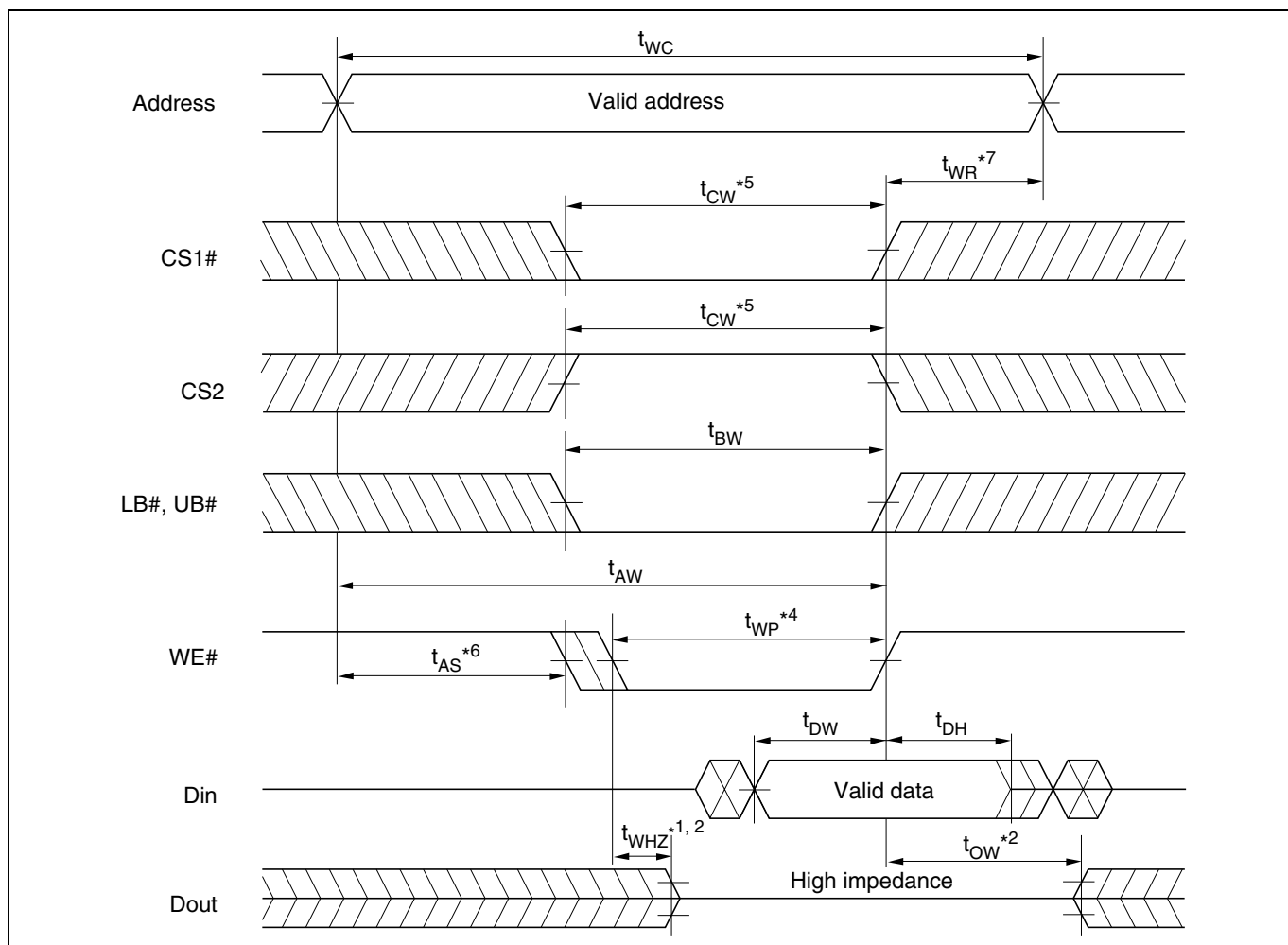
Parameter	Symbol	R1LV0416D				Unit	Notes
		-5SI		-7LI			
		Min	Max	Min	Max		
Write cycle time	t _{WC}	55	—	70	—	ns	
Address valid to end of write	t _{AW}	50	—	60	—	ns	
Chip selection to end of write	t _{CW}	50	—	60	—	ns	5
Write pulse width	t _{WP}	40	—	50	—	ns	4
LB#, UB# valid to end of write	t _{BW}	50	—	55	—	ns	
Address setup time	t _{AS}	0	—	0	—	ns	6
Write recovery time	t _{WR}	0	—	0	—	ns	7
Data to write time overlap	t _{DW}	25	—	30	—	ns	
Data hold from write time	t _{DH}	0	—	0	—	ns	
Output active from end of write	t _{OW}	5	—	5	—	ns	2
Output disable to output in high-Z	t _{OHZ}	0	20	0	25	ns	1, 2, 3
Write to output in high-Z	t _{WHZ}	0	20	0	25	ns	1, 2

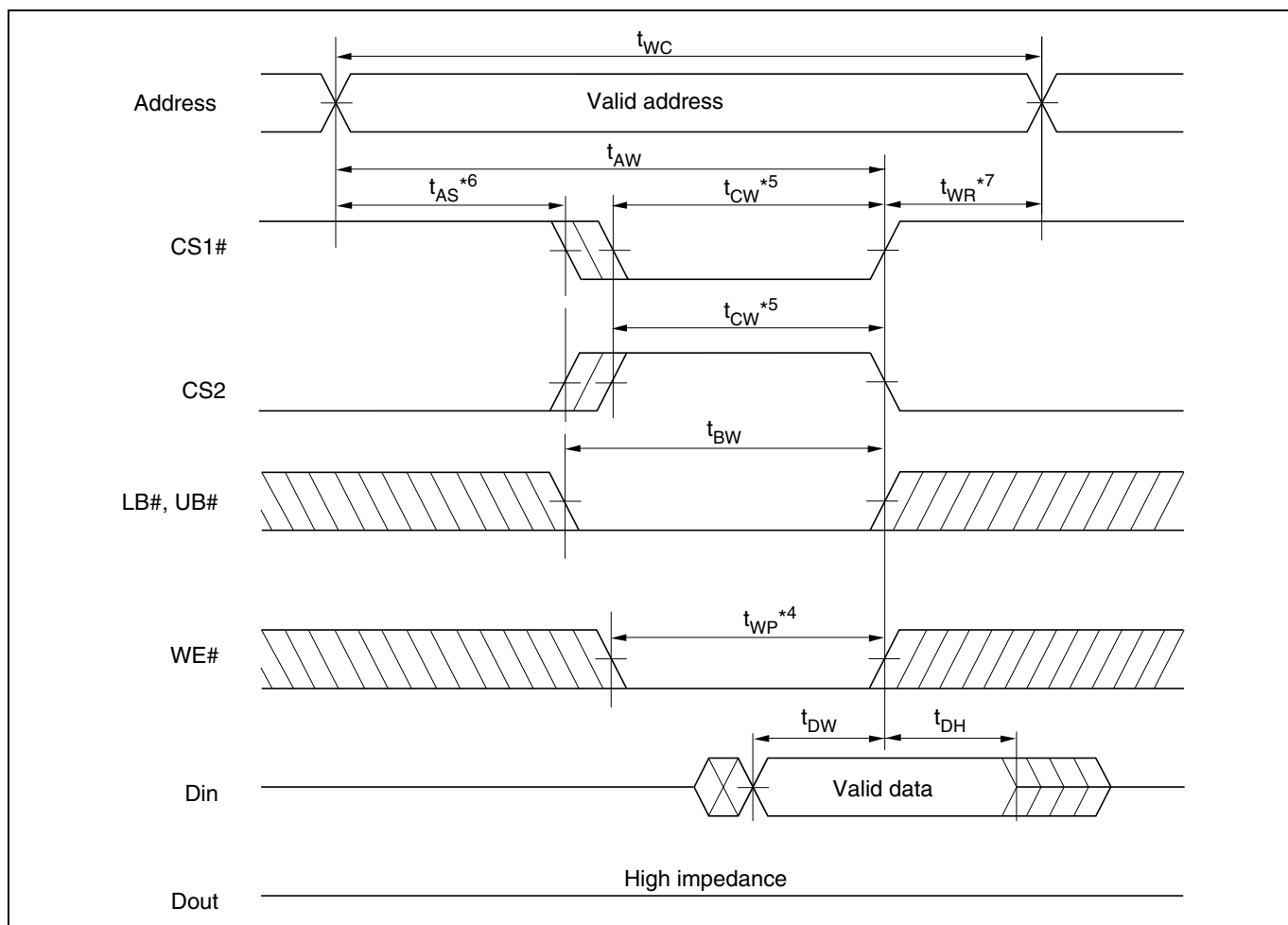
- Notes: 1. t_{CHZ} , t_{OHZ} , t_{WHZ} and t_{BHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
4. A write occurs during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#. A write begins at the latest transition among CS1# going low, CS2 going high, WE# going low and LB# going low or UB# going low. A write ends at the earliest transition among CS1# going high, CS2 going low, WE# going high and LB# going high or UB# going high. t_{WP} is measured from the beginning of write to the end of write.
5. t_{CW} is measured from the later of CS1# going low or CS2 going high to the end of write.
6. t_{AS} is measured from the address valid to the beginning of write.
7. t_{WR} is measured from the earliest of CS1# or WE# going high or CS2 going low to the end of write cycle.

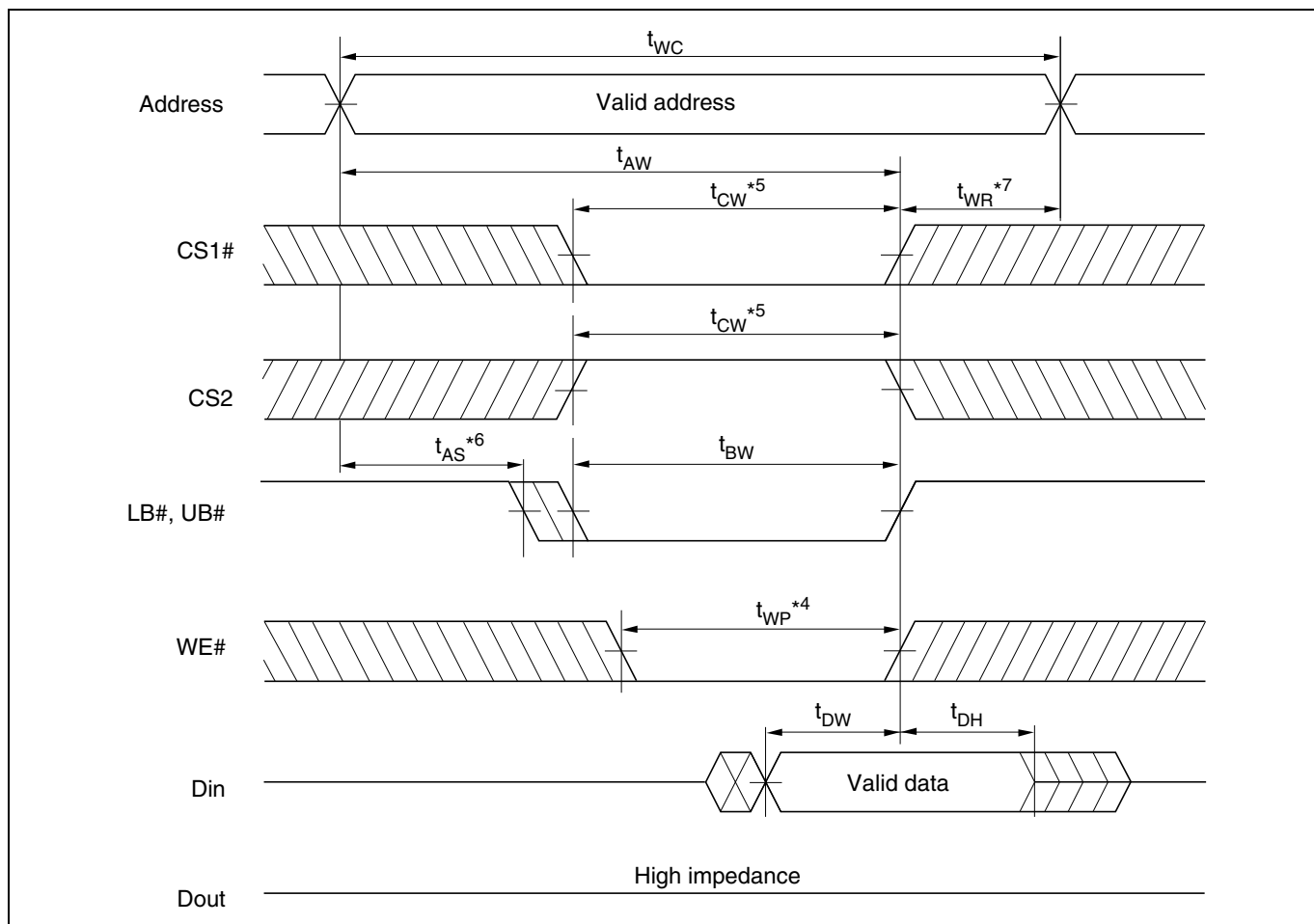
Timing Waveform

Read Timing Waveform ($WE\# = V_{IH}$)

Write Timing Waveform (1) (WE# Clock)



Write Timing Waveform (2) (CS# Clock, OE# = V_{IH})

Write Timing Waveform (3) (LB#, UB# Clock, OE# = V_{IH})

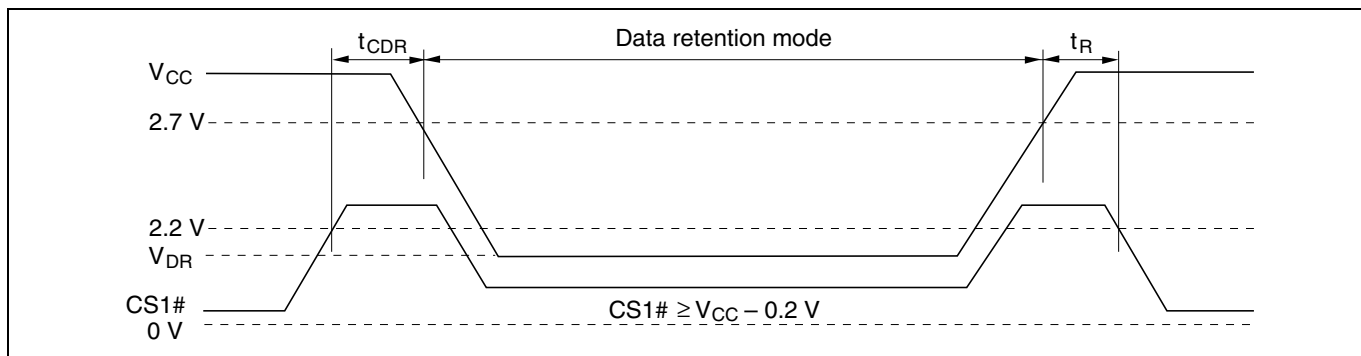
Low V_{CC} Data Retention Characteristics

(Ta = -40 to +85°C)

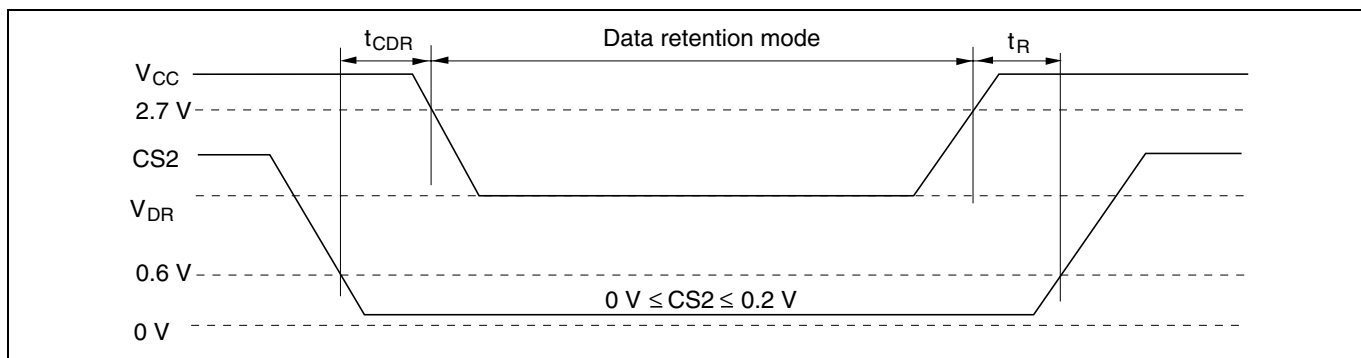
Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
V _{cc} for data retention			V _{DR}	2.0	—	—	V	V _{in} ≥ 0V (1) 0 V ≤ CS2 ≤ 0.2 V or (2) CS2 ≥ V _{cc} − 0.2 V, CS1# ≥ V _{cc} − 0.2 V or (3) LB# = UB# ≥ V _{cc} − 0.2 V, CS2 ≥ V _{cc} − 0.2 V, CS1# ≤ 0.2 V
Data retention current	−5SI	to +85°C	I _{CCDR}	—	—	10	μA	V _{cc} = 3.0 V, V _{in} ≥ 0V (1) 0 V ≤ CS2 ≤ 0.2 V or (2) CS2 ≥ V _{cc} − 0.2 V, CS1# ≥ V _{cc} − 0.2 V or (3) LB# = UB# ≥ V _{cc} − 0.2 V, CS2 ≥ V _{cc} − 0.2 V, CS1# ≤ 0.2 V Average values
		to +70°C	I _{CCDR}	—	—	8	μA	
		to +40°C	I _{CCDR}	—	—	3	μA	
		to +25°C	I _{CCDR}	—	1* ¹	2.5	μA	
	−7LI	to +85°C	I _{CCDR}	—	—	20	μA	
		to +70°C	I _{CCDR}	—	—	16	μA	
		to +40°C	I _{CCDR}	—	—	10	μA	
		to +25°C	I _{CCDR}	—	1* ¹	10	μA	
Chip deselect to data retention time			t _{CDR}	0	—	—	ns	See retention waveform
Operation recovery time			t _r	5	—	—	ms	

Note: 1. Typical values are at $V_{CC} = 3.0V$, $T_a = +25^\circ C$ and specified loading, and not guaranteed.

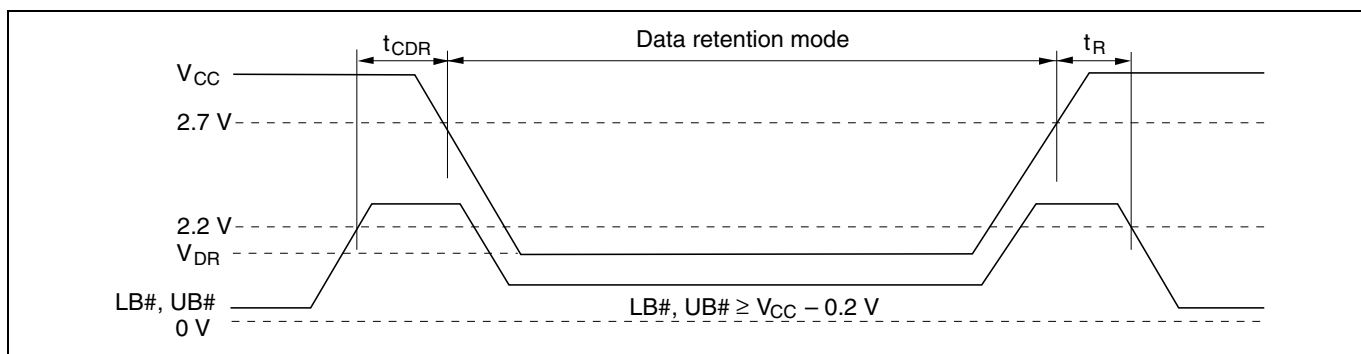
Low V_{CC} Data Retention Timing Waveform (1) (CS1# Controlled)



Low V_{CC} Data Retention Timing Waveform (2) (CS2 Controlled)



Low V_{CC} Data Retention Timing Waveform (3) (LB#, UB# Controlled)



Revision History	R1LV0416D Series Data Sheet
------------------	-----------------------------

Rev.	Date	Contents of Modification	
		Page	Description
0.01	Dec. 25, 2006	—	Initial issue
1.00	May. 24, 2007	2	Ordering Information R1LV0416DSB-5S% to R1LV0416DSB-5SI R1LV0416DSB-7L% to R1LV0416DSB-7LI R1LV0416DBG-5S% to R1LV0416DBG-5SI R1LV0416DBG-7L% to R1LV0416DBG-7LI
		3	Pin Arrangement A6 to A13, A13 to A6
		4	Change of Block Diagram
		5	Absolute Maximum Ratings: Deletion of R ver. specification
		5	DC Operating Conditions: Deletion of R ver. specification
		6	DC Characteristics I_{SB1} (-5SI) (to +25°C) max: 3 μ A to 2.5 μ A
		7	AC Characteristics: Change of Test Conditions
		14	Low V_{CC} Data Retention Characteristics I_{CCDR} (-5SI) (to +25°C) max: 3 μ A to 2.5 μ A Deletion of note 2

Notes:

1. This document is provided for reference purposes only so that Renesas customers may select the appropriate Renesas products for their use. Renesas neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of Renesas or any third party with respect to the information in this document.
2. Renesas shall have no liability for damages or infringement of any intellectual property or other rights arising out of the use of any information in this document, including, but not limited to, product data, diagrams, charts, programs, algorithms, and application circuit examples.
3. You should not use the products or the technology described in this document for the purpose of military applications such as the development of weapons of mass destruction or for the purpose of any other military use. When exporting the products or technology described herein, you should follow the applicable export control laws and regulations, and procedures required by such laws and regulations.
4. All information included in this document such as product data, diagrams, charts, programs, algorithms, and application circuit examples, is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas products listed in this document, please confirm the latest product information with a Renesas sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas such as that disclosed through our website. (<http://www.renesas.com>)
5. Renesas has used reasonable care in compiling the information included in this document, but Renesas assumes no liability whatsoever for any damages incurred as a result of errors or omissions in the information included in this document.
6. When using or otherwise relying on the information in this document, you should evaluate the information in light of the total system before deciding about the applicability of such information to the intended application. Renesas makes no representations, warranties or guarantees regarding the suitability of its products for any particular application and specifically disclaims any liability arising out of the application and use of the information in this document or Renesas products.
7. With the exception of products specified by Renesas as suitable for automobile applications, Renesas products are not designed, manufactured or tested for applications or otherwise in systems the failure or malfunction of which may cause a direct threat to human life or create a risk of human injury or which require especially high quality and reliability such as safety systems, or equipment or systems for transportation and traffic, healthcare, combustion control, aerospace and aeronautics, nuclear power, or undersea communication transmission. If you are considering the use of our products for such purposes, please contact a Renesas sales office beforehand. Renesas shall have no liability for damages arising out of the uses set forth above.
8. Notwithstanding the preceding paragraph, you should not use Renesas products for the purposes listed below:
 - (1) artificial life support devices or systems
 - (2) surgical implantations
 - (3) healthcare intervention (e.g., excision, administration of medication, etc.)
 - (4) any other purposes that pose a direct threat to human lifeRenesas shall have no liability for damages arising out of the uses set forth in the above and purchasers who elect to use Renesas products in any of the foregoing applications shall indemnify and hold harmless Renesas Technology Corp., its affiliated companies and their officers, directors, and employees against any and all damages arising out of such applications.
9. You should use the products described herein within the range specified by Renesas, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas shall have no liability for malfunctions or damages arising out of the use of Renesas products beyond such specified ranges.
10. Although Renesas endeavors to improve the quality and reliability of its products, IC products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Please be sure to implement safety measures to guard against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other applicable measures. Among others, since the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
11. In case Renesas products listed in this document are detached from the products to which the Renesas products are attached or affixed, the risk of accident such as swallowing by infants and small children is very high. You should implement safety measures so that Renesas products may not be easily detached from your products. Renesas shall have no liability for damages arising out of such detachment.
12. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written approval from Renesas.
13. Please contact a Renesas sales office if you have any questions regarding the information contained in this document, Renesas semiconductor products, or if you have any other inquiries.



RENESAS SALES OFFICES

<http://www.renesas.com>

Refer to "<http://www.renesas.com/en/network>" for the latest and detailed information.

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510