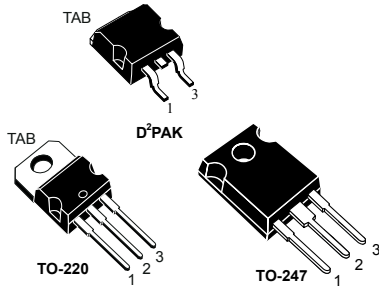




N-channel 600 V, 110 mΩ typ., 24 A MDmesh DM2 Power MOSFET in D²PAK, TO-220 and TO-247 packages



AM01476v1_tab



Features

Order code	$V_{DS} @ T_{Jmax.}$	$R_{DS(on)}$ max.	I_D
STB33N60DM2	650 V	130 mΩ	24 A
STP33N60DM2			
STW33N60DM2			

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

These high voltage N-channel Power MOSFETs are part of the MDmesh DM2 fast recovery diode series. They offer very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low $R_{DS(on)}$, rendering them suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Product status link

[STB33N60DM2](#)

[STP33N60DM2](#)

[STW33N60DM2](#)

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage (static)	± 25	V
	Gate-source voltage (dynamic AC, $f > 1$ Hz)	± 30	
I_D	Drain current (continuous) at $T_C = 25$ °C	24	A
	Drain current (continuous) at $T_C = 100$ °C	15.5	
$I_{DM}^{(1)}$	Drain current (pulsed)	96	A
P_{TOT}	Total power dissipation at $T_C = 25$ °C	190	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	100	V/ns
$di/dt^{(2)}$	Peak diode recovery current slope	1000	A/ μ s
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	100	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		

1. Pulse width is limited by safe operating area.
2. $I_{SD} \leq 24$ A, V_{DS} peak $< V_{(BR)DSS}$, $V_{DD} = 400$ V.
3. $V_{DS} \leq 480$ V.

Table 2. Thermal data

Symbol	Parameter	Value			Unit
		D ² PAK	TO-220	TO-247	
R_{thJC}	Thermal resistance, junction-to-case	0.66			°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	30 ⁽¹⁾	62.5	50	

1. When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (Pulse width limited by T_{Jmax})	5.5	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25$ °C, $I_D = I_{AR}$, $V_{DD} = 50$ V)	570	mJ

2 Electrical characteristics

($T_{case} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}$ ⁽¹⁾			100	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 12\text{ A}$		110	130	m Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	1870	-	pF
C_{oss}	Output capacitance		-	87	-	
C_{rss}	Reverse transfer capacitance		-	2	-	
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DD} = 480\text{ V}$, $V_{GS} = 0\text{ V}$	-	157	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	4.5	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 24\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 18. Test circuit for gate charge behavior)	-	43	-	nC
Q_{gs}	Gate-source charge		-	9.8	-	
Q_{gd}	Gate-drain charge		-	21	-	

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 12\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 17. Test circuit for resistive load switching times and Figure 22. Switching time waveform)	-	17	-	ns
t_r	Rise time		-	8	-	
$t_{d(off)}$	Turn-off delay time		-	62	-	
t_f	Fall time		-	9	-	

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		24	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		96	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 24\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 24\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 19. Test circuit for inductive load switching and diode recovery times)	-	150		ns
Q_{rr}	Reverse recovery charge		-	0.5		μC
I_{RRM}	Reverse recovery current		-	8.8		A
t_{rr}	Reverse recovery time	$I_{SD} = 24\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 19. Test circuit for inductive load switching and diode recovery times)	-	316		ns
Q_{rr}	Reverse recovery charge		-	2.85		μC
I_{RRM}	Reverse recovery current		-	18		A

1. Pulse width is limited by safe operating area.

2. Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics curves

Figure 1. Safe operating area for D²PAK

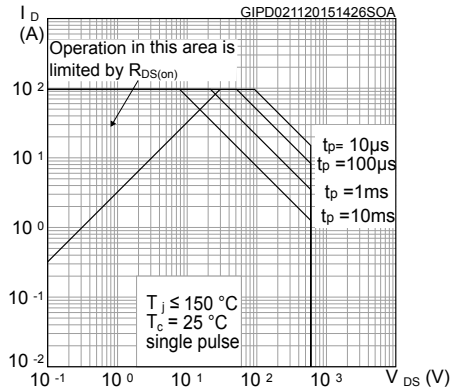


Figure 2. Thermal impedance for D²PAK

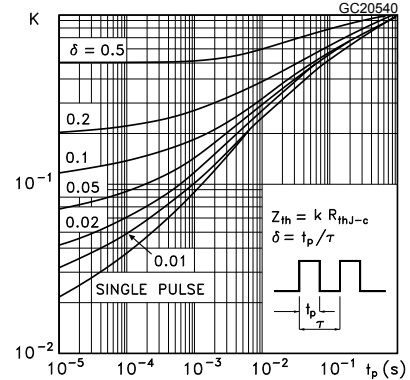


Figure 3. Safe operating area for TO-220

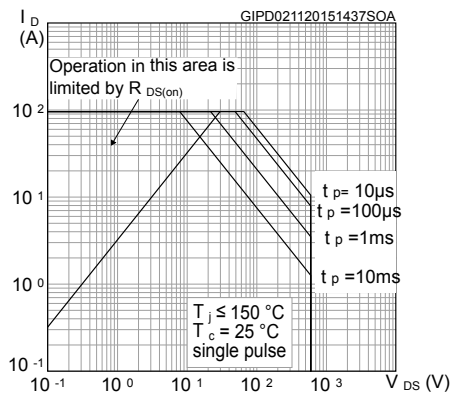


Figure 4. Thermal impedance for TO-220

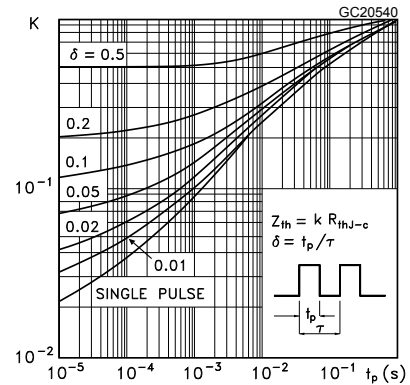


Figure 5. Safe operating area for TO-247

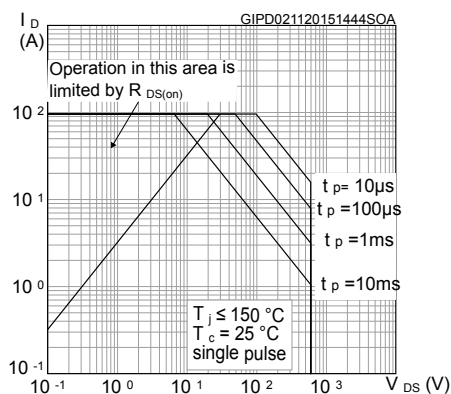


Figure 6. Thermal impedance for TO-247

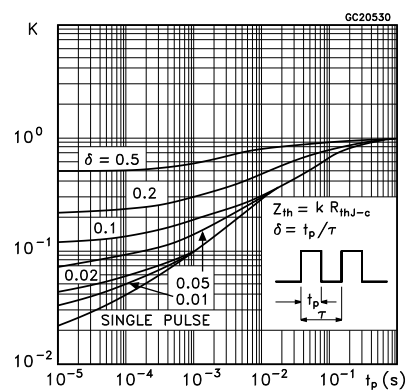


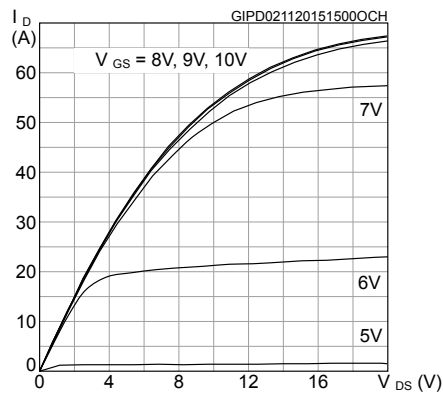
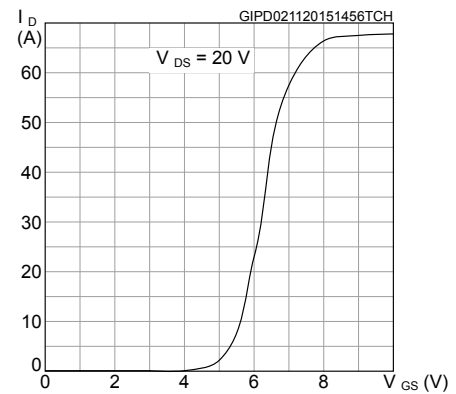
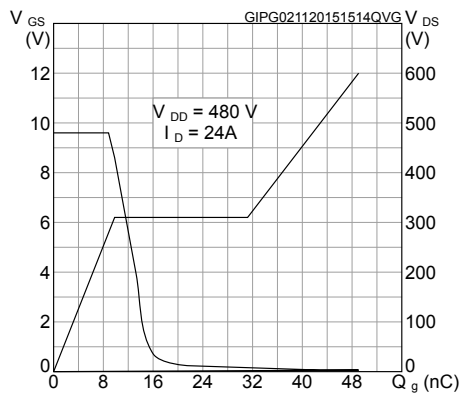
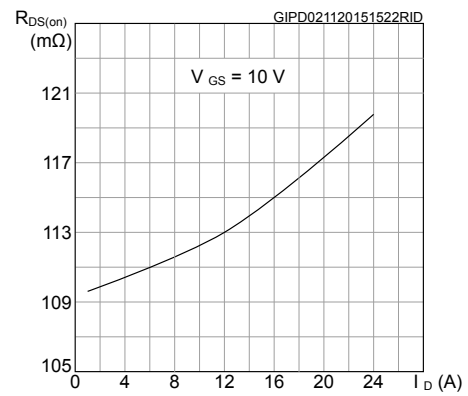
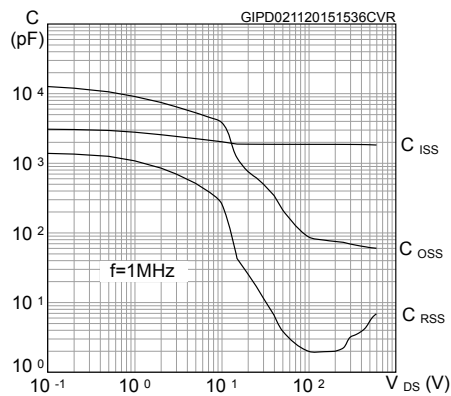
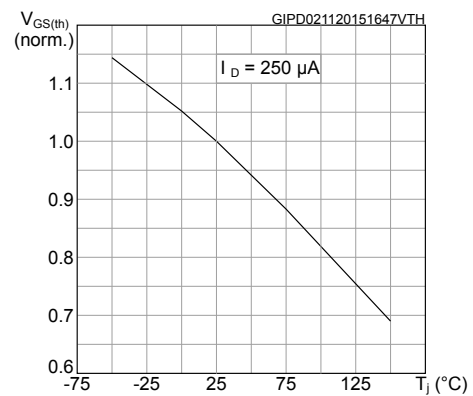
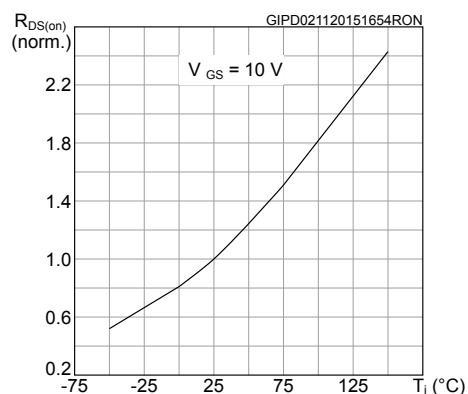
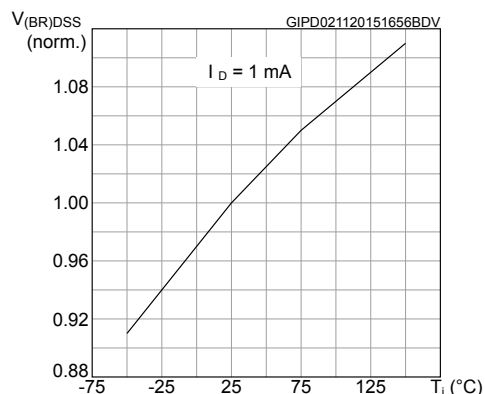
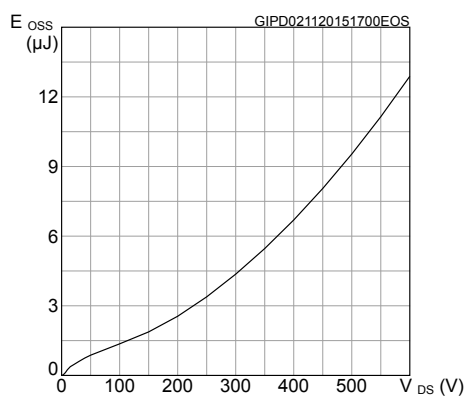
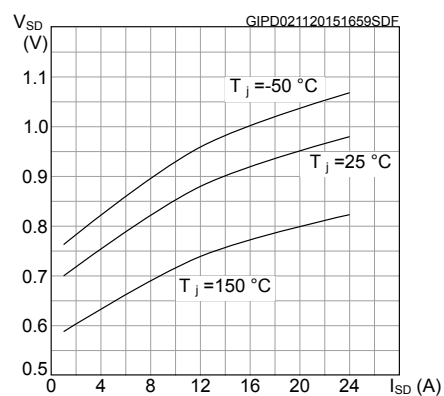
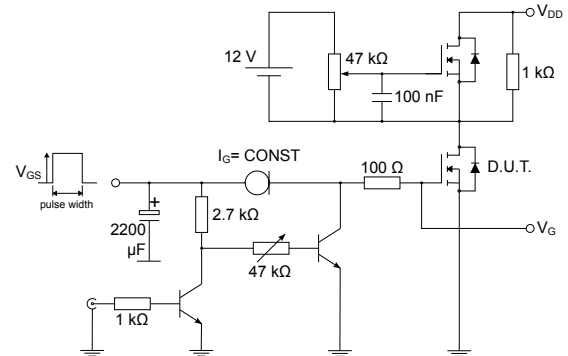
Figure 7. Output characteristics

Figure 8. Transfer characteristics

Figure 9. Gate charge vs gate-source voltage

Figure 10. Static drain-source on-resistance

Figure 11. Capacitance variations

Figure 12. Normalized gate threshold voltage vs temperature


Figure 13. Normalized on-resistance vs temperature

Figure 14. Normalized $V_{(BR)DSS}$ vs temperature

Figure 15. Output capacitance stored energy

Figure 16. Source-drain diode forward characteristics


3 Test circuits

Figure 17. Test circuit for resistive load switching times

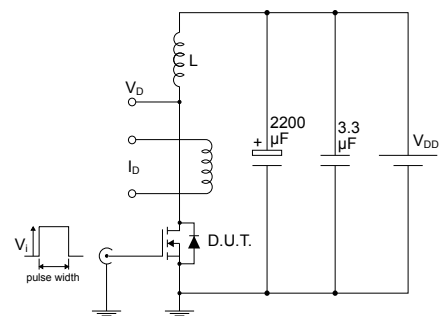

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Figure 18. Test circuit for gate charge behavior


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Figure 19. Test circuit for inductive load switching and diode recovery times

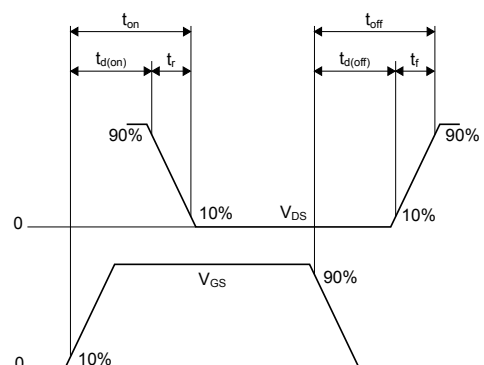

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Figure 20. Unclamped inductive load test circuit


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Figure 21. Unclamped inductive waveform


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Figure 22. Switching time waveform


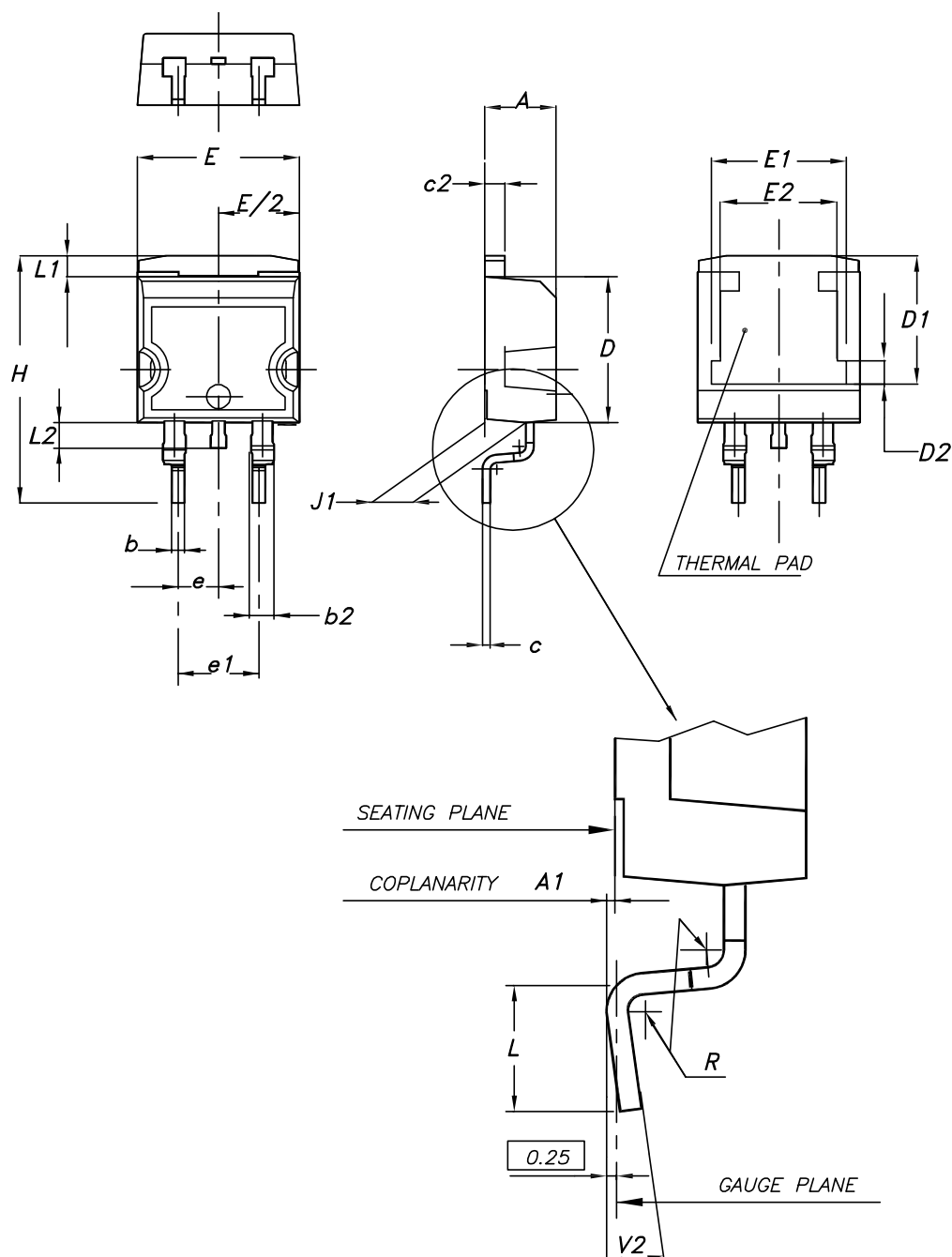
AM01473v1

4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A package information

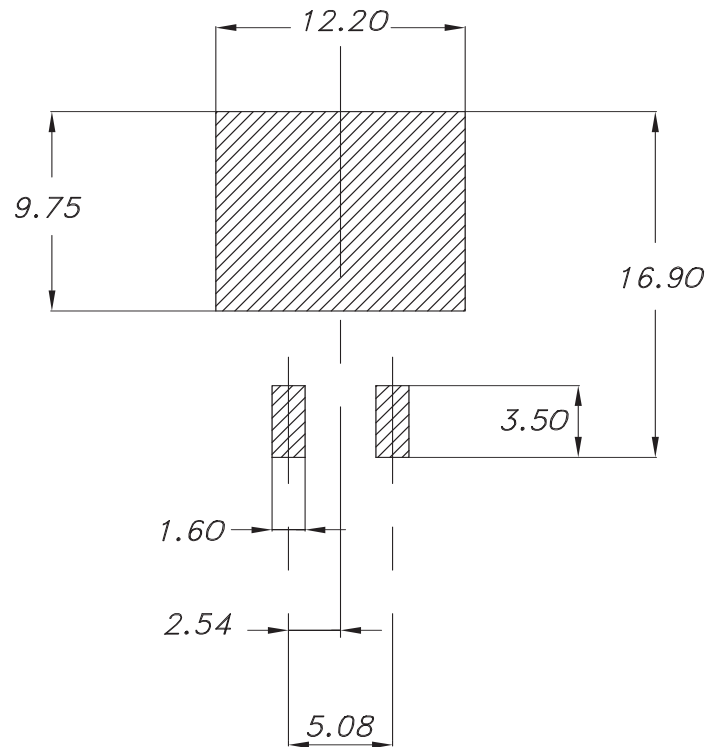
Figure 23. D²PAK (TO-263) type A package outline



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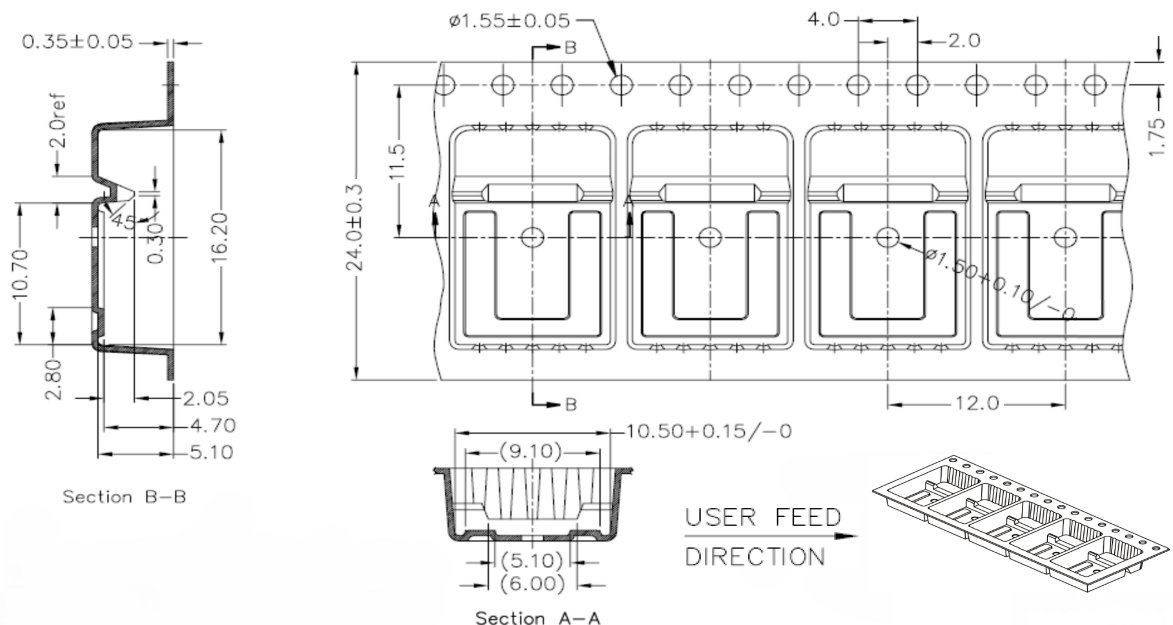
Table 8. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

Figure 24. D²PAK (TO-263) recommended footprint (dimensions are in mm)


0079457_Rev27_footprint

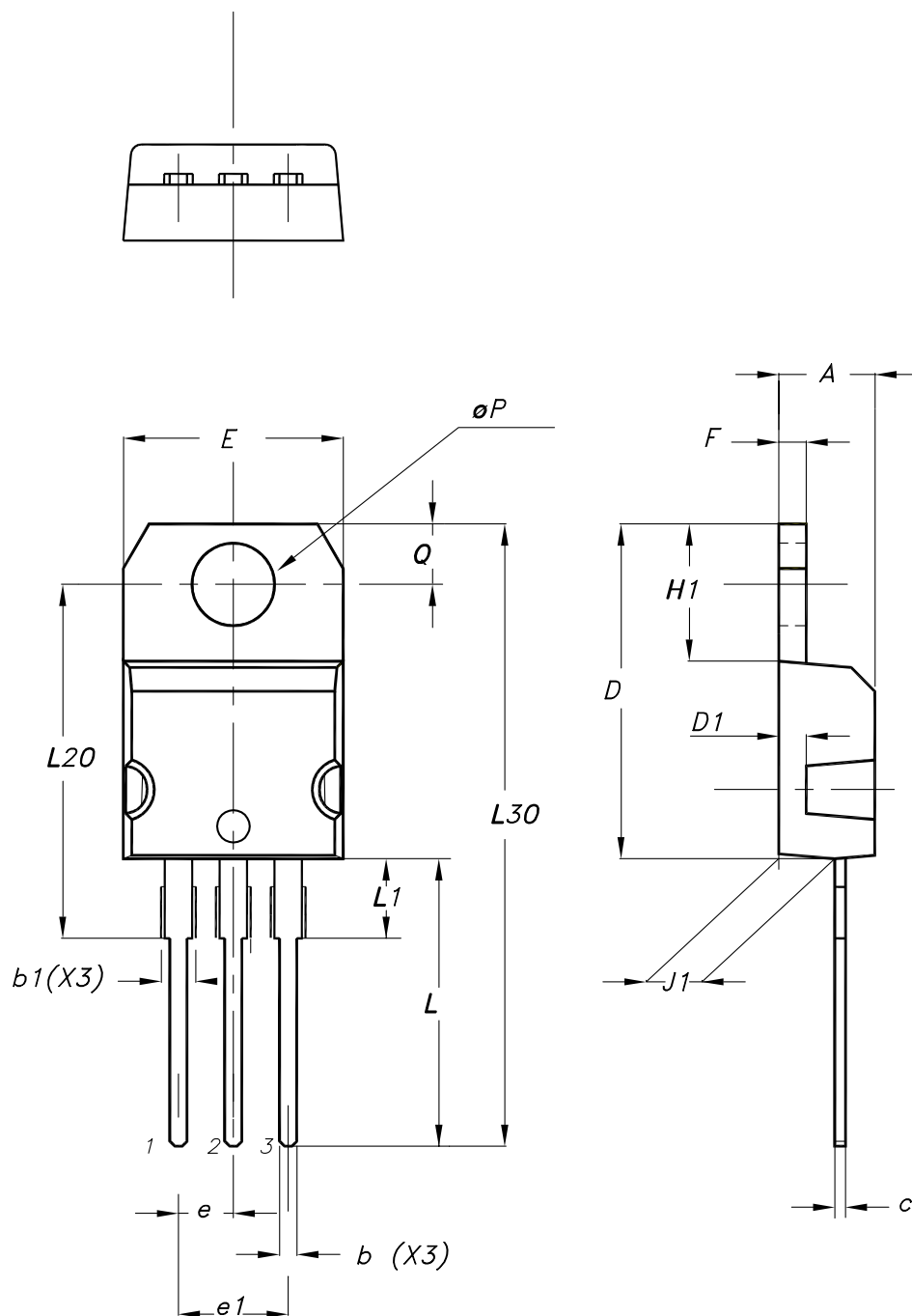
4.2 D²PAK packing information

Figure 25. D²PAK tape drawing (dimensions are in mm)


DM01095771_2

4.3 TO-220 type A package information

Figure 26. TO-220 type A package outline



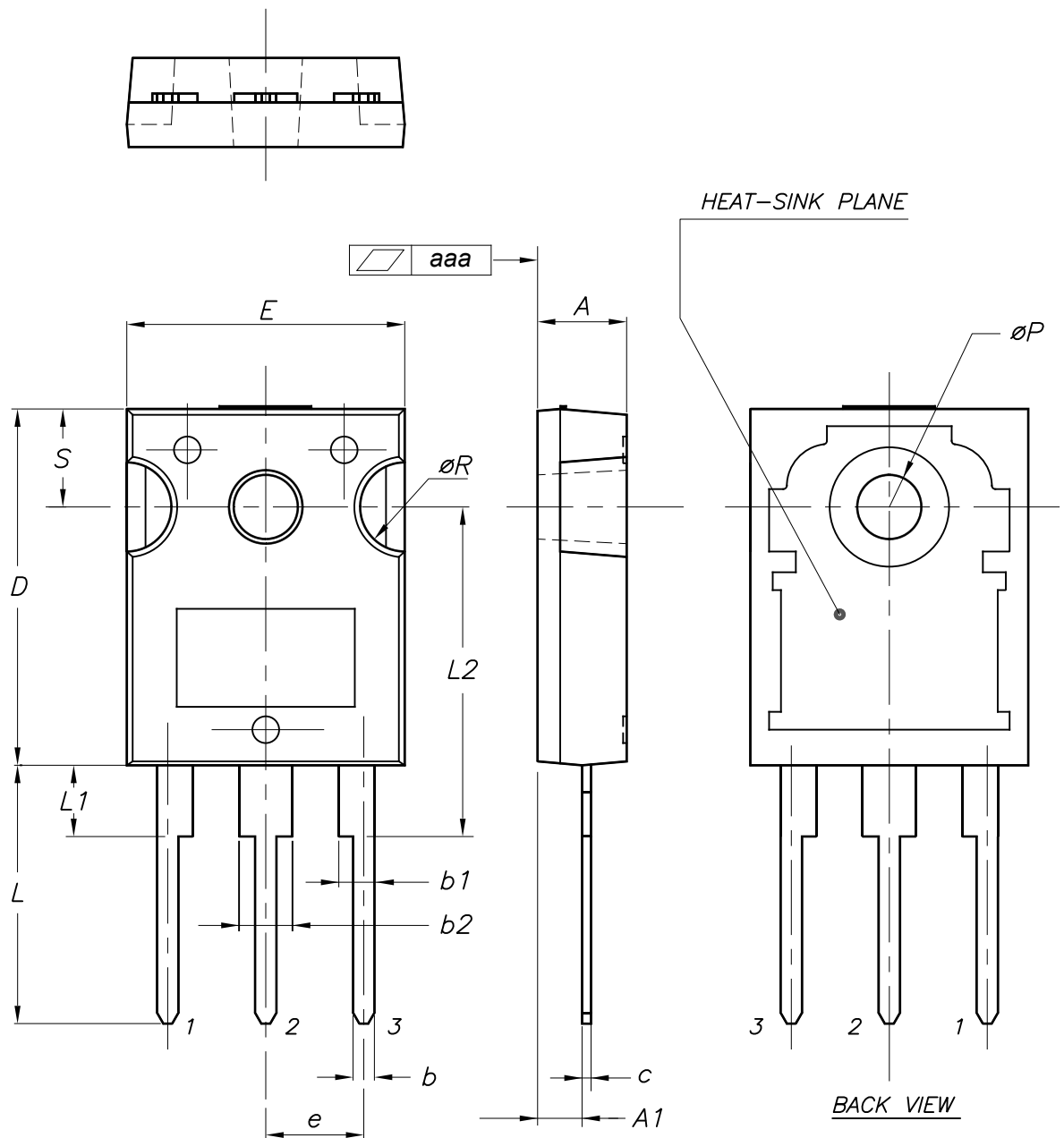
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Table 9. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

4.4 TO-247 package information

Figure 27. TO-247 package outline



0075325_10

Table 10. TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70
aaa		0.04	0.10

5 Ordering information

Table 11. Order codes

Order code	Marking	Package	Packing
STB33N60DM2	33N60DM2	D ² PAK	Tape e reel
STP33N60DM2		TO-220	Tube
STW33N60DM2		TO-247	Tube

Revision history

Table 12. Document revision history

Date	Revision	Changes
16-Oct-2014	1	First release.
02-Nov-2015	2	Document status promoted from preliminary to production data. Updated title and features in cover page. Updated <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 4: "Avalanche characteristics"</i> , <i>Table 5: "Static"</i> , <i>Table 6: "Dynamic"</i> , <i>Table 7: "Switching times"</i> and <i>Table 8: "Source-drain diode"</i> . Added <i>Section 2.1 Electrical characteristics (curves)</i> .
19-Oct-2020	3	Updated <i>Section 1 Electrical ratings</i> . Minor text changes.
01-Aug-2025	4	Updated Section 4: Package information . Minor text changes.

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