



High Performance Communication Buffer

General Description

The **ICS91305I** is a high performance, low skew, low jitter clock driver. It uses a phase lock loop (PLL) technology to align, in both phase and frequency, the REF input with the CLKOUT signal. It is designed to distribute high speed clocks in communication systems operating at speeds from 10 to 133 MHz.

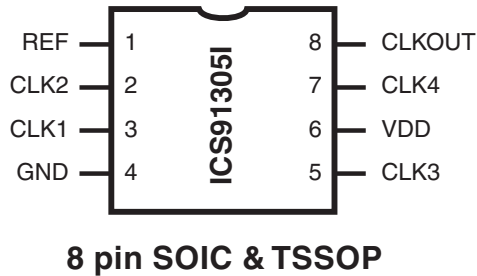
ICS91305I is a zero delay buffer that provides synchronization between the input and output. The synchronization is established via CLKOUT feed back to the input of the PLL. Since the skew between the input and output is less than +/- 350 pS, the part acts as a zero delay buffer.

The **ICS91305I** comes in an eight pin 150 mil SOIC package. It has five output clocks. In the absence of REF input, will be in the power down mode. In this mode, the PLL is turned off and the output buffers are pulled low. Power down mode provides the lowest power consumption for a standby condition.

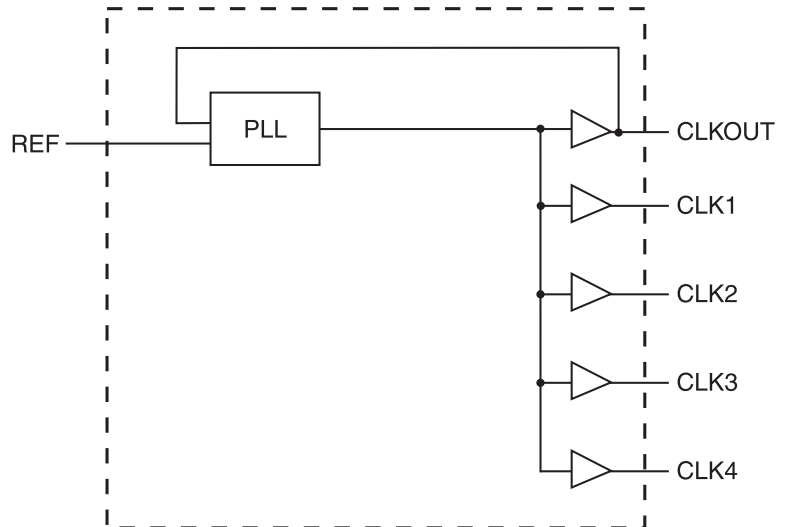
Features

- Zero input - output delay
- Frequency range 10 - 133 MHz (3.3V)
- 5V tolerant input REF
- High loop filter bandwidth ideal for Spread Spectrum applications.
- Less than 200 ps Jitter between outputs
- Skew controlled outputs
- Skew less than 250 ps between outputs
- Available in 8 pin 150 mil SOIC & 173 mil TSSOP packages
- 3.3V \pm 10% operation
- Supports industrial temperature range -40°C to 85°C

Pin Configuration



Block Diagram





Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	REF ²	IN	Input reference frequency, 5V tolerant input.
2	CLK2 ³	OUT	Buffered clock output
3	CLK1 ³	OUT	Buffered clock output
4	GND	PWR	Ground
5	CLK3 ³	OUT	Buffered clock output
6	VDD	PWR	Power Supply (3.3V)
7	CLK4 ³	OUT	Buffered clock output
8	CLKOUT ³	OUT	Buffered clock output. Internal feedback on this pin

Notes:

1. Guaranteed by design and characterization. Not subject to 100% test.
2. Weak pull-down
3. Weak pull-down on all outputs



Absolute Maximum Ratings

Supply Voltage	7.0 V
Logic Inputs (Except REF)	GND -0.5 V to $V_{DD} + 0.5$ V
Logic Input REF	GND -0.5 V to GND + 5.5 V
Ambient Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 3.3V

$V_{DD} = 3.0 - 3.6$ V, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}				0.8	V
Input High Voltage	V_{IH}		2.0			V
Input Low Current	I_{IL}	$V_{IN}=0\text{V}$		19	100.0	μA
Input High Current	I_{IH}	$V_{IN}=V_{DD}$		0.10	250.0	μA
Output Low Voltage ¹	V_{OL}	$I_{OL} = 12\text{mA}$		0.25	0.4	V
Output High Voltage ¹	V_{OH}	$I_{OH} = -12\text{mA}$	2.4	2.9		V
Power Down Supply Current	I_{DD}	REF = 0 MHz		0.3	100.0	μA
Supply Current	I_{DD}	Unloaded outputs at 66.66 MHz SEL inputs at V_{DD} or GND		30.0	80.0	mA

Notes:

1. Guaranteed by design and characterization. Not subject to 100% test.
2. All Skew specifications are measured with a 50 Ω transmission line, load terminated with 50 Ω to 1.4V.
3. Duty cycle measured at 1.4V.
4. Skew measured at 1.4V on rising edges. Loading must be equal on outputs.



Switching Characteristics

Notes:

1. Guaranteed by design and characterization. Not subject to 100% test.
2. REF input has a threshold voltage of 1.4V
3. All parameters expected with loaded outputs



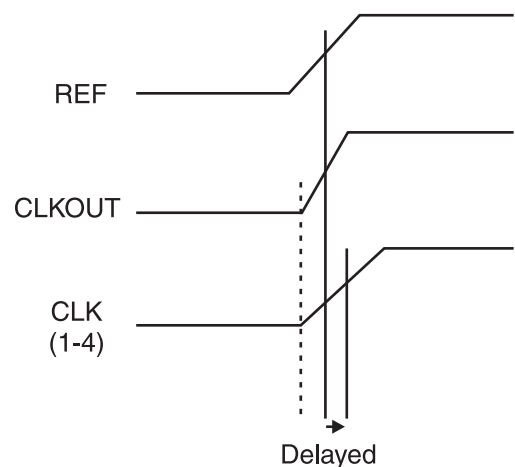
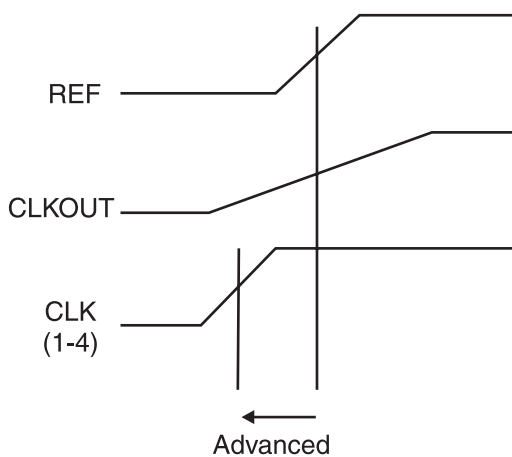
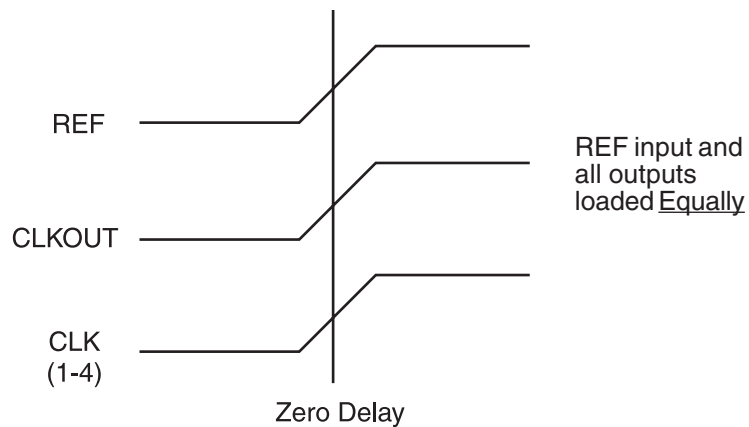
Output to Output Skew

The skew between CLKOUT and the CLK(1-4) outputs is not dynamically adjusted by the PLL. Since CLKOUT is one of the inputs to the PLL, zero phase difference is maintained from REF to CLKOUT. If all outputs are equally loaded, zero phase difference will be maintained from REF to all outputs.

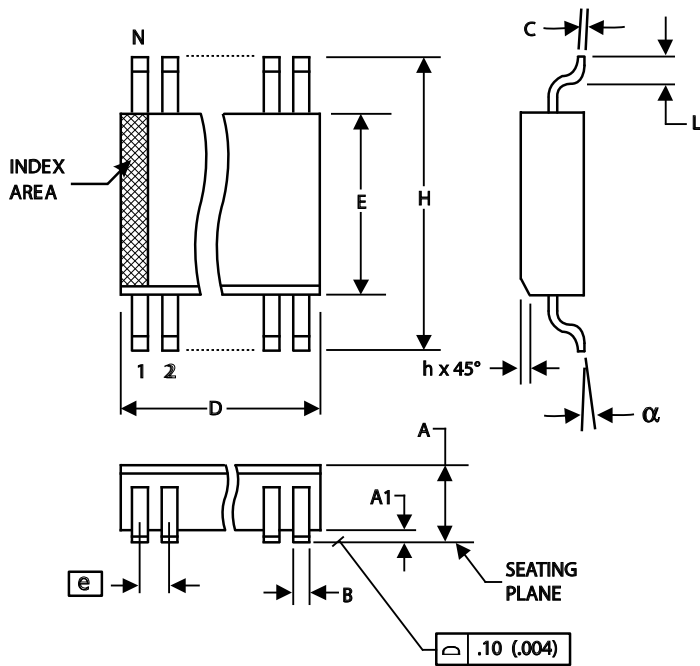
If applications requiring zero output-to-output skew, all the outputs must be equally loaded.

If the CLK(1-4) outputs are less loaded than CLKOUT, CLK(1-4) outputs will lead it; and if the CLK(1-4) is more loaded than CLKOUT, CLK(1-4) will lag the CLKOUT.

Since the CLKOUT and the CLK(1-4) outputs are identical, they all start at the same time, but different loads cause them to have different rise times and different times crossing the measurement thresholds.



Timing diagrams with different loading configurations



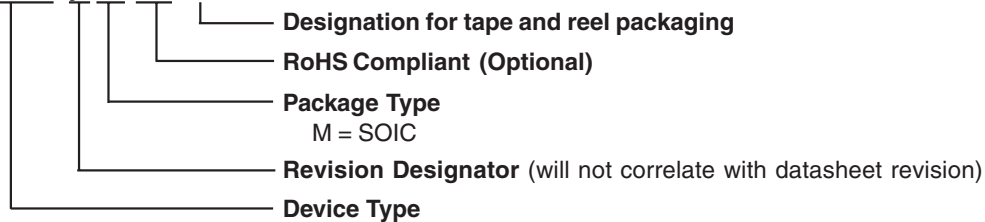
150 mil (Narrow Body) SOIC

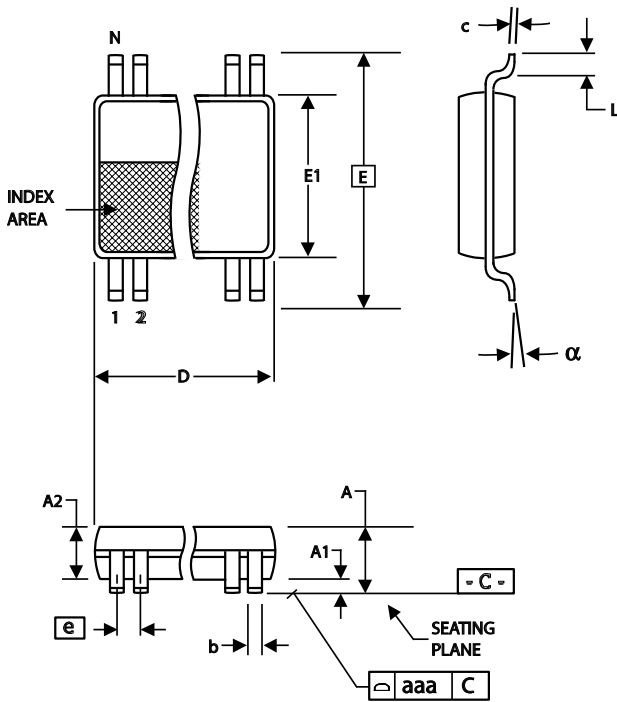
Ordering Information

91305yMILF-T

Example:

XXXX y M LF-T





4.40 mm. Body, 0.65 mm. Pitch TSSOP
(173 mil) (25.6 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.19	0.30	.007	.012
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.65 BASIC		0.0256 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
8	2.90	3.10	.114	.122

Reference Doc.: JEDEC Publication 95, MO-153

10-0035

Ordering Information

91305yGILF-T

Example:

XXXX y G LF-T

- XXXX — Device Type
- y — Revision Designator (will not correlate with datasheet revision)
- G — Package Type
G = TSSOP
- LF — RoHS Compliant (Optional)
- T — Designation for tape and reel packaging



Revision History

Rev.	Issue Date	Description	Page #
F	6/3/2005	1. Resized Electrical Characteristics Table. 2. Updated LF Ordering Information from "Lead Free" to "RoHS Compliant".	3,6,7