

128K x 16 HIGH-SPEED CMOS STATIC RAM WITH 3.3V SUPPLY

PRELIMINARY INFORMATION
JULY 2002

FEATURES

- High-speed access time:
 - IS61LV12816L: 8, 10 ns
 - IS61LV12816LL: 12, 15 ns
- Operating Current:
 - IS61LV12816L: 50mA (typ.)
 - IS61LV12816LL: 25mA (typ.)
- Stand by Current:
 - IS61LV12816L: 500µA (typ.)
 - IS61LV12816LL: 250µA (typ.)
- TTL and CMOS compatible interface levels
- Single 3.3V power supply
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Industrial temperature available

DESCRIPTION

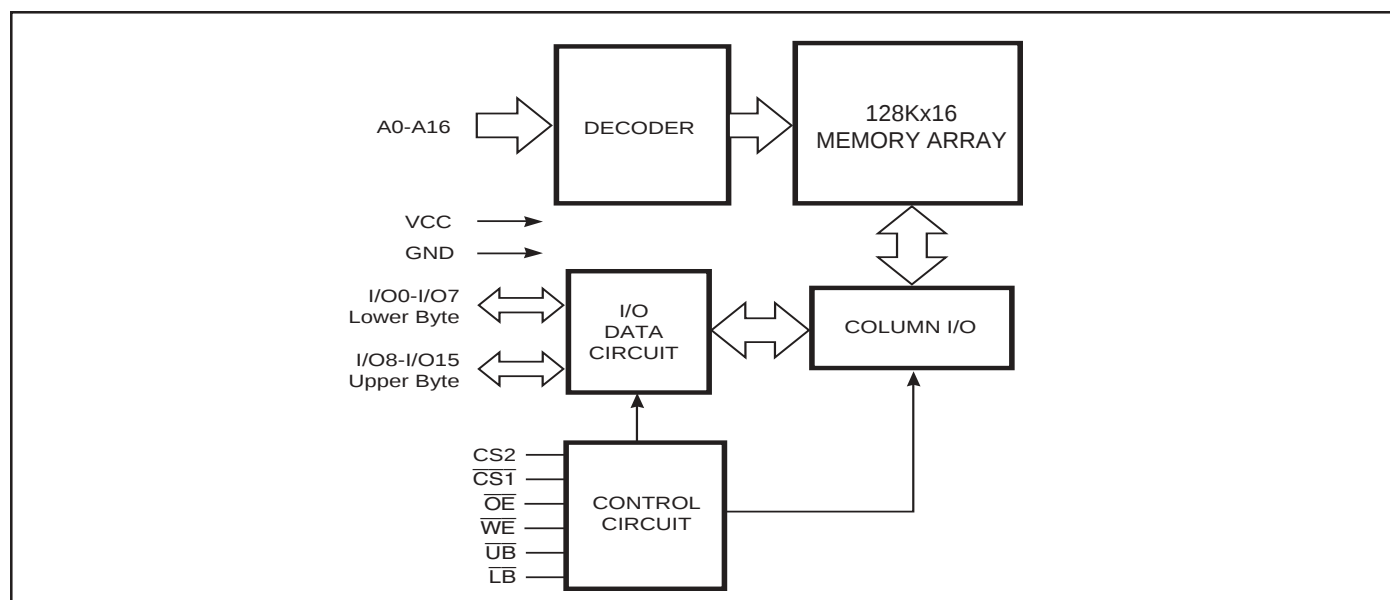
The *ISSI* IS61LV12816L/IS61LV12816LL is a high-speed, 2,097,152-bit static RAM organized as 131,072 words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 8 ns with low power consumption.

When $\overline{CE}$ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, $\overline{CE}$ and $\overline{OE}$. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory. A data byte allows Upper Byte ($\overline{UB}$) and Lower Byte ($\overline{LB}$) access.

The IS61LV12816L/IS61LV12816LL is packaged in the JEDEC standard 44-pin TSOP, 44-pin LQFP, and 48-pin mini BGA (6mm x 8mm).

FUNCTIONAL BLOCK DIAGRAM



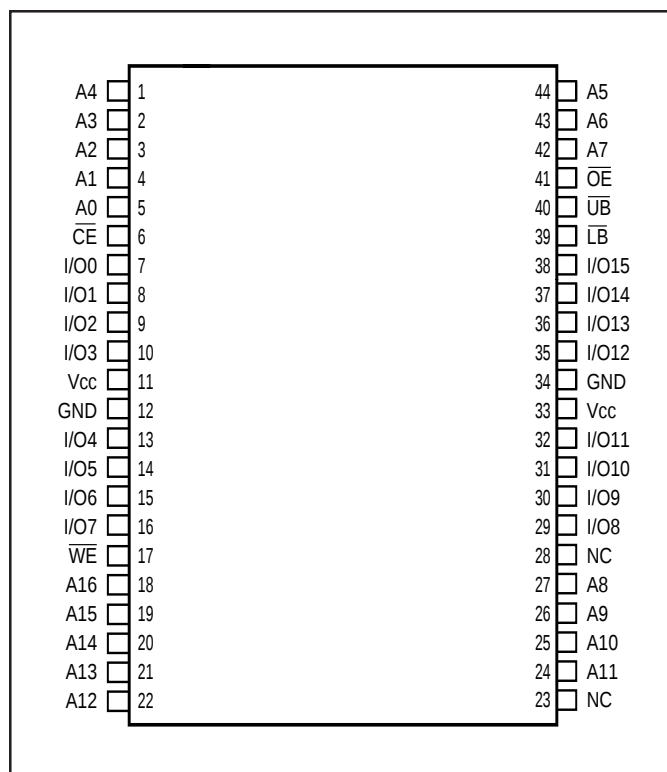
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TRUTH TABLE

	I/O PIN							
Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O0-I/O7	I/O8-I/O15	Vcc Current
Not Selected	X	H	X	X	X	High-Z	High-Z	IsB1, IsB2
Output Disabled	H	L	H	X	X	High-Z	High-Z	Icc
	X	L	X	H	H	High-Z	High-Z	
Read	H	L	L	L	H	DOUT	High-Z	Icc
	H	L	L	H	L	High-Z	DOUT	
	H	L	L	L	L	DOUT	DOUT	
Write	L	L	X	L	H	DIN	High-Z	Icc
	L	L	X	H	L	High-Z	DIN	
	L	L	X	L	L	DIN	DIN	

PIN CONFIGURATION

44-Pin TSOP (T)



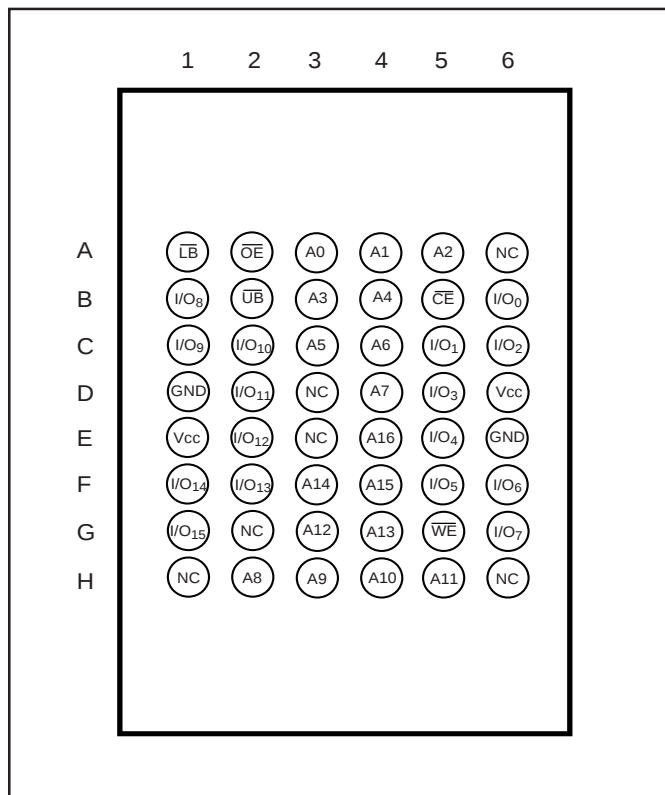
PIN DESCRIPTIONS

A0-A16	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
Vcc	Power
GND	Ground

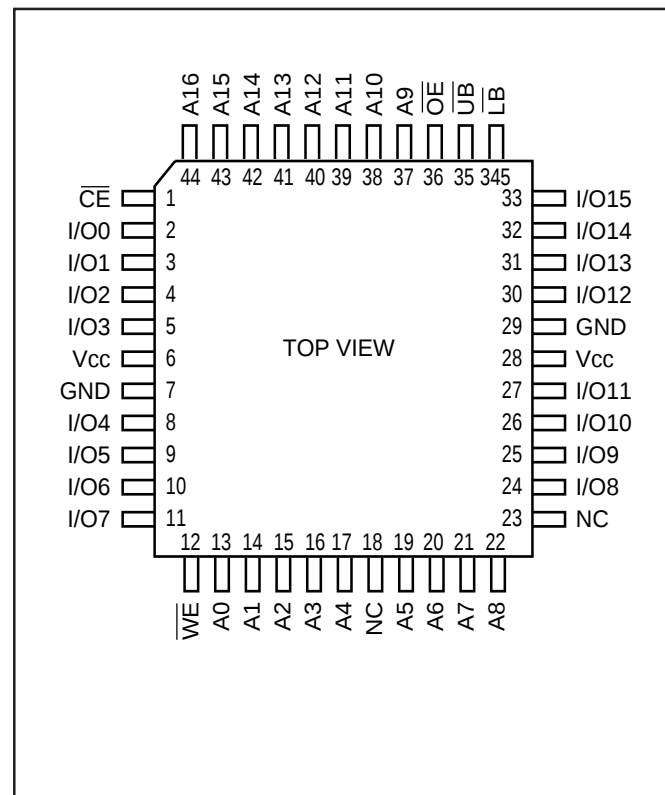
IS61LV12816L, IS61LV12816LL

PIN CONFIGURATION

48-Pin mini BGA (B)



44-Pin LQFP (LQ)



PIN DESCRIPTIONS

A0-A16	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
Vcc	Power
GND	Ground

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V _{CC}	Power Supply Voltage Relative to GND	−0.5 to 4.0V	V
V _{TERM}	Terminal Voltage with Respect to GND	−0.5 to V _{CC} + 0.5	V
T _{STG}	Storage Temperature	−65 to + 150	°C
P _T	Power Dissipation	1.0	W
I _{OUT}	DC Output Current	±20	mA

Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	V _{CC}
Commercial	0°C to + 70°C	3.3V + 10%, -5%
Industrial	−40°C to + 85°C	3.3V + 10%, -5%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = −4.0 mA	2.4	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA	—	0.4	V
V _{IH}	Input HIGH Voltage ⁽¹⁾		2	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage ⁽¹⁾		−0.3	0.8	V
I _{LI}	Input Leakage	GND - V _{IN} - V _{CC}	−1	1	μA
I _{LO}	Output Leakage	GND - V _{OUT} - V _{CC} , Outputs Disabled	−1	1	μA

Note:

1. V_{IL} (min.) = −0.3V DC; V_{IL} (min.) = −2.0V AC (pulse width - 2.0 ns).
V_{IH} (max.) = V_{CC} + 0.3V DC; V_{IH} (max.) = V_{CC} + 2.0V AC (pulse width - 2.0 ns).

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POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

IS61LV12816L

Symbol	Parameter	Test Conditions		-8 ns		-10 ns		Unit
				Min.	Max.	Min.	Max.	
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., $\overline{CE}$ = V _{IL} I _{OUT} = 0 mA, f = Max.	Com. Ind.	—	65 70	—	60 65	mA
I _{SB1}	TTL Standby Current (TTL Inputs)	V _{CC} = Max., V _{IN} = V _{IH} or V _{IL} $\overline{CE} \cdot V_{IH}$, f = max	Com. Ind.	—	30 35	—	25 30	mA
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{CC} = Max., $\overline{CE}$ - V _{CC} - 0.2V, V _{IN} > V _{CC} - 0.2V, or V _{IN} - 0.2V, f = 0	Com. Ind.	—	3	—	3	mA
				—	4	—	4	mA

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

IS61LV12816LL

Symbol	Parameter	Test Conditions		-12 ns		-15 ns		Unit
				Min.	Max.	Min.	Max.	
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., $\overline{CE}$ = V _{IL} I _{OUT} = 0 mA, f = Max.	Com. Ind.	—	50 60	—	45 50	mA
I _{SB1}	TTL Standby Current (TTL Inputs)	V _{CC} = Max., V _{IN} = V _{IH} or V _{IL} $\overline{CE} \cdot V_{IH}$, f = max	Com. Ind.	—	15 20	—	15 20	mA
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{CC} = Max., $\overline{CE}$ - V _{CC} - 0.2V, V _{IN} > V _{CC} - 0.2V, or V _{IN} - 0.2V, f = 0	Com. Ind.	—	200	—	200	μA
				—	300	—	300	μA

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

CAPACITANCE⁽¹⁾

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{OUT}	Input/Output Capacitance	V _{OUT} = 0V	8	pF

Note:

1. Tested initially and after any design or process changes that may affect these parameters.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

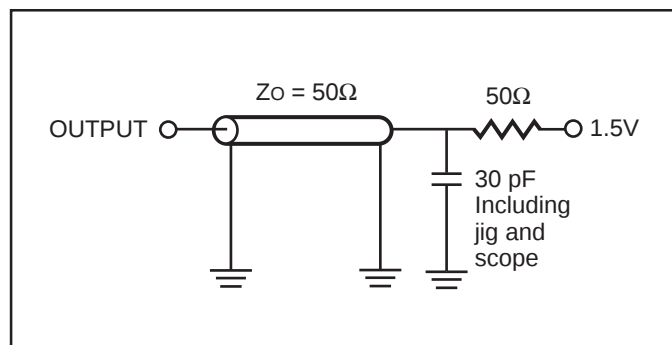


Figure 1.

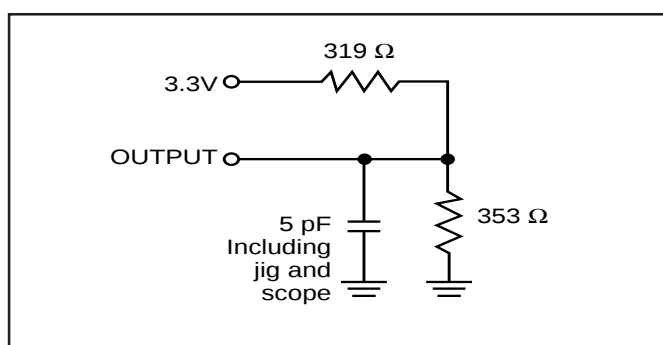


Figure 2.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

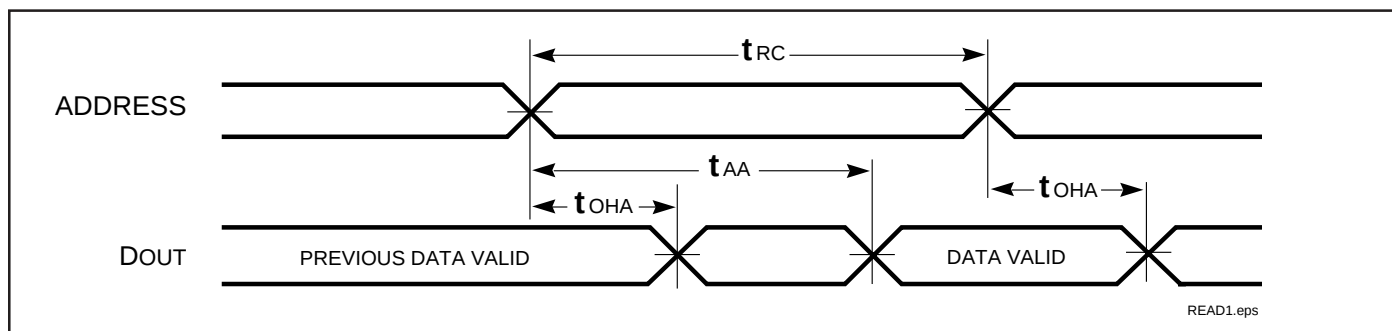
Symbol	Parameter	IS61LV12816L				IS61LV12816LL				Unit
		-8 ns		-10 ns		-12 ns		-15 ns		
		Min.	Max	Min.	Max.	Min.	Max.	Min.	Max.	
t _{RC}	Read Cycle Time	8	—	10	—	12	—	15	—	ns
t _{AA}	Address Access Time	—	8	—	10	—	12	—	15	ns
t _{OHA}	Output Hold Time	3	—	3	—	3	—	3	—	ns
t _{ACE}	$\overline{CE}$ Access Time	8	—	—	10	—	12	—	15	ns
t _{DOE}	$\overline{OE}$ Access Time	—	3.5	—	4	—	5	—	6	ns
t _{HZOE} ⁽²⁾	$\overline{OE}$ to High-Z Output	—	3.5	—	4	—	5	0	6	ns
t _{LZOE} ⁽²⁾	$\overline{OE}$ to Low-Z Output	0	—	0	—	0	—	0	—	ns
t _{HZCE} ⁽²⁾	$\overline{CE}$ to High-Z Output	0	3.5	0	4	0	5	0	8	ns
t _{LZCE} ⁽²⁾	$\overline{CE}$ to Low-Z Output	3.5	—	3	—	3	—	3	—	ns
t _{BA}	$\overline{LB}$, $\overline{UB}$ Access Time	—	3.5	—	4	—	5	—	6	ns
t _{HZB} ⁽²⁾	$\overline{LB}$, $\overline{UB}$ to High-Z Output	0	3.5	0	4	0	5	0	6	ns
t _{LZB} ⁽²⁾	$\overline{LB}$, $\overline{UB}$ to Low-Z Output	0	—	0	—	0	—	0	—	ns

Notes:

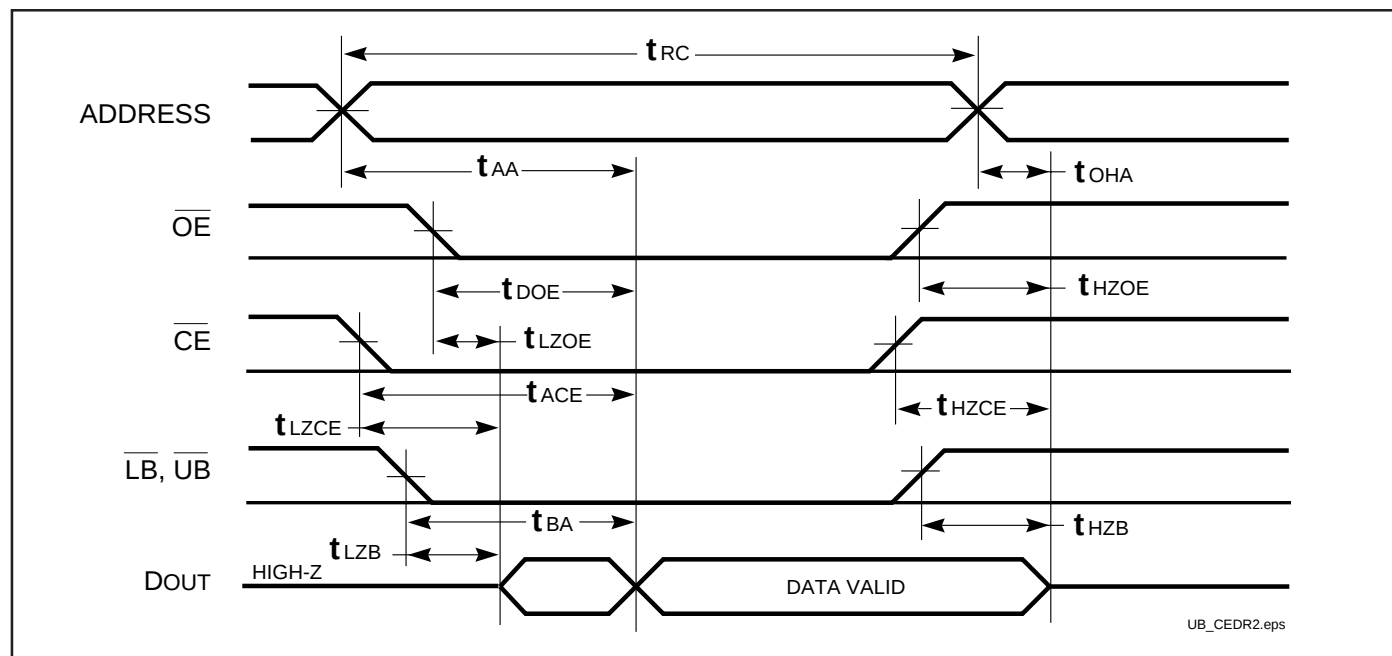
1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

READ CYCLE NO. 1^(1,2) (Address Controlled) ($\overline{CE} = \overline{OE} = V_{IL}$, $\overline{UB}$ or $\overline{LB} = V_{IL}$)



READ CYCLE NO. 2^(1,3)



Notes:

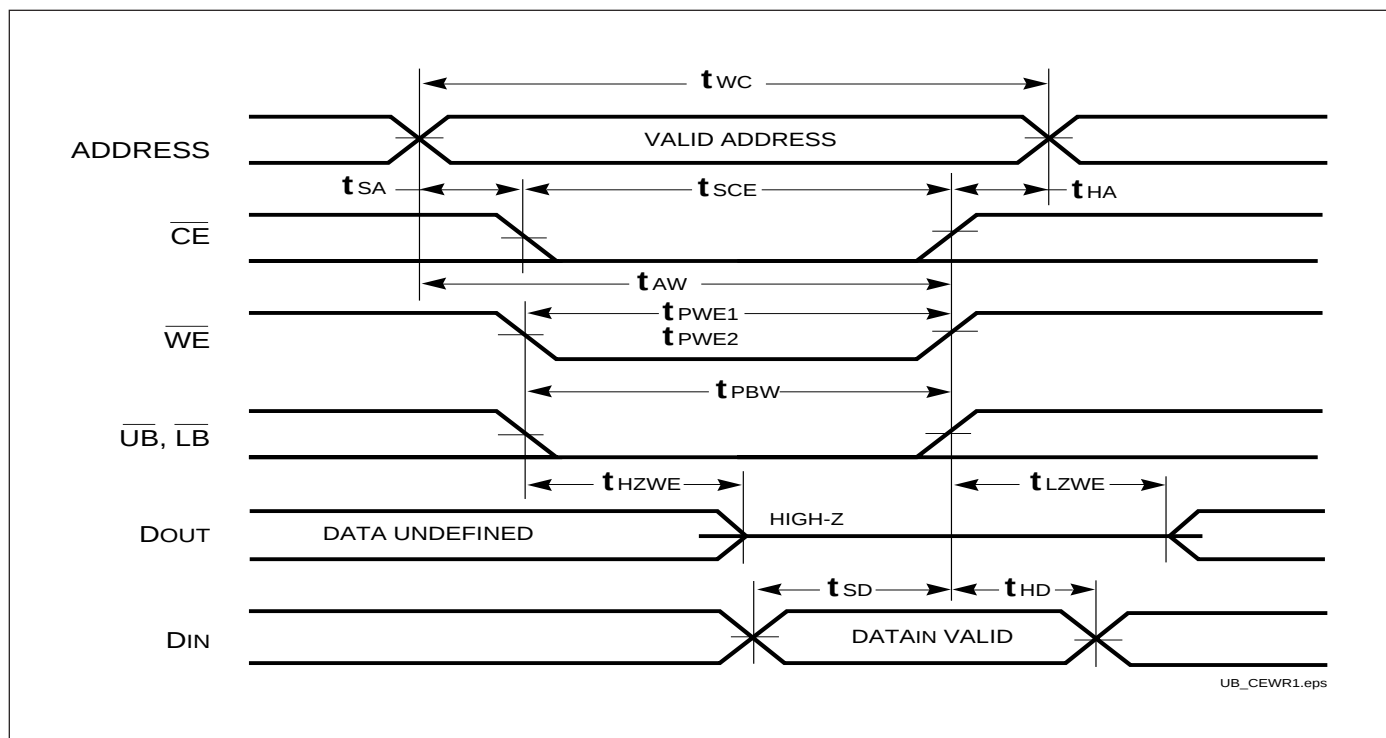
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{UB}$, or $\overline{LB} = V_{IL}$.
3. Address is valid prior to or coincident with $\overline{CE}$ LOW transition.

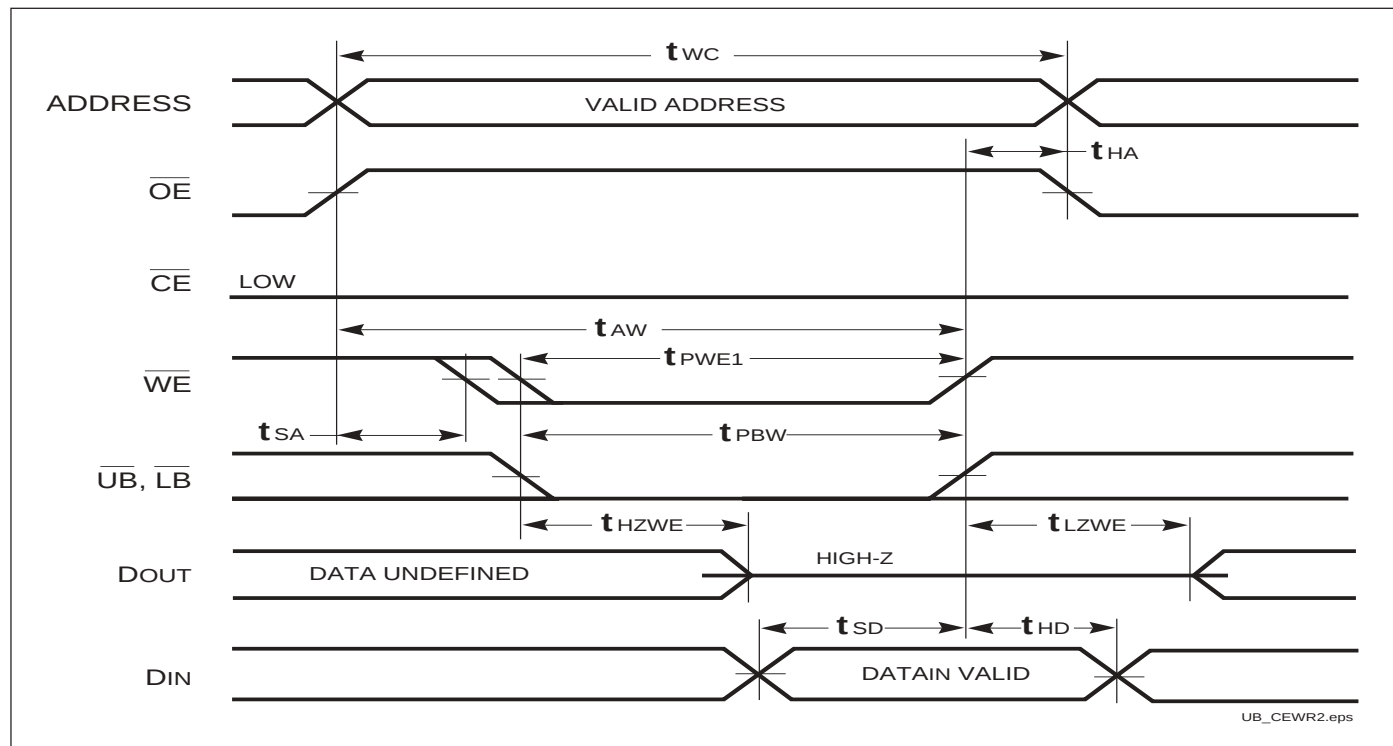
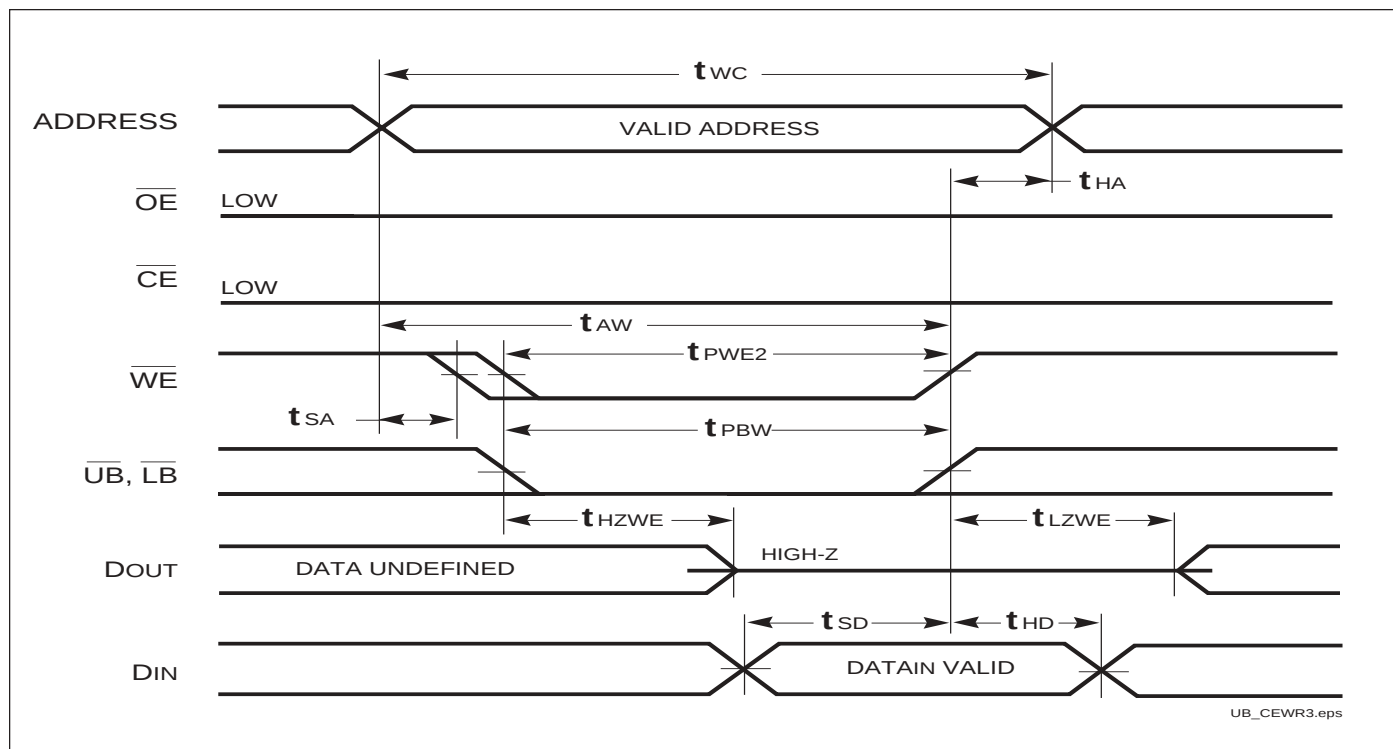
WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

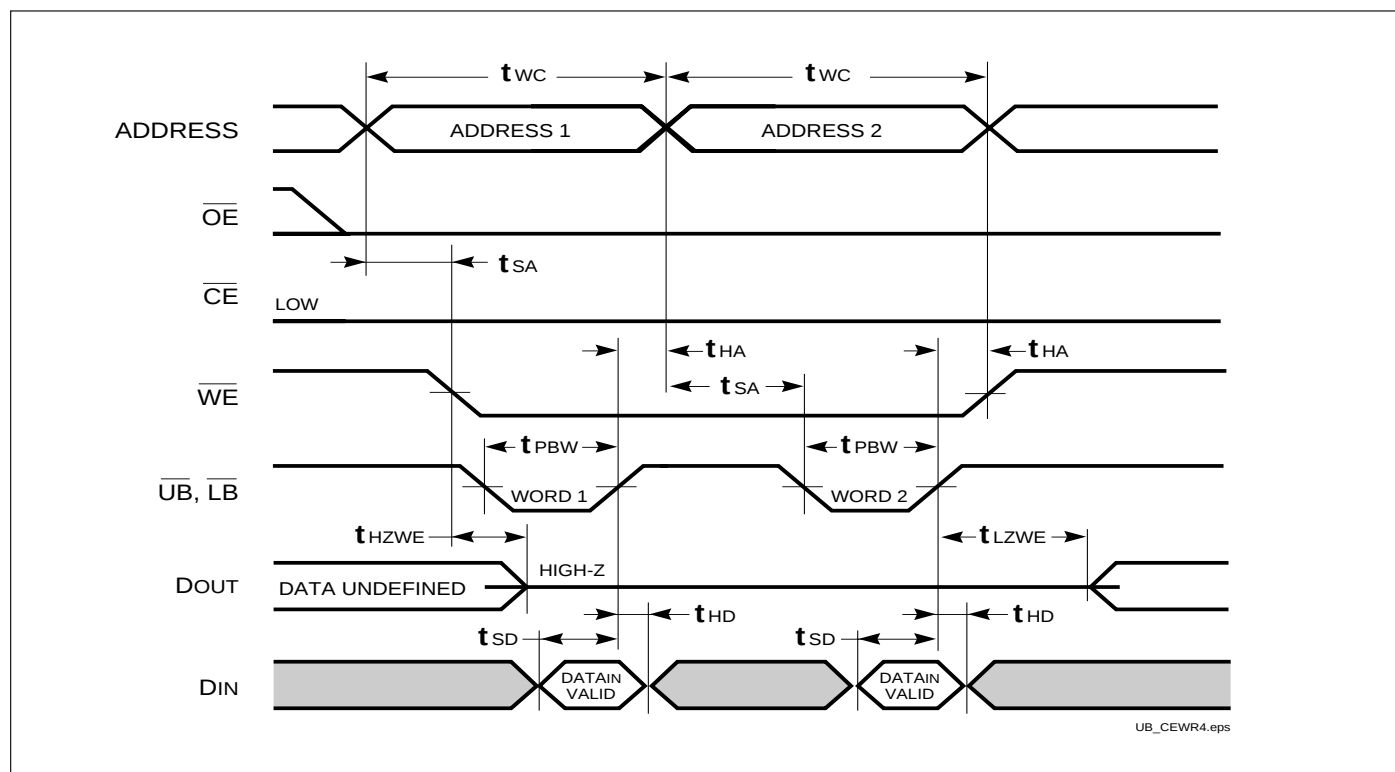
Symbol	Parameter	IS61LV12816L				IS61LV12816LL				Unit
		-8 ns		-10 ns		-12 ns		-15 ns		
		Min.	Max	Min.	Max.	Min.	Max.	Min.	Max.	
t _{WC}	Write Cycle Time	8	—	10	—	12	—	15	—	ns
t _{SCE}	$\overline{\text{CE}}$ to Write End	7	—	8	—	8	—	10	—	ns
t _{AW}	Address Setup Time to Write End	7	—	8	—	8	—	10	—	ns
t _{HA}	Address Hold from Write End	0	—	0	—	0	—	0	—	ns
t _{SA}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t _{PWB}	$\overline{\text{LB}}$, $\overline{\text{UB}}$ Valid to End of Write	6.5	—	8	—	9	—	10	—	ns
t _{PWE1}	$\overline{\text{WE}}$ Pulse Width ($\overline{\text{OE}}$ = HIGH)	6	—	7	—	8	—	10	—	ns
t _{PWE2}	$\overline{\text{WE}}$ Pulse Width ($\overline{\text{OE}}$ = LOW)	6.5	—	8	—	10	—	11	—	ns
t _{SD}	Data Setup to Write End	4	—	5	—	6	—	7	—	ns
t _{HD}	Data Hold from Write End	0	—	0	—	0	—	0	—	ns
t _{HZWE} ⁽³⁾	$\overline{\text{WE}}$ LOW to High-Z Output	—	3	—	4	—	5	—	6	ns
t _{LZWE} ⁽³⁾	$\overline{\text{WE}}$ HIGH to Low-Z Output	0	—	0	—	0	—	0	—	ns

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0V to 3.0V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{UB}}$ or $\overline{\text{LB}}$, and $\overline{\text{WE}}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.

WRITE CYCLE NO. 1^(1,2) ($\overline{CE}$ Controlled, $\overline{OE}$ = HIGH or LOW)

WRITE CYCLE NO. 2⁽¹⁾ ($\overline{WE}$ Controlled, $\overline{OE}$ = HIGH during Write Cycle)**WRITE CYCLE NO. 3** ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)

WRITE CYCLE NO. 4 ($\overline{\text{LB}}$, $\overline{\text{UB}}$ Controlled, Back-to-Back Write) ^(1,3)**Notes:**

1. The internal Write time is defined by the overlap of $\overline{\text{CE}} = \text{LOW}$, $\overline{\text{UB}}$ and/or $\overline{\text{LB}} = \text{LOW}$, and $\overline{\text{WE}} = \text{LOW}$. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The t_{SA} , t_{HA} , t_{SD} , and t_{HD} timing is referenced to the rising or falling edge of the signal that terminates the Write.
2. Tested with $\overline{\text{OE}}$ HIGH for a minimum of 4 ns before $\overline{\text{WE}} = \text{LOW}$ to place the I/O in a HIGH-Z state.
3. $\overline{\text{WE}}$ may be held LOW across many address cycles and the $\overline{\text{LB}}$, $\overline{\text{UB}}$ pins can be used to control the Write function.

IS61LV12816L, IS61LV12816LL**IS61LV12816L****ORDERING INFORMATION****Commercial Range: 0°C to +70°C**

Speed(ns)	Order Part No.	Package
8	IS61LV12816L-8B	mini BGA (6mm x 8mm)
	IS61LV12816L-8LQ	LQFP
	IS61LV12816L-8T	Plastic TSOP
10	IS61LV12816L-10B	mini BGA (6mm x 8mm)
	IS61LV12816L-10LQ	LQFP
	IS61LV12816L-10T	Plastic TSOP

IS61LV12816LL**ORDERING INFORMATION****Commercial Range: 0°C to +70°C**

Speed(ns)	Order Part No.	Package
12	IS61LV12816LL-12B	mini BGA (6mm x 8mm)
	IS61LV12816LL-12LQ	LQFP
	IS61LV12816LL-12T	Plastic TSOP
15	IS61LV12816LL-15B	mini BGA (6mm x 8mm)
	IS61LV12816LL-15LQ	LQFP
	IS61LV12816LL-15T	Plastic TSOP

IS61LV12816L**ORDERING INFORMATION****Industrial Range: -40°C to +85°C**

Speed(ns)	Order Part No.	Package
8	IS61LV12816L-8BI	mini BGA (6mm x 8mm)
	IS61LV12816L-8LQI	LQFP
	IS61LV12816L-8TI	Plastic TSOP
10	IS61LV12816L-10BI	mini BGA (6mm x 8mm)
	IS61LV12816L-10LQI	LQFP
	IS61LV12816L-10TI	Plastic TSOP

IS61LV12816LL**ORDERING INFORMATION****Industrial Range: -40°C to +85°C**

Speed(ns)	Order Part No.	Package
12	IS61LV12816LL-12BI	mini BGA (6mm x 8mm)
	IS61LV12816LL-12LQI	LQFP
	IS61LV12816LL-12TI	Plastic TSOP
15	IS61LV12816LL-15BI	mini BGA (6mm x 8mm)
	IS61LV12816LL-15LQI	LQFP
	IS61LV12816LL-15TI	Plastic TSOP