



STW55NM60ND

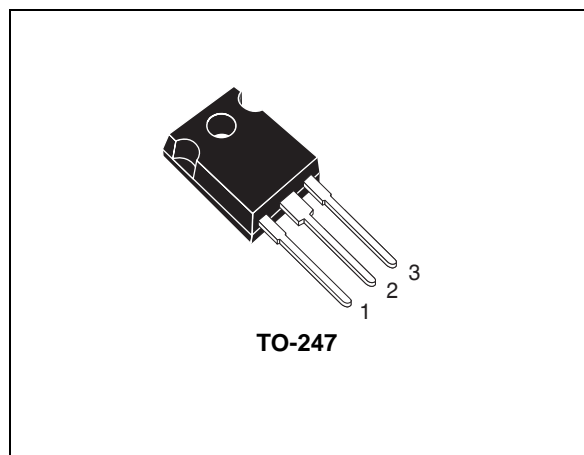
N-channel 600 V, 0.047 Ω typ., 51 A FDmesh™ II Power MOSFET
(with fast diode) in a TO-247 package

Datasheet — production data

Features

Type	V _{DSS} (@T _J max)	R _{DS(on)} max	I _D
STW55NM60ND	650 V	< 0.060 Ω	51 A

- The worldwide best R_{DS(on)} amongst the fast recovery diode devices in TO-247
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance
- High dv/dt and avalanche capabilities



Application

- Switching applications

Description

This FDmesh™ II Power MOSFET with intrinsic fast-recovery body diode is produced using the second generation of MDmesh™ technology. Utilizing a new strip-layout vertical structure, this revolutionary device features extremely low on-resistance and superior switching performance. It is ideal for bridge topologies and ZVS phase-shift converters.

Figure 1. Internal schematic diagram

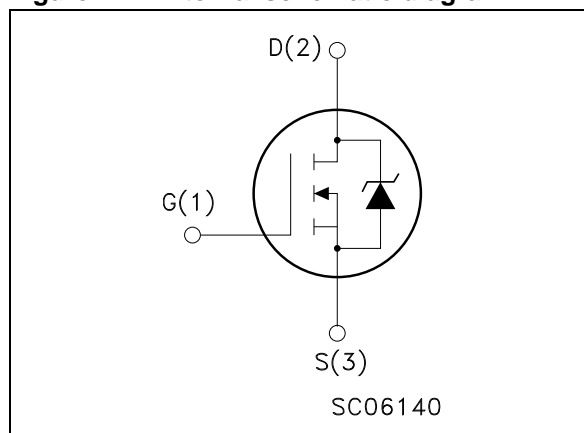


Table 1. Device summary

Order code	Marking	Package	Packaging
STW55NM60ND	55NM60ND	TO-247	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate- source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	51	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	32	A
$I_{DM}^{(1)}$	Drain current (pulsed)	204	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	350	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	40	V/ns
T_{stg}	Storage temperature	-55 to 150	$^{\circ}\text{C}$
T_j	Max. operating junction temperature	150	$^{\circ}\text{C}$

1. Pulse width limited by safe operating area

2. $I_{SD} \leq 51\text{ A}$, $di/dt \leq 600\text{ A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.36	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	50	$^{\circ}\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose	300	$^{\circ}\text{C}$

Table 4. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	15	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AS}$, $V_{DD} = 50\text{ V}$)	1600	mJ

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1 \text{ mA}$, $V_{GS} = 0$	600			V
$dv/dt^{(1)}$	Drain source voltage slope	$V_{DD}=480 \text{ V}$, $I_D = 51 \text{ A}$, $V_{GS} = 10 \text{ V}$	30			V/ns
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 600 \text{ V}$ $V_{DS} = 600 \text{ V}$, $T_C = 125^{\circ}\text{C}$			10 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20 \text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10 \text{ V}$, $I_D = 25.5 \text{ A}$		0.047	0.060	Ω

1. Characteristic value at turn off on inductive load.

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15 \text{ V}$, $I_D = 25.5 \text{ A}$		45		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 50 \text{ V}$, $f = 1 \text{ MHz}$, $V_{GS} = 0$		5800 300 30		pF pF pF
$C_{oss \text{ eq.}}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0$, $V_{DS} = 0 \text{ to } 480 \text{ V}$		900		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 300 \text{ V}$, $I_D = 25.5 \text{ A}$ $R_G = 4.7 \Omega$, $V_{GS} = 10 \text{ V}$ (see Figure 19), (see Figure 14)		33 68 188 96		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 480 \text{ V}$, $I_D = 51 \text{ A}$, $V_{GS} = 10 \text{ V}$, (see Figure 15)		190 30 90		nC nC nC
R_g	Gate input resistance	$f=1 \text{ MHz}$ Gate DC Bias = 0 Test signal level = 20 mV Open drain		2.5		Ω

1. Pulsed: pulse duration= 300 μs , duty cycle 1.5%

2. $C_{oss \text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				51	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				204	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 51\text{ A}$, $V_{GS} = 0$			1.3	V
t_{rr}	Reverse recovery time	$I_{SD} = 51\text{ A}$, $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$ (see Figure 16)		200		ns
Q_{rr}	Reverse recovery charge			1.8		μC
I_{RRM}	Reverse recovery current			18		A
t_{rr}	Reverse recovery time	$I_{SD} = 51\text{ A}$, $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16)		280		ns
Q_{rr}	Reverse recovery charge			3.4		μC
I_{RRM}	Reverse recovery current			24		A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

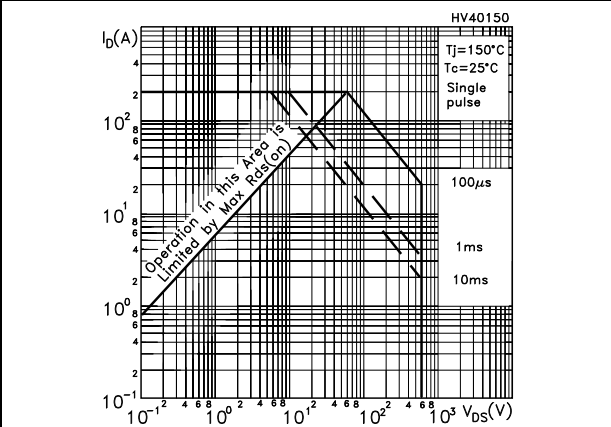


Figure 3. Thermal impedance

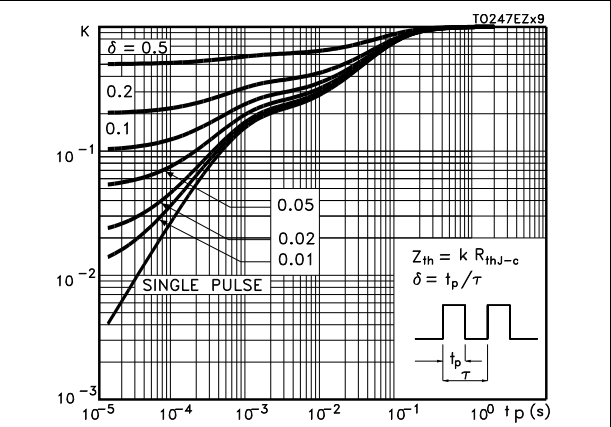


Figure 4. Output characteristics

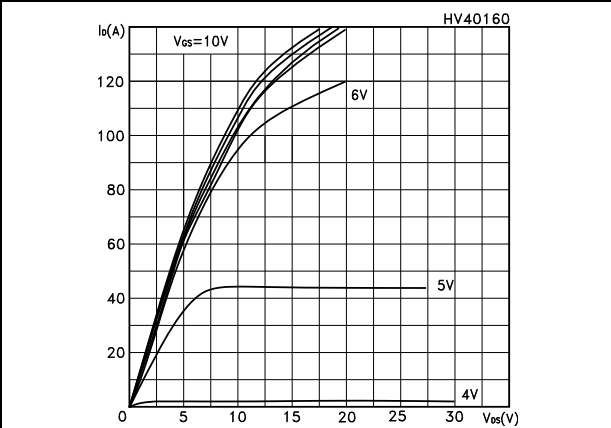


Figure 5. Transfer characteristics

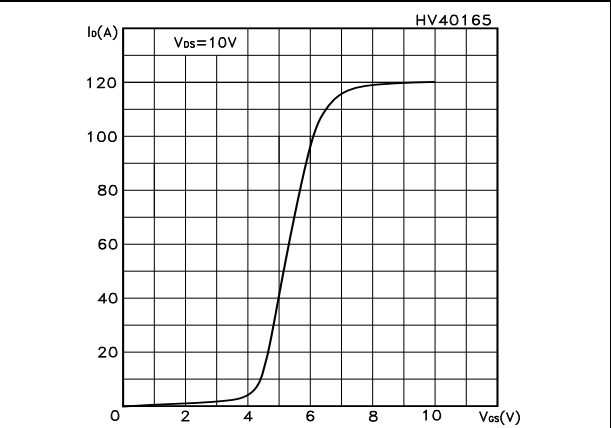


Figure 6. Transconductance

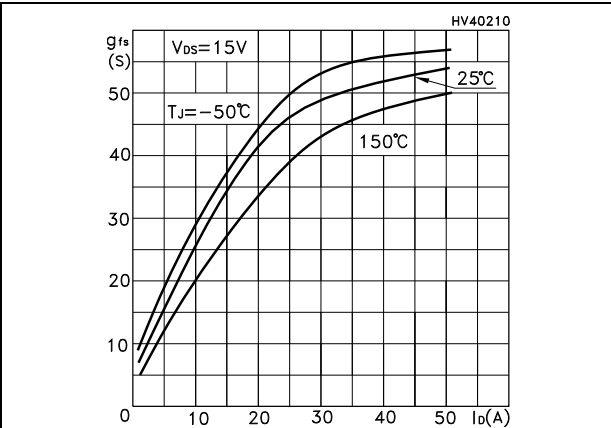


Figure 7. Static drain-source on-resistance

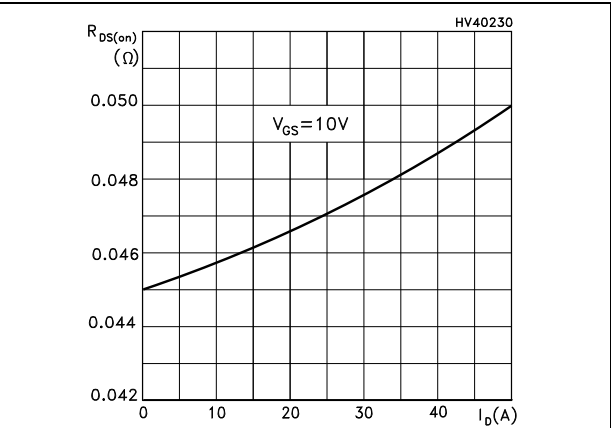
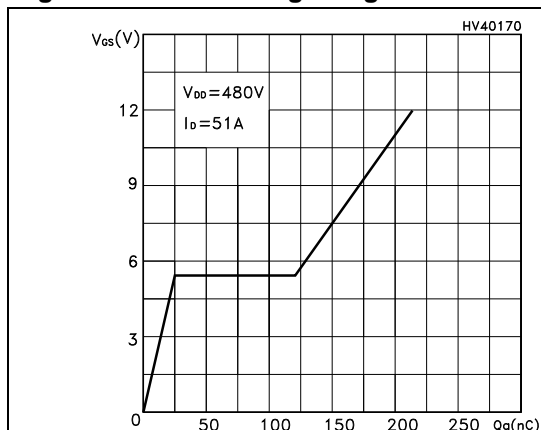
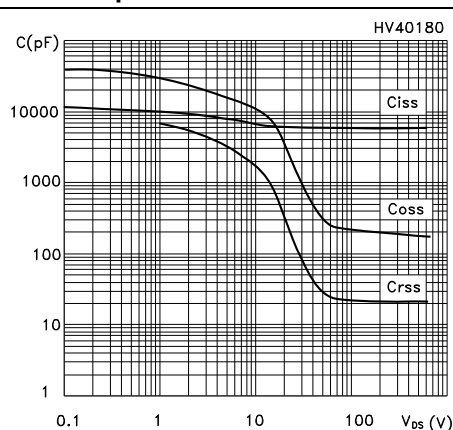
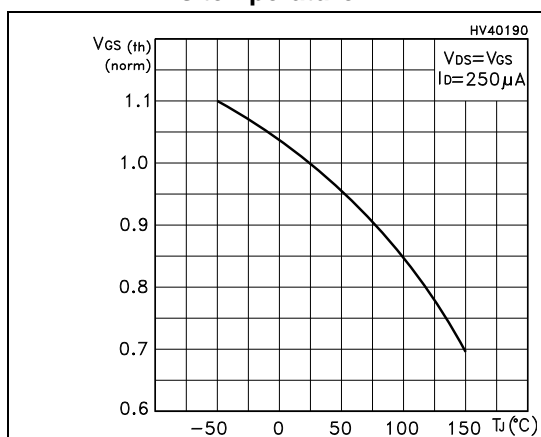
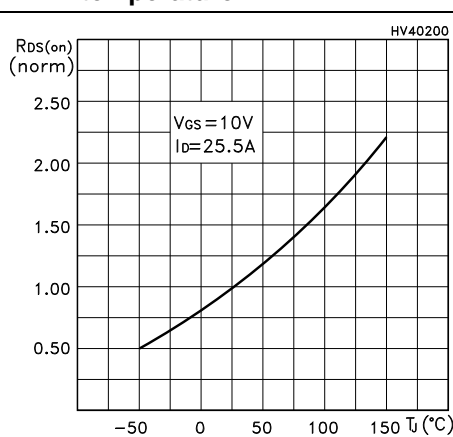
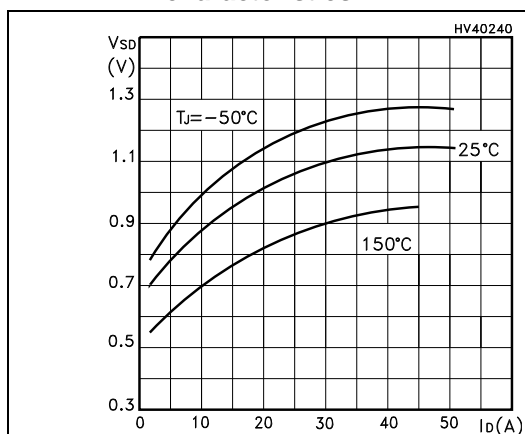
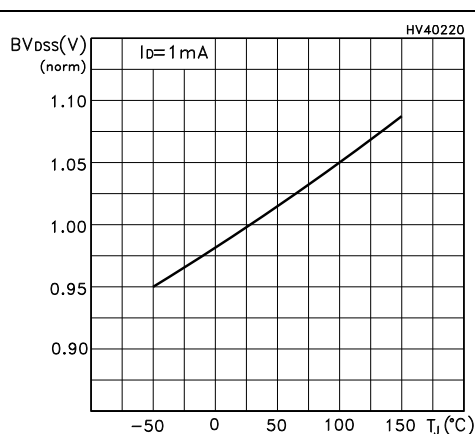


Figure 8. Gate charge vs gate-source voltage**Figure 9. Capacitance variations****Figure 10. Normalized gate threshold voltage vs temperature****Figure 11. Normalized on resistance vs temperature****Figure 12. Source-drain diode forward characteristics****Figure 13. Normalized BVDS vs temperature**

3 Test circuits

Figure 14. Switching times test circuit for resistive load

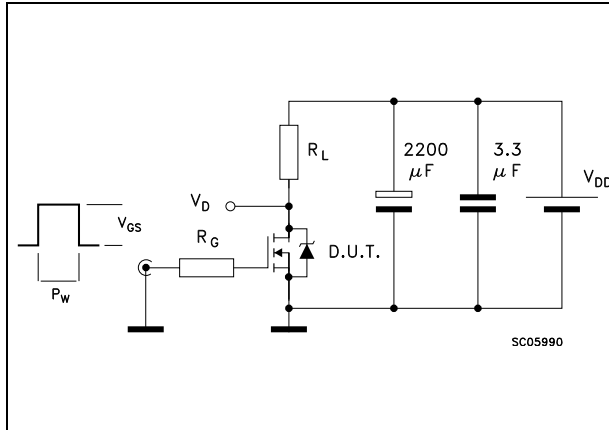


Figure 15. Gate charge test circuit

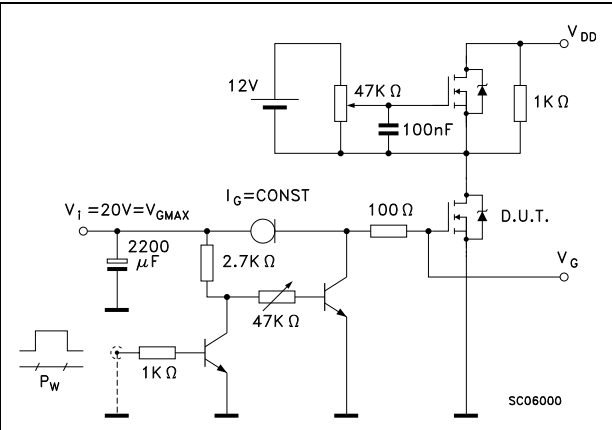


Figure 16. Test circuit for inductive load switching and diode recovery times

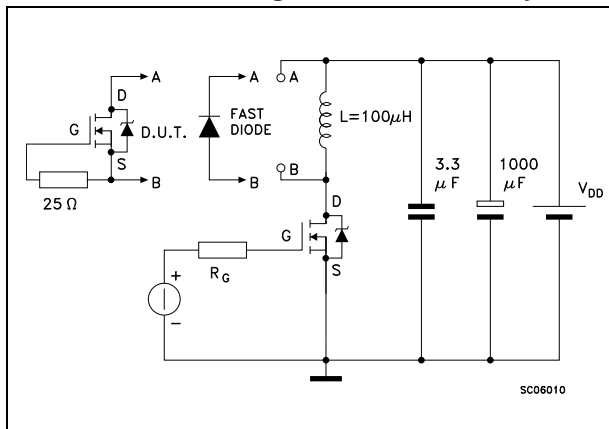


Figure 17. Unclamped Inductive load test circuit

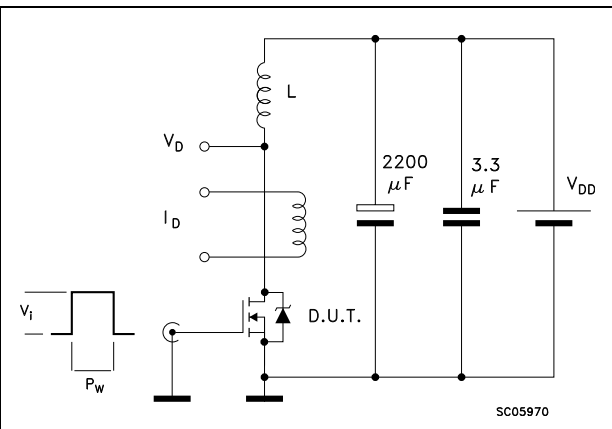


Figure 18. Unclamped inductive waveform

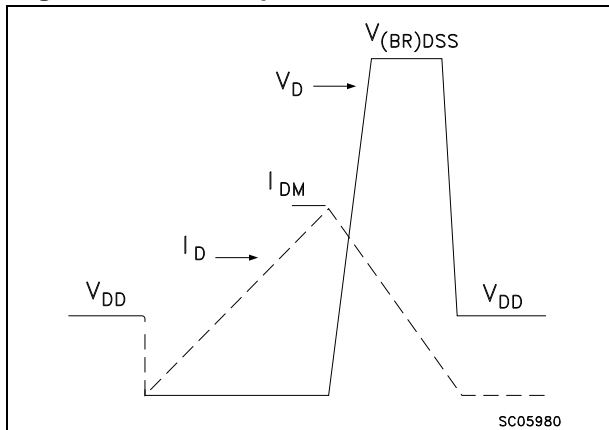
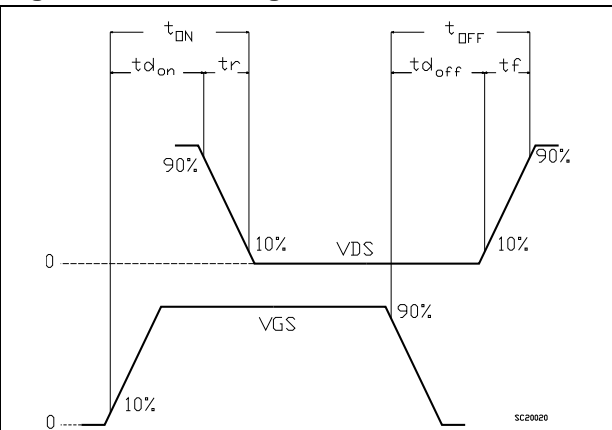


Figure 19. Switching time waveform



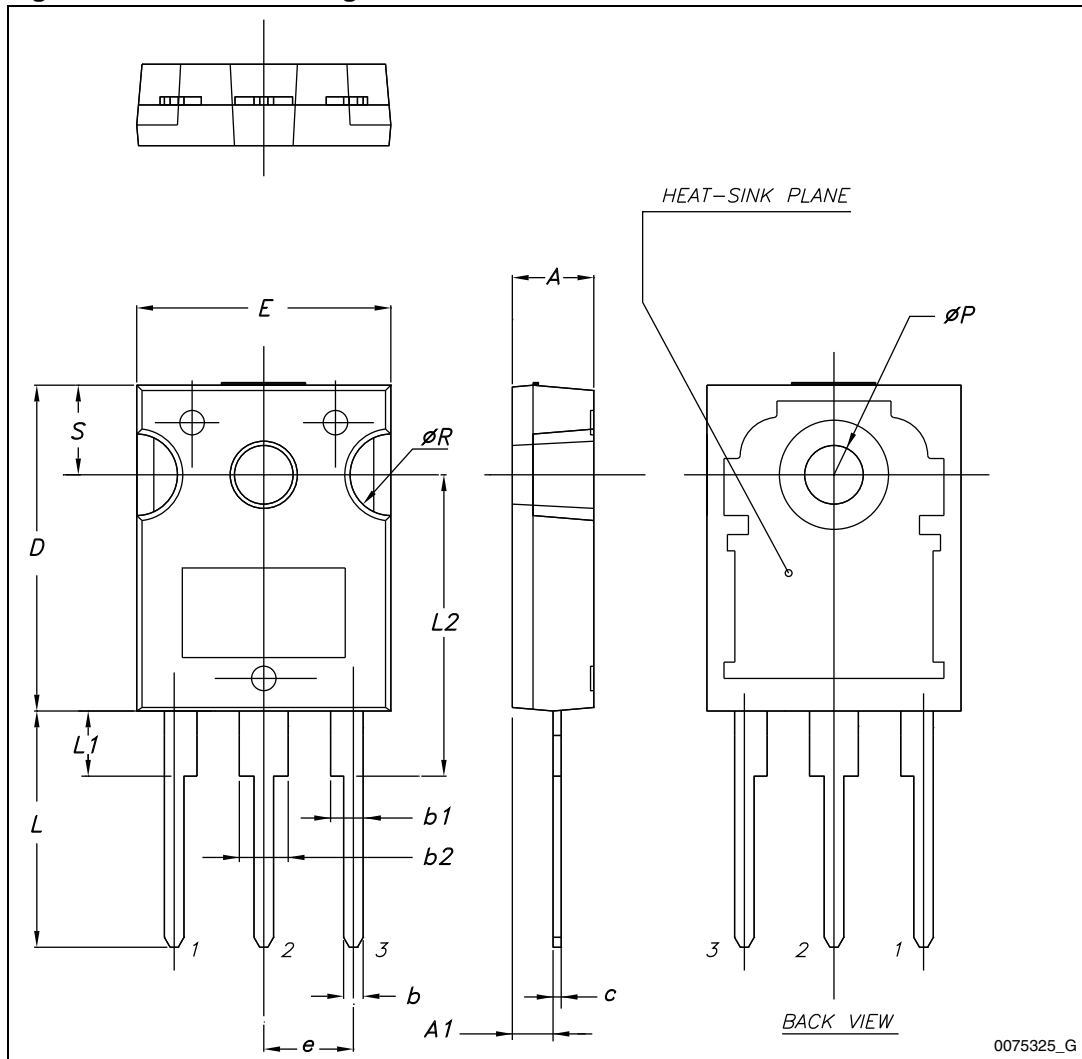
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

Figure 20. TO-247 drawing



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
16-Nov-2007	1	First release.
22-Apr-2008	2	Document status promoted from preliminary data to datasheet.
19-Dec-2012	3	Title changed on the cover page. Minor text changes. Updated Section 4: Package mechanical data .

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