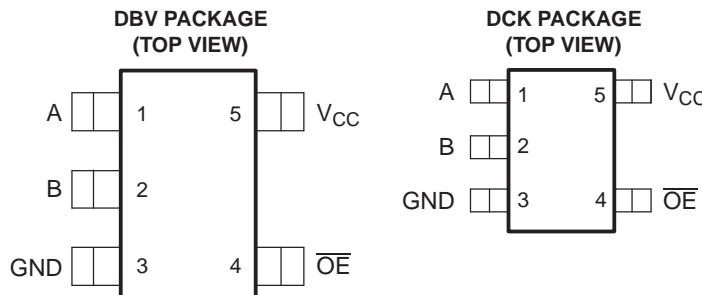


## FEATURES

- 5- $\Omega$  Switch Connection Between Two Ports
- TTL-Compatible Control Input Levels



See mechanical drawings for dimensions.

## DESCRIPTION/ORDERING INFORMATION

The SN74CBT1G384 features a single high-speed line switch. The switch is disabled when the output-enable ( $\overline{OE}$ ) input is high.

### ORDERING INFORMATION

| $T_A$   | PACKAGE <sup>(1)</sup> | ORDERABLE PART NUMBER | TOP-SIDE MARKING <sup>(2)</sup> |
|---|------------------------|-----------------------|---------------------------------|
| $-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$ | SOT (SOT-23) – DBV     | Reel of 3000          | S8D_                            |
|   |                        | Reel of 250           |                                 |
|   | SOT (SC-70) – DCK      | Reel of 3000          | S8_                             |
|   |                        | Reel of 250           |                                 |

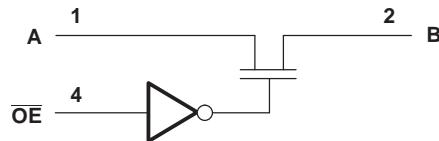
(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

(2) The actual top-side marking has one additional character that designates the assembly/test site.

### FUNCTION TABLE

| INPUT<br>$\overline{OE}$ | FUNCTION        |
|--------------------------|-----------------|
| L                        | A port = B port |
| H                        | Disconnect      |

### LOGIC DIAGRAM (POSITIVE LOGIC)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# SN74CBT1G384

## SINGLE FET BUS SWITCH

SCDS065G – JULY 1998 – REVISED JUNE 2006



### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|               |                                      | MIN  | MAX | UNIT |
|---------------|--------------------------------------|------|-----|------|
| $V_{CC}$      | Supply voltage range                 | -0.5 | 7   | V    |
| $V_I$         | Input voltage range <sup>(2)</sup>   | -0.5 | 7   | V    |
|               | Continuous channel current           |      | 128 | mA   |
| $I_{IK}$      | Input clamp current<br>$V_{I/O} < 0$ |      | -50 | mA   |
| $\theta_{JA}$ | DBV package                          | 206  |     | °C/W |
|               | DCK package                          | 252  |     |      |
| $T_{stg}$     | Storage temperature range            | -65  | 150 | °C   |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

### Recommended Operating Conditions<sup>(1)</sup>

|          |                                  | MIN | MAX | UNIT |
|----------|----------------------------------|-----|-----|------|
| $V_{CC}$ | Supply voltage                   | 4   | 5.5 | V    |
| $V_{IH}$ | High-level control input voltage | 2   |     | V    |
| $V_{IL}$ | Low-level control input voltage  |     | 0.8 | V    |
| $T_A$    | Operating free-air temperature   | -40 | 85  | °C   |

- (1) All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER      | TEST CONDITIONS   |  |  |               | MIN | TYP <sup>(1)</sup> | MAX | UNIT |
|----------------|---|--|--|---------------|-----|--------------------|-----|------|
| $V_{IK}$       | $V_{CC} = 4.5$ V, $I_I = -18$ mA                                    |  |  |               |     | -1.2               |     | V    |
| $I_I$          | $V_{CC} = 5.5$ V, $V_I = 5.5$ V or GND                              |  |  |               |     | ±1                 |     | µA   |
| $I_{CC}$       | $V_{CC} = 5.5$ V, $I_O = 0$ , $V_I = V_{CC}$ or GND                 |  |  |               |     | 1                  |     | µA   |
| $C_i$          | Control input   | $V_I = 3$ V or 0                           |  |               |     | 3                  |     | pF   |
| $C_{io(OFF)}$  |   | $V_O = 3$ V or 0, $\overline{OE} = V_{CC}$ |  |               |     | 4                  |     | pF   |
| $r_{on}^{(2)}$ | $V_{CC} = 4$ V, TYP at $V_{CC} = 4$ V, $V_I = 2.4$ V, $I_I = 15$ mA |  |  |               | 14  | 20                 |     | Ω    |
|                | $V_{CC} = 4.5$ V  | $V_I = 0$                                  |  | $I_I = 64$ mA |     | 5                  | 7   |      |
|                |   |  |  | $I_I = 30$ mA |     | 5                  | 7   |      |
|                |   | $V_I = 2.4$ V, $I_I = 15$ mA               |  |               | 10  | 15                 |     |      |

- (1) All typical values are at  $V_{CC} = 5$  V (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

- (2) Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower voltage of the two (A or B) terminals.

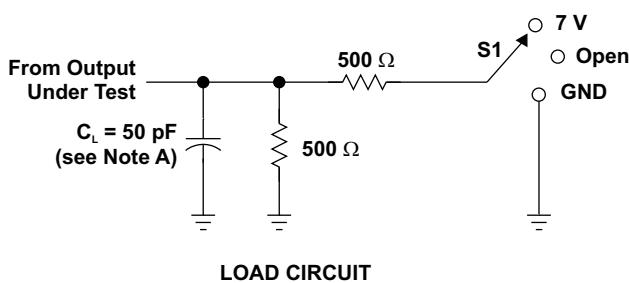
## Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see [Figure 1](#))

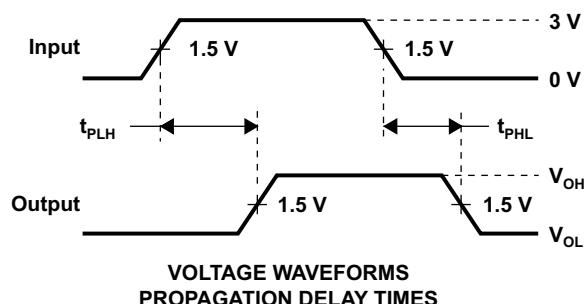
| PARAMETER      | FROM<br>(INPUT) | TO<br>(OUTPUT) | $V_{CC} = 4 \text{ V}$ |      | $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ |      | UNIT |
|----------------|-----------------|----------------|------------------------|------|--|------|------|
|                |                 |                | MIN                    | MAX  | MIN                                      | MAX  |      |
| $t_{pd}^{(1)}$ | A or B          | B or A         |                        | 0.35 |  | 0.25 | ns   |
| $t_{en}$       | $\overline{OE}$ | A or B         |                        | 5.5  | 1.6                                      | 4.9  | ns   |
| $t_{dis}$      | $\overline{OE}$ | A or B         |                        | 4.5  | 1  | 4.2  | ns   |

(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

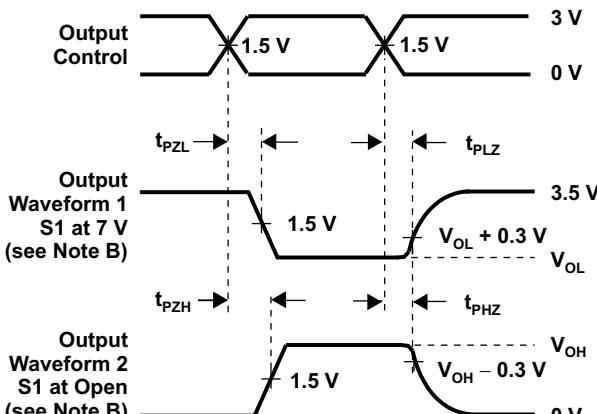
**PARAMETER MEASUREMENT INFORMATION**



| TEST              | S1   |
|-------------------|------|
| $t_{pd}$          | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V  |
| $t_{PHZ}/t_{PZH}$ | Open |



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES**

NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.  
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
D. The output is measured with one input transition per measurement.  
E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
H.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

| Orderable part number | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)       |
|-----------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------------|
| SN74CBT1G384DBVR      | Active        | Production           | SOT-23 (DBV)   5 | 3000   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -40 to 85    | (S8DG, S8DJ, S8DR)        |
| SN74CBT1G384DBVR.A    | Active        | Production           | SOT-23 (DBV)   5 | 3000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 85    | (S8DG, S8DJ, S8DR)        |
| SN74CBT1G384DBVT      | NRND          | Production           | SOT-23 (DBV)   5 | 250   SMALL T&R       | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -40 to 85    | (S8DJ, S8DR)              |
| SN74CBT1G384DBVT.A    | NRND          | Production           | SOT-23 (DBV)   5 | 250   SMALL T&R       | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 85    | (S8DJ, S8DR)              |
| SN74CBT1G384DCKR      | NRND          | Production           | SC70 (DCK)   5   | 3000   LARGE T&R      | Yes         | NIPDAU   SN   NIPDAU                 | Level-1-260C-UNLIM                | -40 to 85    | (S83, S8G, S8J, S8R, S8U) |
| SN74CBT1G384DCKR.A    | NRND          | Production           | SC70 (DCK)   5   | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | (S83, S8G, S8J, S8R, S8U) |
| SN74CBT1G384DCKT      | NRND          | Production           | SC70 (DCK)   5   | 250   SMALL T&R       | Yes         | NIPDAU   SN   NIPDAU                 | Level-1-260C-UNLIM                | -40 to 85    | (S83, S8J, S8R)           |
| SN74CBT1G384DCKT.A    | NRND          | Production           | SC70 (DCK)   5   | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | (S83, S8J, S8R)           |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

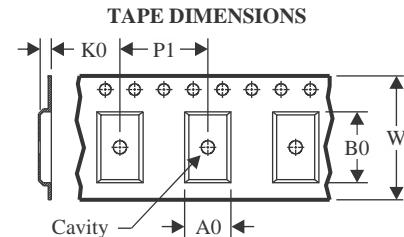
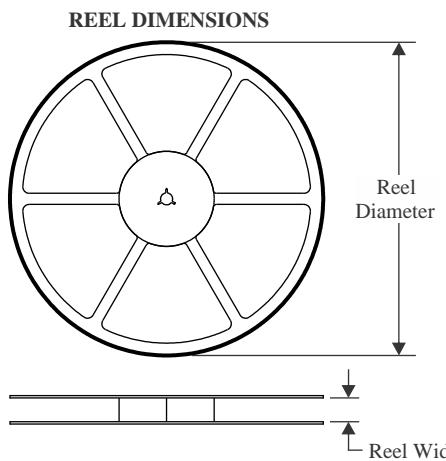
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

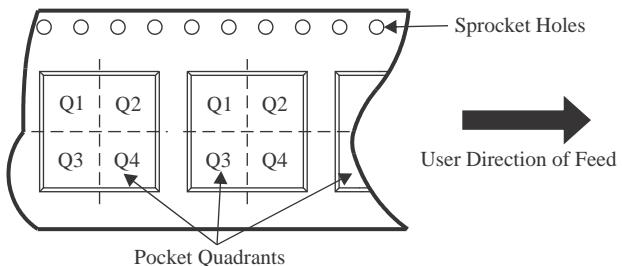
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**TAPE AND REEL INFORMATION**


|    |   |
|----|---|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74CBT1G384DBVR | SOT-23       | DBV             | 5    | 3000 | 178.0              | 9.0                | 3.3     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| SN74CBT1G384DBVT | SOT-23       | DBV             | 5    | 250  | 178.0              | 9.0                | 3.3     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| SN74CBT1G384DBVT | SOT-23       | DBV             | 5    | 250  | 180.0              | 8.4                | 3.23    | 3.17    | 1.37    | 4.0     | 8.0    | Q3            |
| SN74CBT1G384DCKR | SC70         | DCK             | 5    | 3000 | 180.0              | 8.4                | 2.47    | 2.3     | 1.25    | 4.0     | 8.0    | Q3            |
| SN74CBT1G384DCKR | SC70         | DCK             | 5    | 3000 | 178.0              | 9.0                | 2.4     | 2.5     | 1.2     | 4.0     | 8.0    | Q3            |
| SN74CBT1G384DCKR | SC70         | DCK             | 5    | 3000 | 179.0              | 8.4                | 2.2     | 2.5     | 1.2     | 4.0     | 8.0    | Q3            |
| SN74CBT1G384DCKT | SC70         | DCK             | 5    | 250  | 178.0              | 9.0                | 2.4     | 2.5     | 1.2     | 4.0     | 8.0    | Q3            |
| SN74CBT1G384DCKT | SC70         | DCK             | 5    | 250  | 180.0              | 8.4                | 2.47    | 2.3     | 1.25    | 4.0     | 8.0    | Q3            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74CBT1G384DBVR | SOT-23       | DBV             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| SN74CBT1G384DBVT | SOT-23       | DBV             | 5    | 250  | 180.0       | 180.0      | 18.0        |
| SN74CBT1G384DBVT | SOT-23       | DBV             | 5    | 250  | 202.0       | 201.0      | 28.0        |
| SN74CBT1G384DCKR | SC70         | DCK             | 5    | 3000 | 202.0       | 201.0      | 28.0        |
| SN74CBT1G384DCKR | SC70         | DCK             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| SN74CBT1G384DCKR | SC70         | DCK             | 5    | 3000 | 203.0       | 203.0      | 35.0        |
| SN74CBT1G384DCKT | SC70         | DCK             | 5    | 250  | 180.0       | 180.0      | 18.0        |
| SN74CBT1G384DCKT | SC70         | DCK             | 5    | 250  | 202.0       | 201.0      | 28.0        |

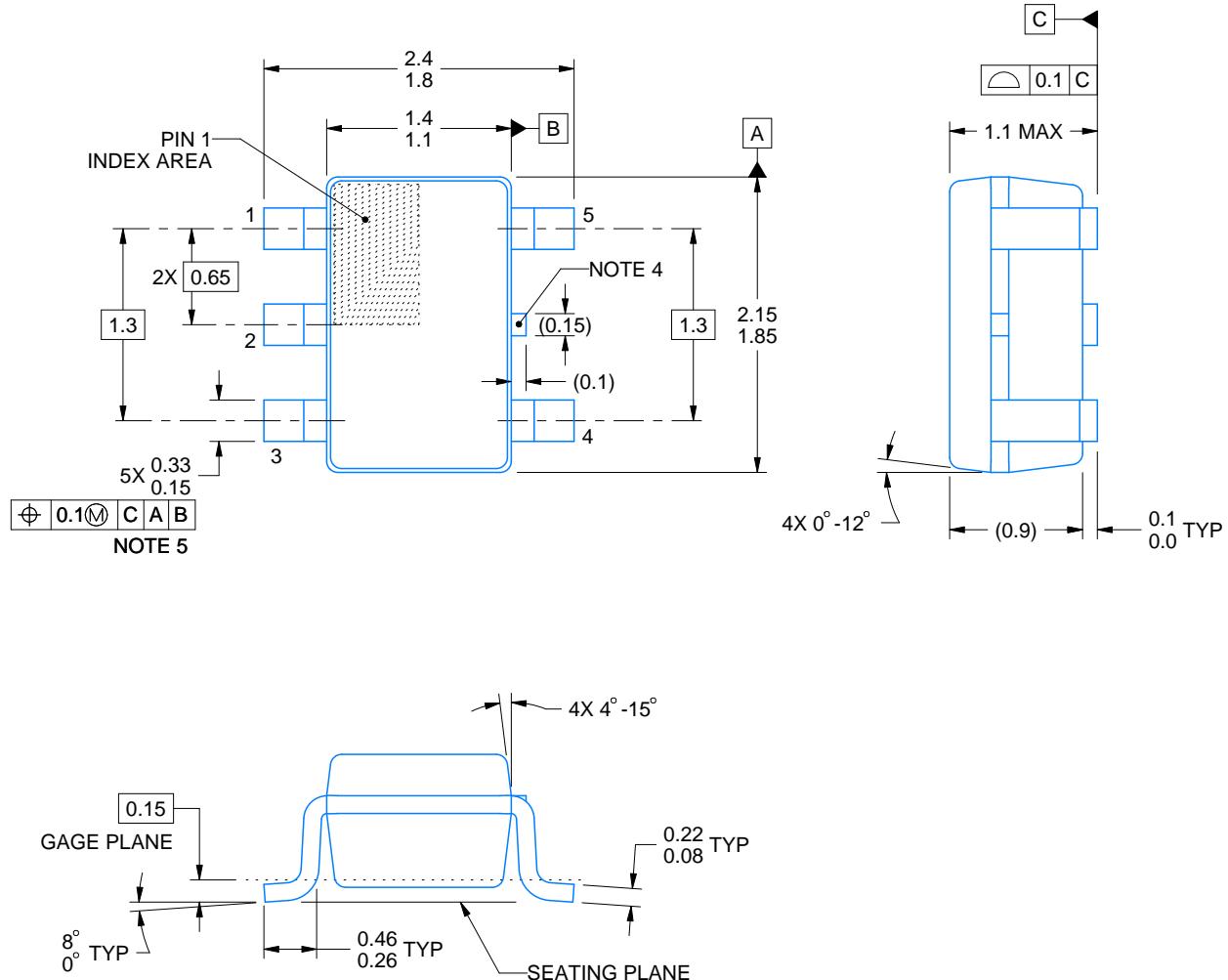
## PACKAGE OUTLINE

**DCK0005A**



## SOT - 1.1 max height

## SMALL OUTLINE TRANSISTOR



4214834/G 11/2024

## NOTES:

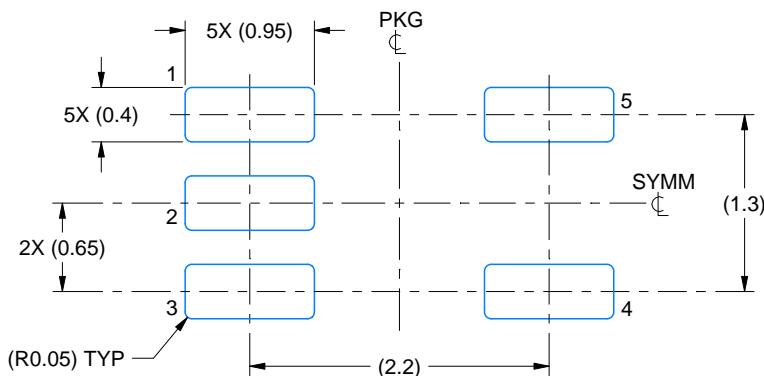
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

# EXAMPLE BOARD LAYOUT

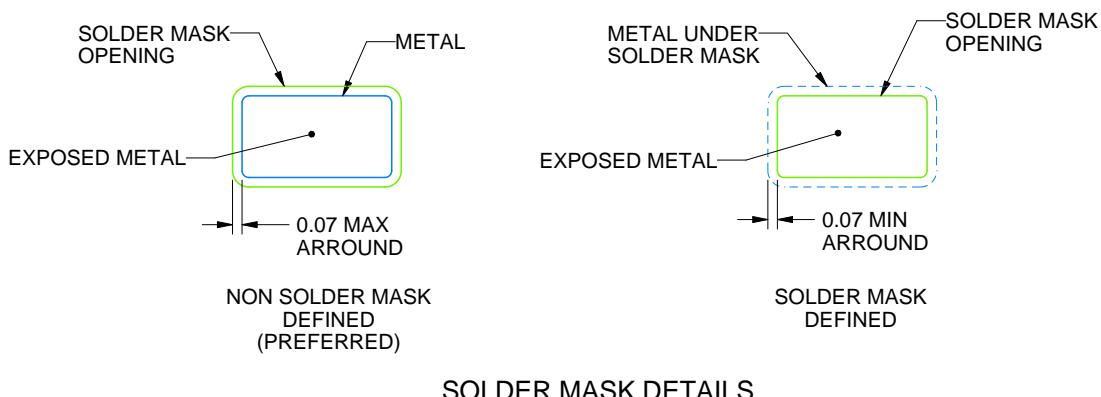
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

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NOTES: (continued)

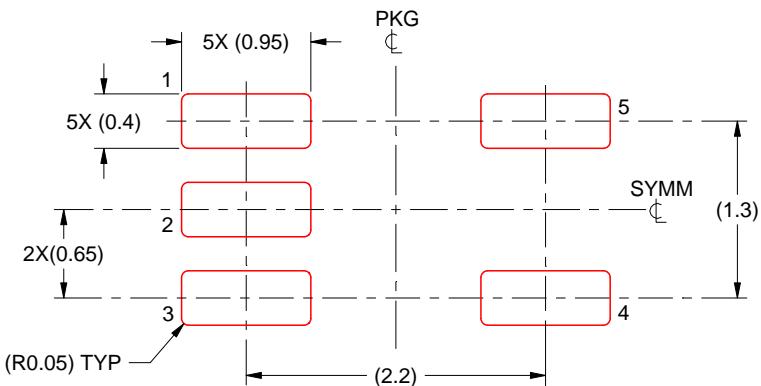
7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:18X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

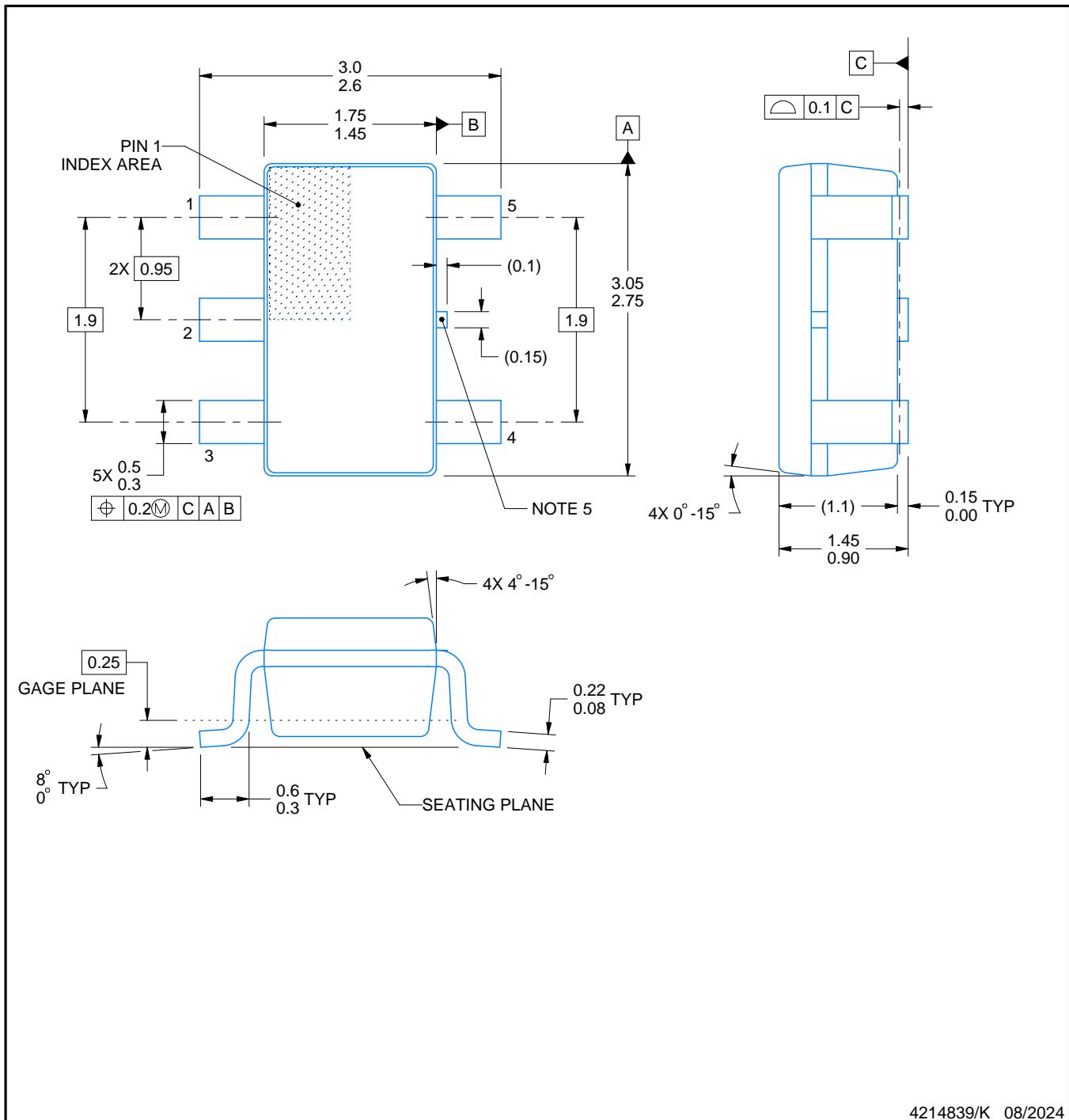
## PACKAGE OUTLINE

**DBV0005A**



## **SOT-23 - 1.45 mm max height**

## SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

## NOTES:

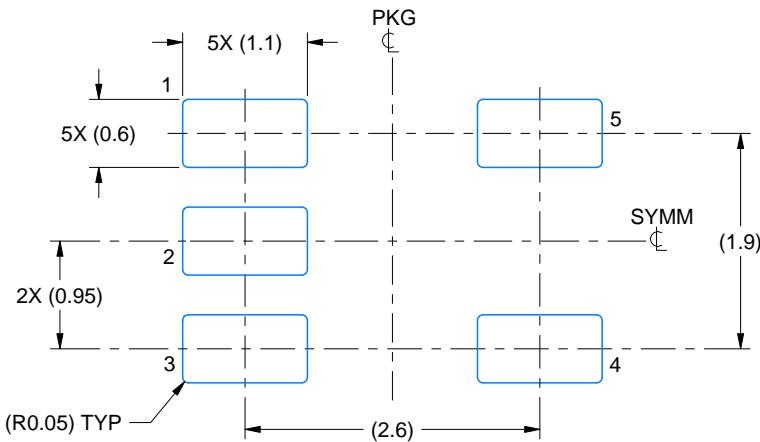
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

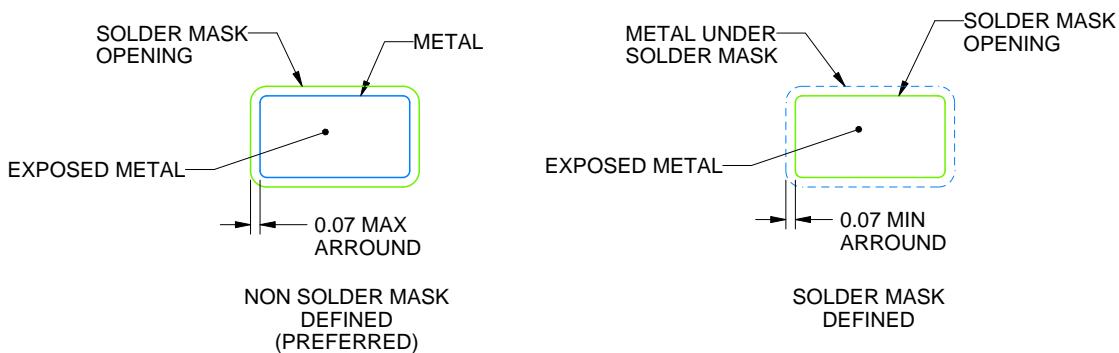
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

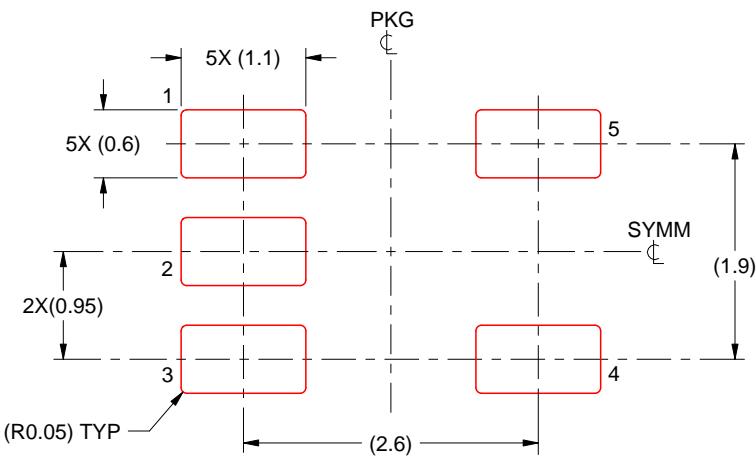
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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