

Low Skew, 1-to-16 LVCMOS / LVTTTL Clock Driver

Product Features

- 16 LVCMOS/LVTTTL outputs (4 banks of 4 outputs)
- Selectable differential or single-ended clock inputs
- CLK1, nCLK1 pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- CLK0 supports the following input types: LVCMOS, LVTTTL
- Maximum output frequency: 250MHz
- Independent bank control for $\div 1$ or $\div 2$ operation
- Independent output bank voltage settings for 3.3V, 2.5V, or 1.8V operations
- Output skew: 170ps (max)
- Bank skew: 30ps (max)
- Part-to-part skew: 750ps (max)
- 3.3V core, 3.3V, 2.5V, or 1.8V output operating supply
- -40° to $+85^{\circ}\text{C}$ ambient operating temperature
- Available packages:
-Pb-free & green 48-pin LQFP(FB)

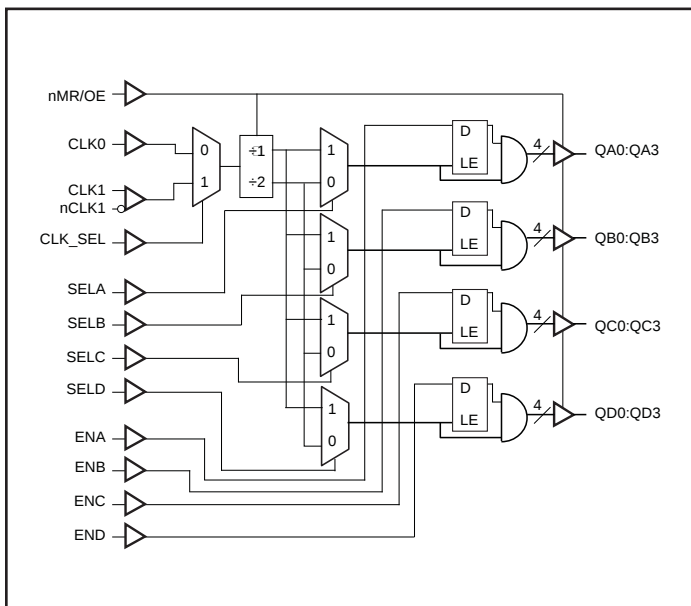
Product Description

The PI6C487016 is a low skew, 1:16 LVCMOS/LVTTTL Clock Driver. The device has 4 banks of 4 outputs and each bank can be independently selected for $\div 1$ or $\div 2$ frequency operation. Each bank also has its own power supply pins so that the banks can operate at the following different voltage levels: 3.3V, 2.5V, and 1.8V. The low impedance LVCMOS/LVTTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines.

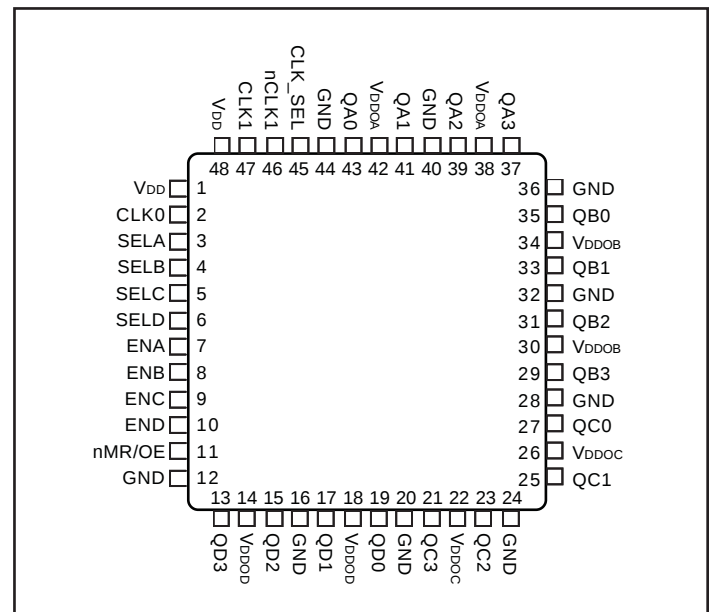
The divide select inputs, SELA: SELD, control the output frequency of each bank with either $\div 1$ or $\div 2$ frequency operation. The bank enable inputs, ENA: END, support enabling and disabling each bank of outputs individually. The outputs synchronized when enabling or disabling the clock outputs. The master reset input nMR/OE, resets the $\div 1/\div 2$ flip flops and also controls the active and high impedance states of all outputs.

The PI6C487016 is characterized to operate with the core at 3.3V and the output banks at 3.3V, 2.5V or 1.8V.

Block Diagram



Pin Description



Pin Descriptions

Number	Name	Type		Description
1, 48	V _{DD}	Power		Core supply pins (3.3V)
2	CLK0	Input	Pulldown	LVC MOS / LVTTL clock input
3, 4, 5, 6	SELA : SELD	Input	Pullup	Controls frequency division for outputs. LVC MOS / LVTTL interface levels. QAx:QDx
7, 8, 9, 10	ENA : END	Input	Pullup	Output enable for QAx : QDx Outputs. Active HIGH. If pin is LOW, outputs drive low. LVC MOS / LVTTL interface levels.
11	nMR/OE	Input	Pullup	Master reset. When LOW, resets the ÷1/÷2 flip flops and sets the outputs to high impedance. LVC MOS / LVTTL interface levels.
12, 16, 20, 24, 28, 32, 36, 40, 44	GND	Power		Supply Ground
13, 15, 17, 19	QD0 : QD3	Output		Bank D Outputs, LVC MOS / LVTTL interface levels.
14, 18	V _{DDOD}	Power		Voltage supply for QD0 : QD3
21, 23, 25, 27	QC0 : QC3	Output		Bank C outputs, LVC MOS / LVTTL interface levels.
22, 26	V _{DDOC}	Power		Voltage supply for QC0 : QC3
29, 31, 33, 35	QB0 : QB3	Output		Bank B outputs, LVC MOS / LVTTL interface levels.
30, 34	V _{DDOB}	Power		Voltage supply for QB0 : QB3
37, 39, 41, 43	QA0 : QA3	Output		Bank A outputs, LVC MOS / LVTTL interface levels.
38, 42	V _{DDOA}	Power		Voltage supply for QA0 : QA3
45	CLK_SEL	Input	Pulldown	Clock select input, when HIGH, select CLK1, nCLK1 inputs. When LOW, selects CLK0 input. LVC MOS / LVTTL interface levels.
46	nCLK1	Input	Pullup	Inverting differential clock input
47	CLK1	Input	Pulldown	Non-inverting differential clock input

Notes:

1. Pullup and Pulldown refer to internal input resistors. See Table 2, Pin characteristics, for typical values.

Function Table

Inputs			Outputs	
nMR/OE	ENx	SELx	Bank X	Qx Frequency
0	X	X	Hi Z	N/A
1	1	0	Active	F _{IN} /2
1	1	1	Active	F _{IN}
1	0	X	Low	N/A

Absolute Maximum Ratings

Supply Voltage, VDD	4.6V
Inputs, V _I	-0.5V to V _{DD} +0.5V
Outputs, V _O	-0.5V to V _{DDO} +0.5V
Package Thermal Impedance, θ_{JA}	47.9° C/W (0lfpm)
Storage Temperature, T _{STG}	-65°C to +150°C

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of products at these conditions or any conditions beyond those listed in the DC Characteristics or AC characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Pin Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
C _{IN}	Input Capacitance			4		pF
R _{PULLDOWN}	Input Pulldown Resistor			51		k Ω
R _{PULLUP}	Input Pullup Resistor			51		
CPD	Power Dissipation Capacitance (per output)	V _{DD} , V _{DDOX} = 3.465V			18	pf
		V _{DD} = 3.465, V _{DDOX} = 2.625V			20	
		V _{DD} = 3.465, V _{DDOX} = 1.895V			30	
R _{OUT}	Output Impedance		5	7	12	Ω

Power Supply DC Characteristics, (V_{DD} = 3.3V $\pm$ 5%, T_A = -40° to +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Units
V _{DD}	Core Supply Voltage	3.135	3.3	3.465	V
V _{DDOX}	Output Supply Voltage	3.135	3.3	3.465	
		2.375	2.5	2.625	
		1.71	1.8	1.89	
I _{DD}	Core Supply Current			100	mA
I _{DDOX}	Output Supply Current ⁽¹⁾			15	

Note:

- Measured with all outputs disabled (EN_x=0, nMR=1)

LVC MOS/LVTTL DC Characteristics, ($V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ$ to $+85^\circ C$)

Symbol	Parameter		Test Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	SELx, ENx, nMR/OE, CLK_SEL		2		$V_{DD} + 0.3$	V
		CLK0		2		$V_{DD} + 0.3$	
V_{IL}	Input Low Voltage	SELx, ENx, nMR/OE, CLK_SEL		-0.3		0.8	
		CLK0		-0.3		1.3	
I_{IH}	Input High Current	ENx, SELx, nMR/OE	$V_{DD} = V_{IN} = 3.465V$			5	μA
		CLK0, CLK_SEL				150	
I_{IL}	Input Low Current	ENx, SELx, nMR/OE	$V_{DD} = 3.465V, V_{IN} = 0V$	-150			
		CLK0, CLK_SEL		-5			
V_{OH}	Output High Voltage ⁽¹⁾		$V_{DDOX} = 3.3 \pm 5\%$	2.6			V
			$V_{DDOX} = 2.5 \pm 5\%$	1.8			
			$V_{DDOX} = 1.8 \pm 5\%$ $I_{OH} = -2mA$	$V_{DD} - 0.45$			
V_{OL}	Output Low Voltage ⁽¹⁾		$V_{DDOX} = 3.3 \pm 5\%$			0.5	
			$V_{DDOX} = 2.5 \pm 5\%$			0.5	
			$V_{DDOX} = 1.8 \pm 5\%$ $I_{OH} = -2mA$			0.45	
I_{OZL}	Output Tristate Current Low			-5			μA
I_{OZH}	Output Tristate Current High					5	

Notes:

1. Outputs terminate with 50Ω to $V_{DDOX}/2$. See Parameter Measurement information, Output Load Test Circuit

Differential DC Characteristics, ($V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ$ to $+85^\circ C$)

Symbol	Parameter		Test Conditions	Min.	Typ.	Max.	Units
I_{IH}	Input High Current	nCLK1	$V_{IN} = V_{DD} = 3.465V$			5	μA
		CLK1	$V_{IN} = V_{DD} = 3.465V$			150	
I_{IL}	Input Low Current	nCLK1	$V_{IN} = 0V, V_{DD} = 3.465V$	-150			
		CLK1	$V_{IN} = 0V, V_{DD} = 3.465V$	-5			
V_{PP}	Peak-to-peak Input Voltage			0.15		1.3	V
V_{CMR}	Common mode input voltage ^(1,2)			GND + 0.5		$V_{DD} - 0.85$	

Notes:

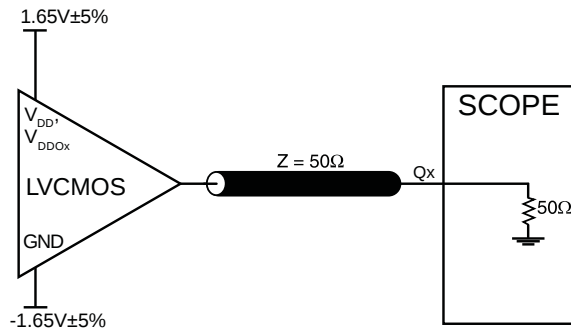
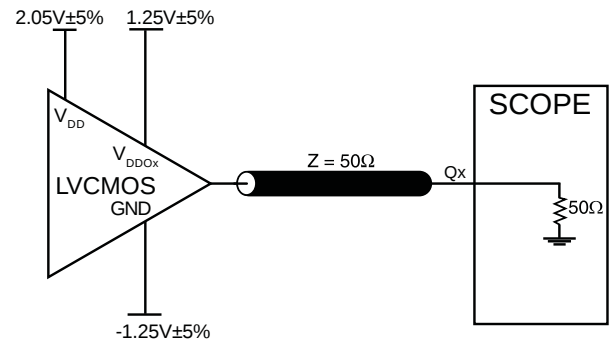
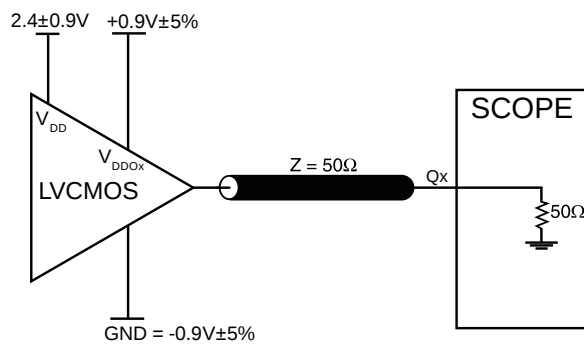
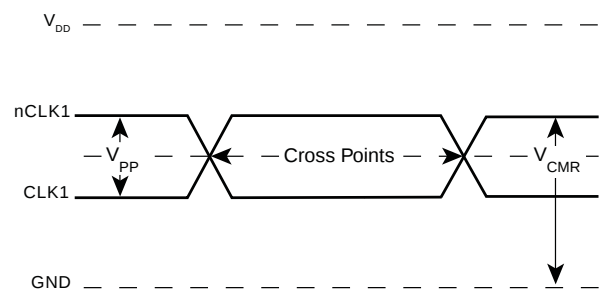
1. For single ended application, the maximum input voltage for CLK1, nCLK1 is $V_{DD} + 0.3V$.
2. Common mode voltage is defined as V_{IH} .

AC Characteristics, ($V_{DD} = 3.3V \pm 5\%$, $V_{DDOX} = 1.8V \pm 5\%$ to $3.3V \pm 5\%$, $T_A = -40^\circ$ to $+85^\circ C$)⁽⁷⁾

Symbol	Parameter		Test Conditions	Min.	Typ.	Max.	Units
f_{MAX}	Output Frequency					250	MHz
T_{PLH}	Propagation Delay, Low to High	CLK0 ⁽¹⁾	$V_{DDOX} = 3.3V$	2.3	3.4	3.9	ns
		CLK1, nCLK1 ⁽²⁾		2.5	3.4	3.9	
		CLK0 ⁽¹⁾	$V_{DDOX} = 2.5V$	2.3	3.5	4.0	
		CLK1, nCLK1 ⁽²⁾		2.5	3.5	4.0	
		CLK0 ⁽¹⁾	$V_{DDOX} = 1.8V$	2.4	3.9	4.7	
		CLK1, nCLK1 ⁽²⁾		2.6	3.9	4.7	
tsk(b)	Bank skew ⁽³⁾		Measured on the rising edge			30	ps
tsk(o)	Output skew ⁽⁴⁾		Measured on the rising edge			170	
tsk(pp)	Part-to-Part skew ⁽⁵⁾					750	
t_R/t_F	Output Rise/Fall Time ⁽⁵⁾		20% to 80%	200		700	
odc	Output duty cycle			40		60	%
t_{EN}	Output enable time ⁽⁶⁾					10	ns
t_{DIS}	Output Disable Time ⁽⁶⁾					10	

Notes:

1. Measured from the $V_{DD}/2$ of the input to $V_{DDOX}/2$ of the output
2. Measured from the differential input crossing point to $V_{DDOX}/2$ of the output
3. Defined as a skew within a bandwidth equal load conditions
4. Defined as a skew between outputs at the same supply voltage, same frequency, and with equal load conditions. Measured at $V_{DDOX}/2$
5. Defined as a skew between outputs on a different devices operation at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDOX}/2$.
6. These parameters are guaranteed by characterization. Not tested in production.
7. All parameters are measured at 250MHz with SEL [A:D] = 1 unless noted otherwise.

Parameter Measurement Information

3.3V Core/3.3V Output Load AC Test Circuit

3.3V Core/2.5V Output Load AC Circuit

3.3V Core/1.8V Output Load AC Test Circuit

Differential Input Level

Application Information

Wiring the differential input to accept single ended levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{DD}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{DD} = 3.3V$, V_{REF} should be 1.25V and $R1/R2 = 0.609$.

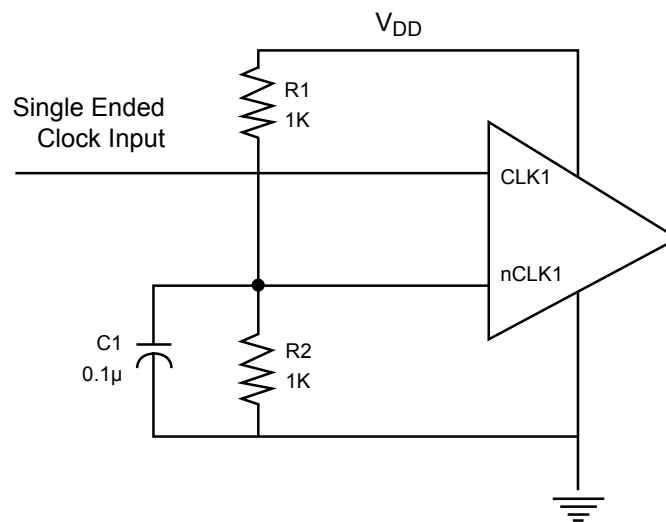
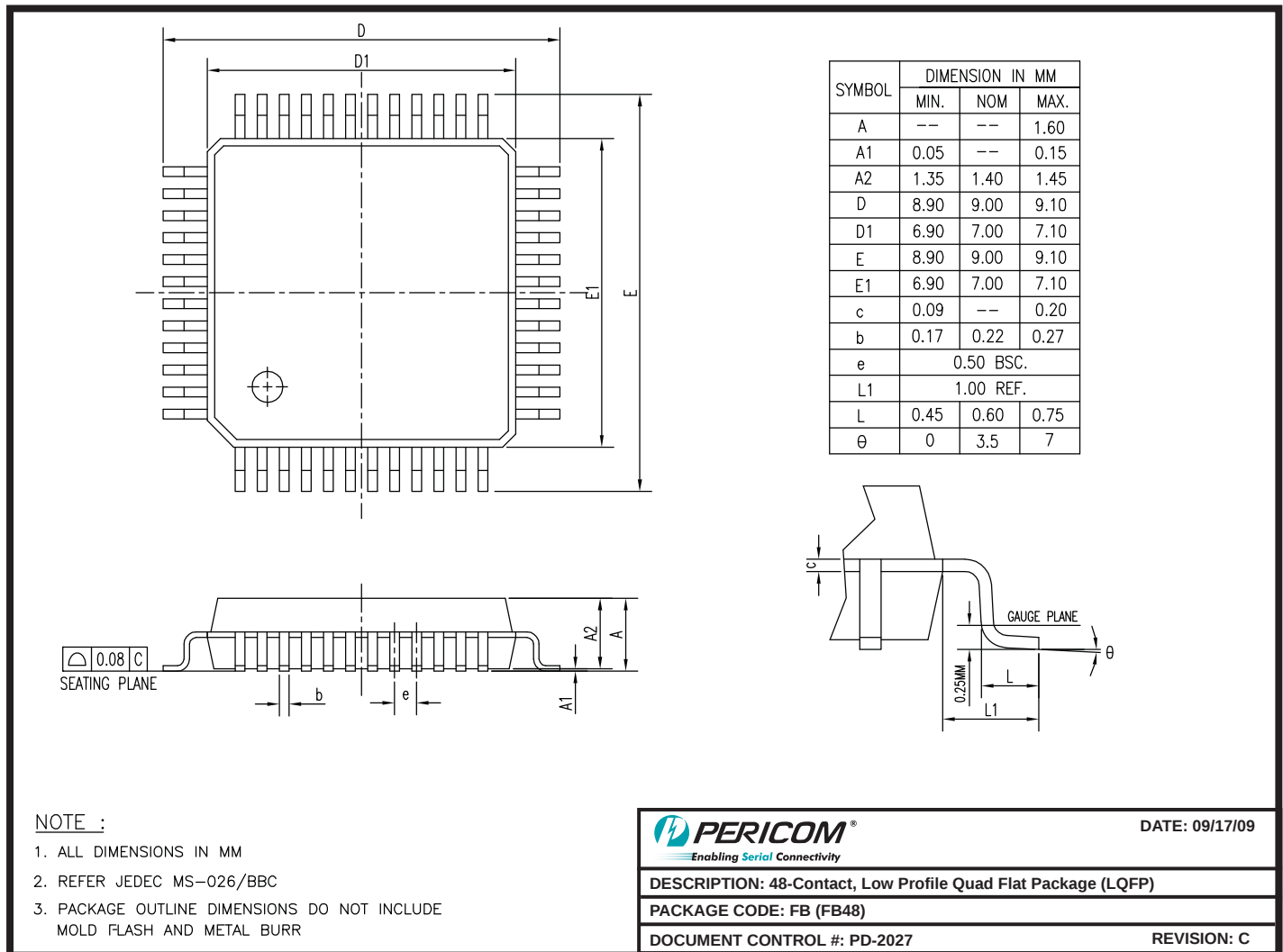


Figure 1: Single-ended Signal Driving Differential Input

Package Mechanical: 48-pin LQFP (FB)


09-0012

Note:

- For latest package info, please check: <http://www.pericom.com/products/packaging/mechanicals.php>

Ordering Information

Ordering Code	Package Code	Package Type
PI6C487016FBE	FB	Pb-free & Green, 48-pin LQFP

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- Adding an X suffix = Tape/Reel