

- Member of the Texas Instruments Widebus+™ Family
- Pinout Optimizes DDR2 DIMM PCB Layout
- Configurable as 25-Bit 1:1 or 14-Bit 1:2 Registered Buffer
- Chip-Select Inputs Gate the Data Outputs from Changing State and Minimizes System Power Consumption
- Output Edge-Control Circuitry Minimizes Switching Noise in an Unterminated Line
- Supports SSTL\_18 Data Inputs
- Differential Clock (CLK and CLK) Inputs
- Supports LVCMOS Switching Levels on the Control and RESET Inputs
- Checks Parity on DIMM-Independent Data Inputs
- Able to Cascade with a Second SN74SSTU32866
- RESET Input Disables Differential Input Receivers, Resets All Registers, and Forces All Outputs Low, Except QERR
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

#### description/ordering information

This 25-bit 1:1 or 14-bit 1:2 configurable registered buffer is designed for 1.7-V to 1.9-V  $V_{CC}$  operation. In the 1:1 pinout configuration, only one device per DIMM is required to drive nine SDRAM loads. In the 1:2 pinout configuration, two devices per DIMM are required to drive 18 SDRAM loads.

All inputs are SSTL\_18, except the reset (RESET) and control (Cn) inputs, which are LVCMOS. All outputs are edge-controlled circuits optimized for unterminated DIMM loads and meet SSTL\_18 specifications, except the open-drain error (QERR) output.

The SN74SSTU32866 operates from a differential clock (CLK and CLK). Data are registered at the crossing of CLK going high and CLK going low.

The SN74SSTU32866 accepts a parity bit from the memory controller on the parity bit (PAR\_IN) input, compares it with the data received on the DIMM-independent D-inputs (D2–D3, D5–D6, D8–D25 when C0 = 0 and C1 = 0; D2–D3, D5–D6, D8–D14 when C0 = 0 and C1=1; or D1–D6, D8–D13 when C0 = 1 and C1=1) and indicates whether a parity error has occurred on the open-drain QERR pin (active low). The convention is even parity; i.e., valid parity is defined as an even number of ones across the DIMM-independent data inputs, combined with the parity input bit. To calculate parity, all DIMM-independent data inputs must be tied to a known logic state.

When used as a single device, the C0 and C1 inputs are tied low. In this configuration, parity is checked on the PAR\_IN input signal, which arrives one cycle after the input data to which it applies. Two clock cycles after the data are registered, the corresponding partial-parity-out (PPO) and QERR signals are generated.

#### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	LFBGA – GKE	Tape and reel	SN74SSTU32866GKER	SU866

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**description/ordering information (continued)**

When used in pairs, the C0 input of the first register is tied low, and the C0 input of the second register is tied high. The C1 input of both registers are tied high. Parity, which arrives one cycle after the data input to which it applies, is checked on the PAR\_IN input signal of the first device. Two clock cycles after the data are registered, the corresponding PPO and QERR signals are generated on the second device. The PPO output of the first register is cascaded to the PAR\_IN of the second SN74SSTU32866. The QERR output of the first SN74SSTU32866 is left floating, and the valid error information is latched on the QERR output of the second SN74SSTU32866.

If an error occurs and the QERR output is driven low, it stays latched low for a minimum of two clock cycles or until RESET is driven low. If two or more consecutive parity errors occur, the QERR output is driven low and latched low for a clock duration equal to the parity-error duration or until RESET is driven low. The DIMM-dependent signals (DCKE, DCS, DODT, and CSR) are not included in the parity-check computation.

The C0 input controls the pinout configuration of the 1:2 pinout from register-A configuration (when low) to register-B configuration (when high). The C1 input controls the pinout configuration from 25-bit 1:1 (when low) to 14-bit 1:2 (when high). C0 and C1 should not be switched during normal operation. They should be hard-wired to a valid low or high level to configure the register in the desired mode. In the 25-bit 1:1 pinout configuration, the A6, D6, and H6 terminals are driven low and are do-not-use (DNU) pins.

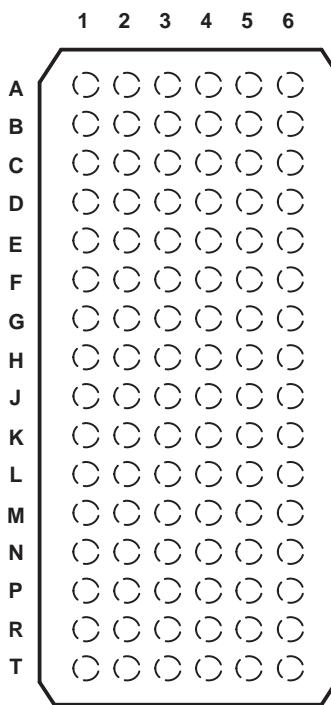
In the DDR2 RDIMM application, RESET is specified to be completely asynchronous with respect to CLK and CLK. Therefore, no timing relationship can be ensured between the two. When entering reset, the register is cleared, and the data outputs are driven low quickly, relative to the time required to disable the differential input receivers. However, when coming out of reset, the register becomes active quickly, relative to the time required to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of RESET until the input receivers are fully enabled, the design of the SN74SSTU32866 ensures that the outputs remain low, thus ensuring there will be no glitches on the output.

To ensure defined outputs from the register before a stable clock has been supplied, RESET must be held in the low state during power up.

The device supports low-power standby operation. When RESET is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage (V<sub>REF</sub>) inputs are allowed. In addition, when RESET is low, all registers are reset and all outputs are forced low, except QERR. The LVCMS RESET and C<sub>n</sub> inputs always must be held at a valid logic high or low level.

The device also supports low-power active operation by monitoring both system chip select (DCS and CSR) inputs and gates the Q<sub>n</sub> and PPO outputs from changing states when both DCS and CSR inputs are high. If either DCS or CSR input is low, the Q<sub>n</sub> and PPO outputs function normally. Also, if the internal low-power signal (LPS1) is high (one cycle after DCS and CSR go high), the device gates the QERR output from changing states. If LPS1 is low, the QERR output functions normally. The RESET input has priority over the DCS and CSR control and, when driven low, forces the Q<sub>n</sub> and PPO outputs low and forces the QERR output high. If the DCS control functionality is not desired, the CSR input can be hard-wired to ground, in which case the setup-time requirement for DCS is the same as for the other D data inputs. To control the low-power mode with DCS only, the CSR input should be pulled up to V<sub>CC</sub> through a pullup resistor.

The two V<sub>REF</sub> pins (A3 and T3) are connected together internally by approximately 150 Ω. However, it is necessary to connect only one of the two V<sub>REF</sub> pins to the external V<sub>REF</sub> power supply. An unused V<sub>REF</sub> pin should be terminated with a V<sub>REF</sub> coupling capacitor.

GKE PACKAGE  
(TOP VIEW)

## terminal assignments for 1:1 register (C0 = 0, C1 = 0)

	1	2	3	4	5	6
A	D1 (DCKE)	PPO	V <sub>REF</sub>	V <sub>CC</sub>	Q1 (QCKE)	DNU
B	D2	D15	GND	GND	Q2	Q15
C	D3	D16	V <sub>CC</sub>	V <sub>CC</sub>	Q3	Q16
D	D4 (DODT)	<u>QERR</u>	GND	GND	Q4 (QODT)	DNU
E	D5	D17	V <sub>CC</sub>	V <sub>CC</sub>	Q5	Q17
F	D6	D18	GND	GND	Q6	Q18
G	PAR_IN	<u>RESET</u>	V <sub>CC</sub>	V <sub>CC</sub>	C1	C0
H	CLK	D7 ( <u>DCS</u> )	GND	GND	Q7 ( <u>QCS</u> )	DNU
J	<u>CLK</u>	<u>CSR</u>	V <sub>CC</sub>	V <sub>CC</sub>	NC	NC
K	D8	D19	GND	GND	Q8	Q19
L	D9	D20	V <sub>CC</sub>	V <sub>CC</sub>	Q9	Q20
M	D10	D21	GND	GND	Q10	Q21
N	D11	D22	V <sub>CC</sub>	V <sub>CC</sub>	Q11	Q22
P	D12	D23	GND	GND	Q12	Q23
R	D13	D24	V <sub>CC</sub>	V <sub>CC</sub>	Q13	Q24
T	D14	D25	V <sub>REF</sub>	V <sub>CC</sub>	Q14	Q25

Each pin name in parentheses indicates the DDR2 DIMM signal name.

DNU – Do not use

NC – No internal connection

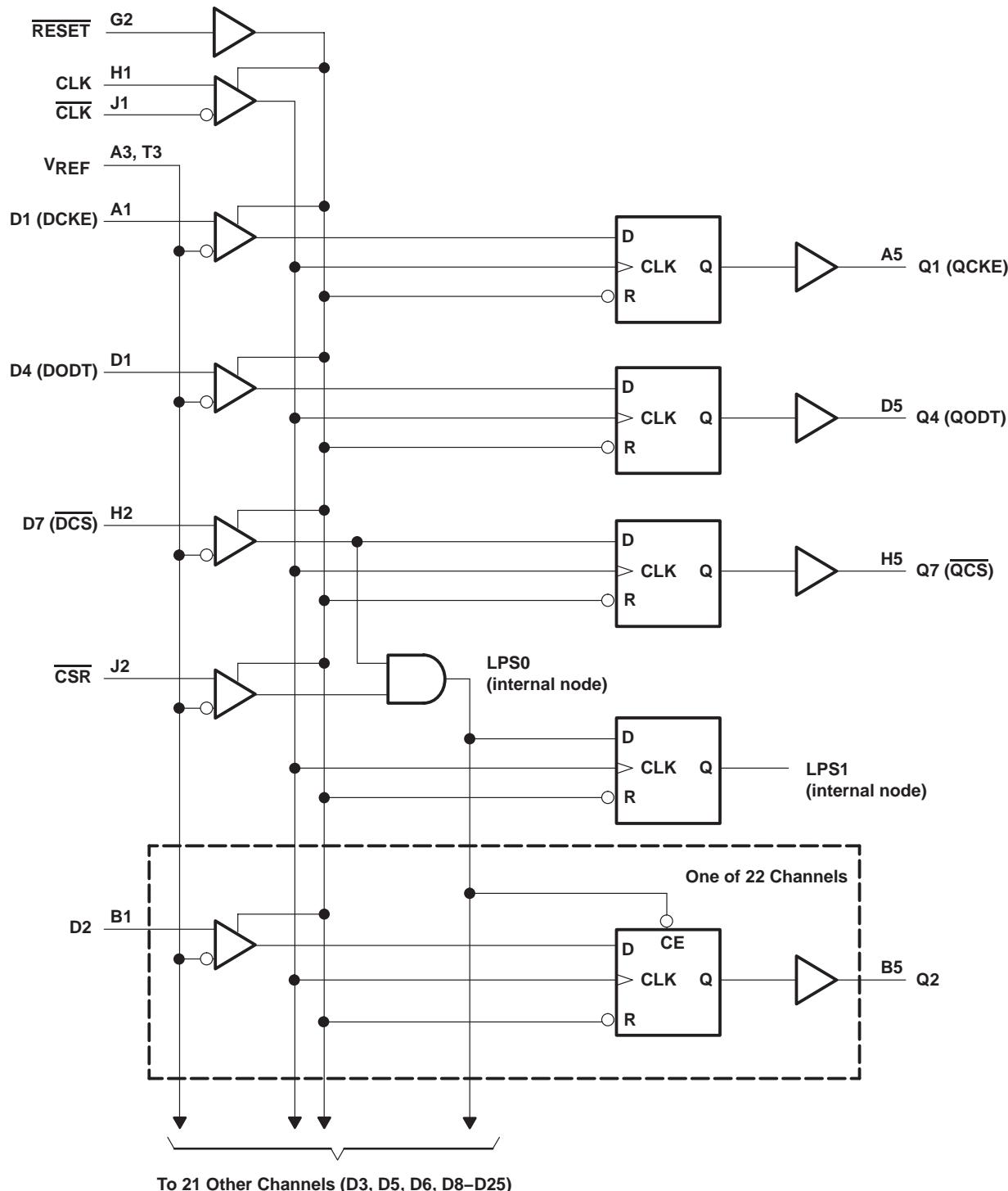
# SN74SSTU32866

## 25-BIT CONFIGURABLE REGISTERED BUFFER

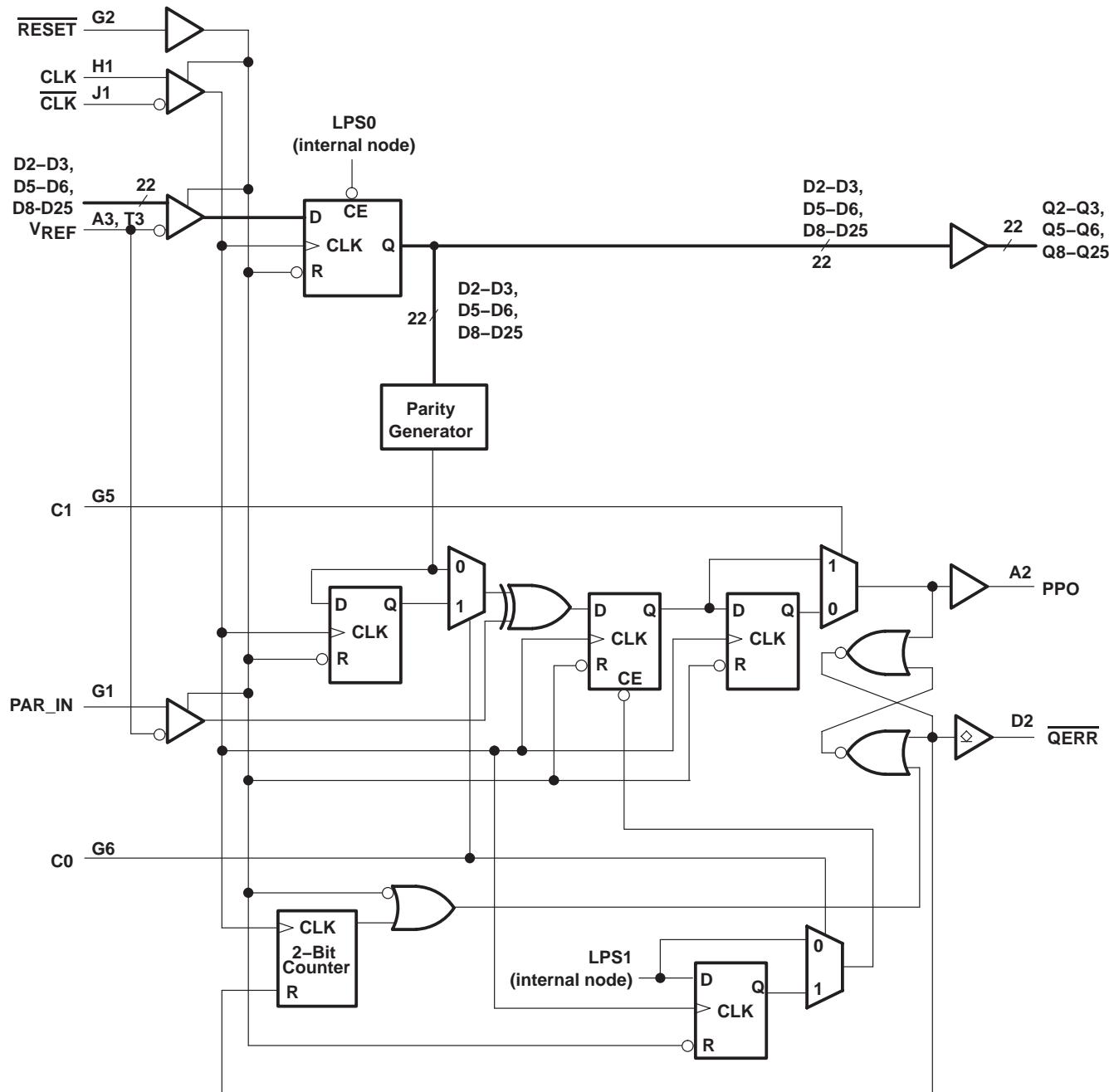
### WITH ADDRESS-PARITY TEST

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logic diagram for 1:1 register configuration (positive logic); C0 = 0, C1 = 0

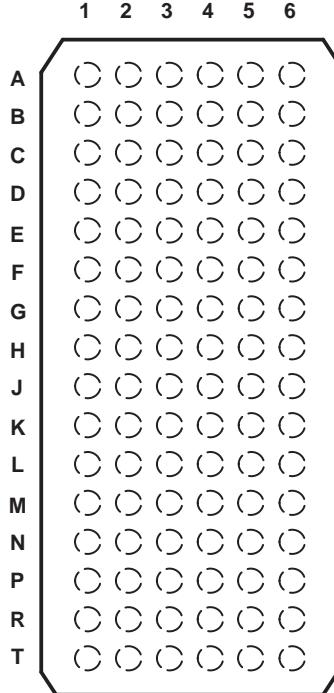


parity logic diagram for 1:1 register configuration (positive logic);  $C0 = 0$ ,  $C1 = 0$



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**GKE PACKAGE  
(TOP VIEW)****terminal assignments for 1:2 register-A (C0 = 0, C1 = 1)**

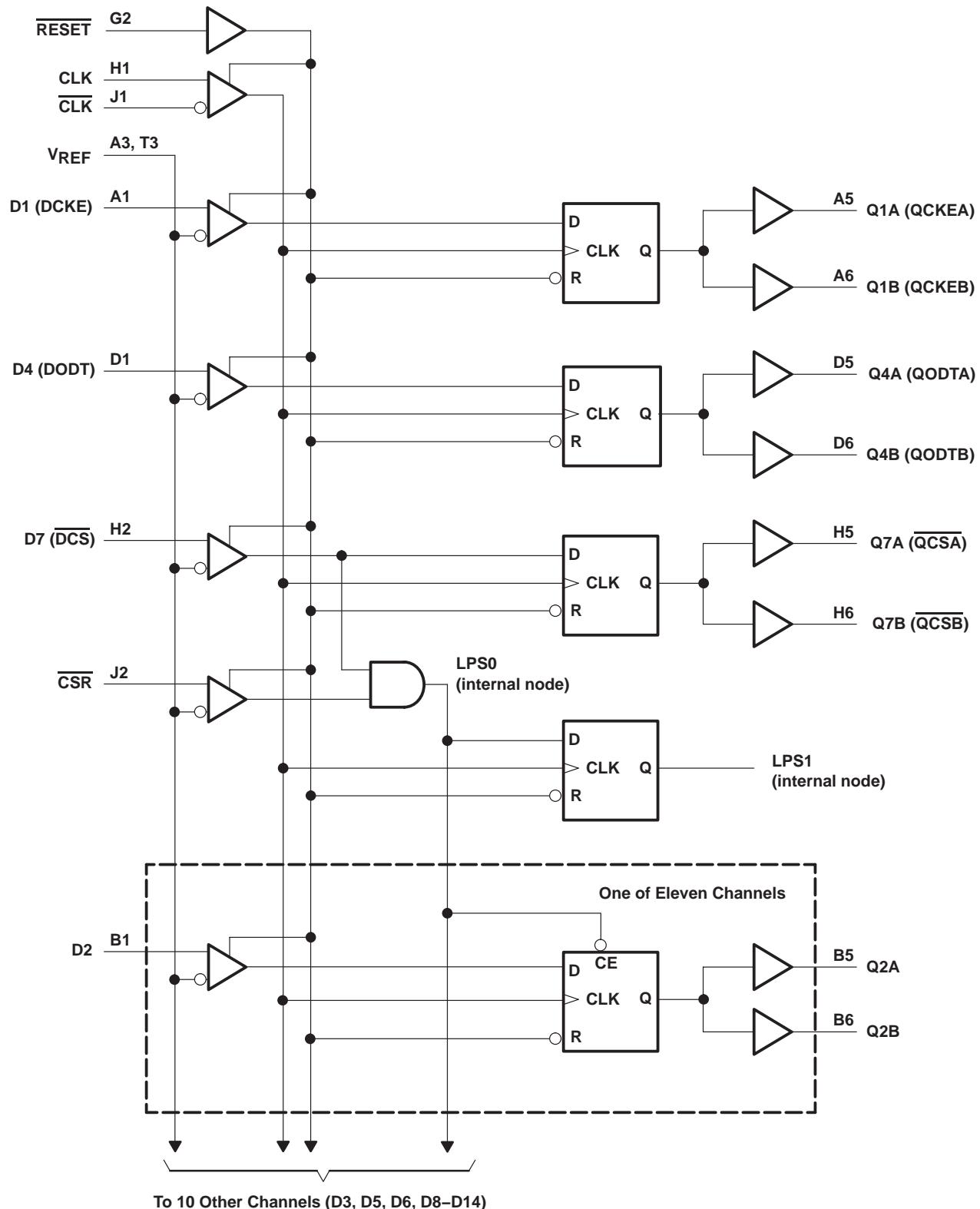
	1	2	3	4	5	6
A	D1 (DCKE)	PPO	V <sub>REF</sub>	V <sub>CC</sub>	Q1A (QCKEA)	Q1B (QCKEB)
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	V <sub>CC</sub>	V <sub>CC</sub>	Q3A	Q3B
D	D4 (DODT)	<u>QERR</u>	GND	GND	Q4A (QODTA)	Q4B (QODTB)
E	D5	DNU	V <sub>CC</sub>	V <sub>CC</sub>	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	PAR_IN	<u>RESET</u>	V <sub>CC</sub>	V <sub>CC</sub>	C1	C0
H	CLK	D7 ( <u>DCS</u> )	GND	GND	<u>Q7A</u> (QCSA)	<u>Q7B</u> (QCSB)
J	CLK	<u>CSR</u>	V <sub>CC</sub>	V <sub>CC</sub>	NC	NC
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V <sub>CC</sub>	V <sub>CC</sub>	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	D11	DNU	V <sub>CC</sub>	V <sub>CC</sub>	Q11A	Q11B
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V <sub>CC</sub>	V <sub>CC</sub>	Q13A	Q13B
T	D14	DNU	V <sub>REF</sub>	V <sub>CC</sub>	Q14A	Q14B

Each pin name in parentheses indicates the DDR2 DIMM signal name.

DNU – Do not use

NC – No internal connection

logic diagram for 1:2 register-A configuration (positive logic); C0 = 0, C1 = 1

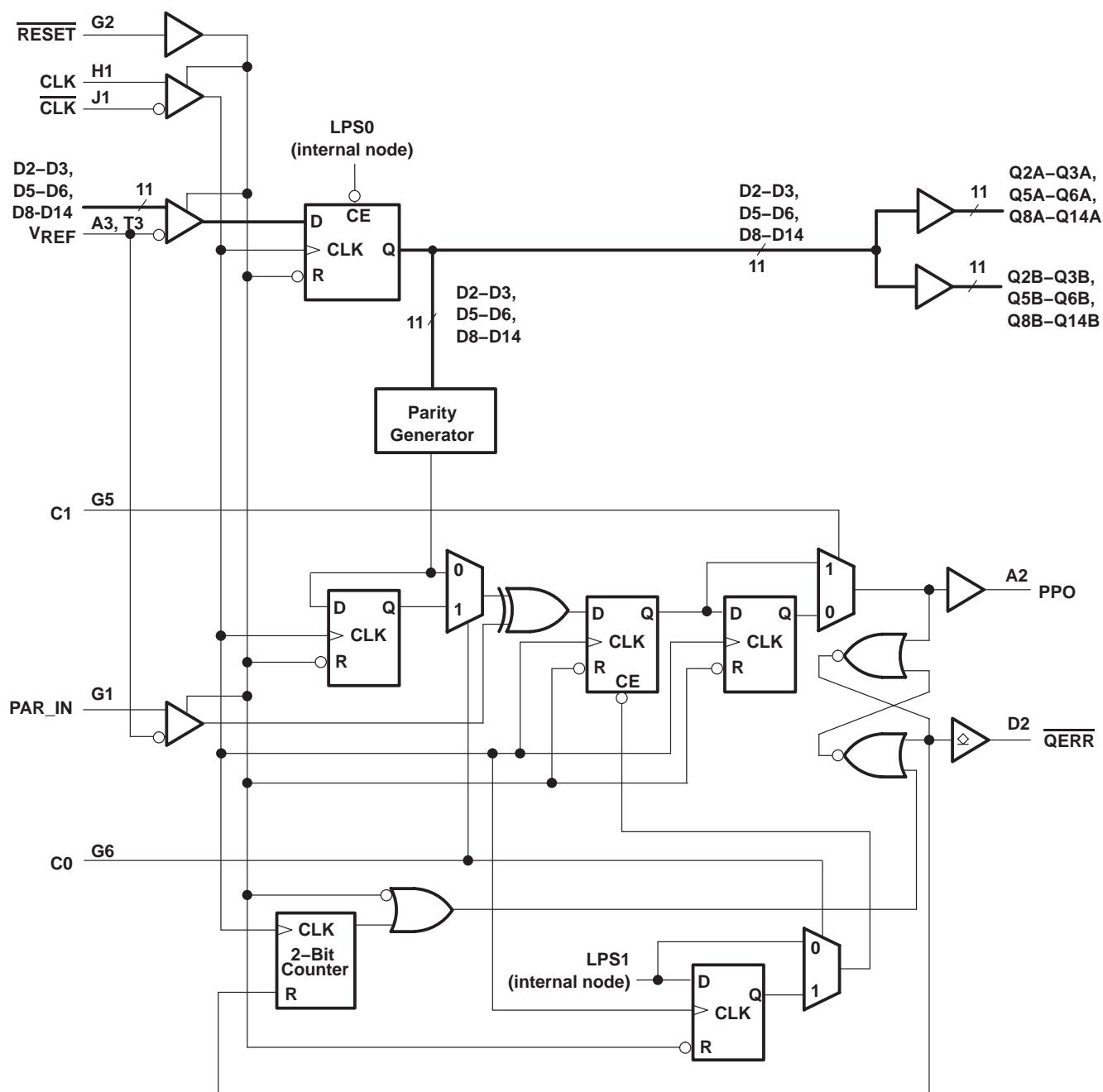


**SN74SSTU32866**

## 25-BIT CONFIGURABLE REGISTERED BUFFER

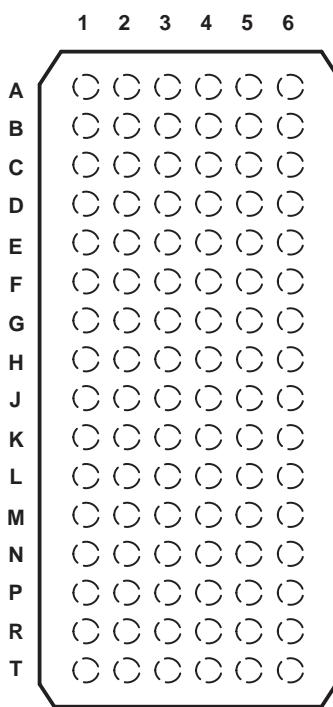
WITH ADDRESS-PARITY TEST

### parity logic diagram for 1:2 register-A configuration (positive logic): C0 = 0, C1 = 1



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**25-BIT CONFIGURABLE REGISTERED BUFFER  
 WITH ADDRESS-PARITY TEST**  
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**GKE PACKAGE  
 (TOP VIEW)**



**terminal assignments for 1:2 register-B (C0 = 1, C1 = 1)**

	1	2	3	4	5	6
A	D1	PPO	V <sub>REF</sub>	V <sub>CC</sub>	Q1A	Q1B
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	V <sub>CC</sub>	V <sub>CC</sub>	Q3A	Q3B
D	D4	<u>QERR</u>	GND	GND	Q4A	Q4B
E	D5	DNU	V <sub>CC</sub>	V <sub>CC</sub>	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	PAR_IN	<u>RESET</u>	V <sub>CC</sub>	V <sub>CC</sub>	C1	C0
H	CLK	D7 ( <u>DCS</u> )	GND	GND	<u>Q7A</u> (QCSA)	<u>Q7B</u> (QCSB)
J	<u>CLK</u>	<u>CSR</u>	V <sub>CC</sub>	V <sub>CC</sub>	NC	NC
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V <sub>CC</sub>	V <sub>CC</sub>	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	D11 (DODT)	DNU	V <sub>CC</sub>	V <sub>CC</sub>	Q11A (QODTA)	Q11B (QODTB)
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V <sub>CC</sub>	V <sub>CC</sub>	Q13A	Q13B
T	D14 (DCKE)	DNU	V <sub>REF</sub>	V <sub>CC</sub>	Q14A (QCKEA)	Q14B (QCKEB)

Each pin name in parentheses indicates the DDR2 DIMM signal name.

DNU – Do not use

NC – No internal connection

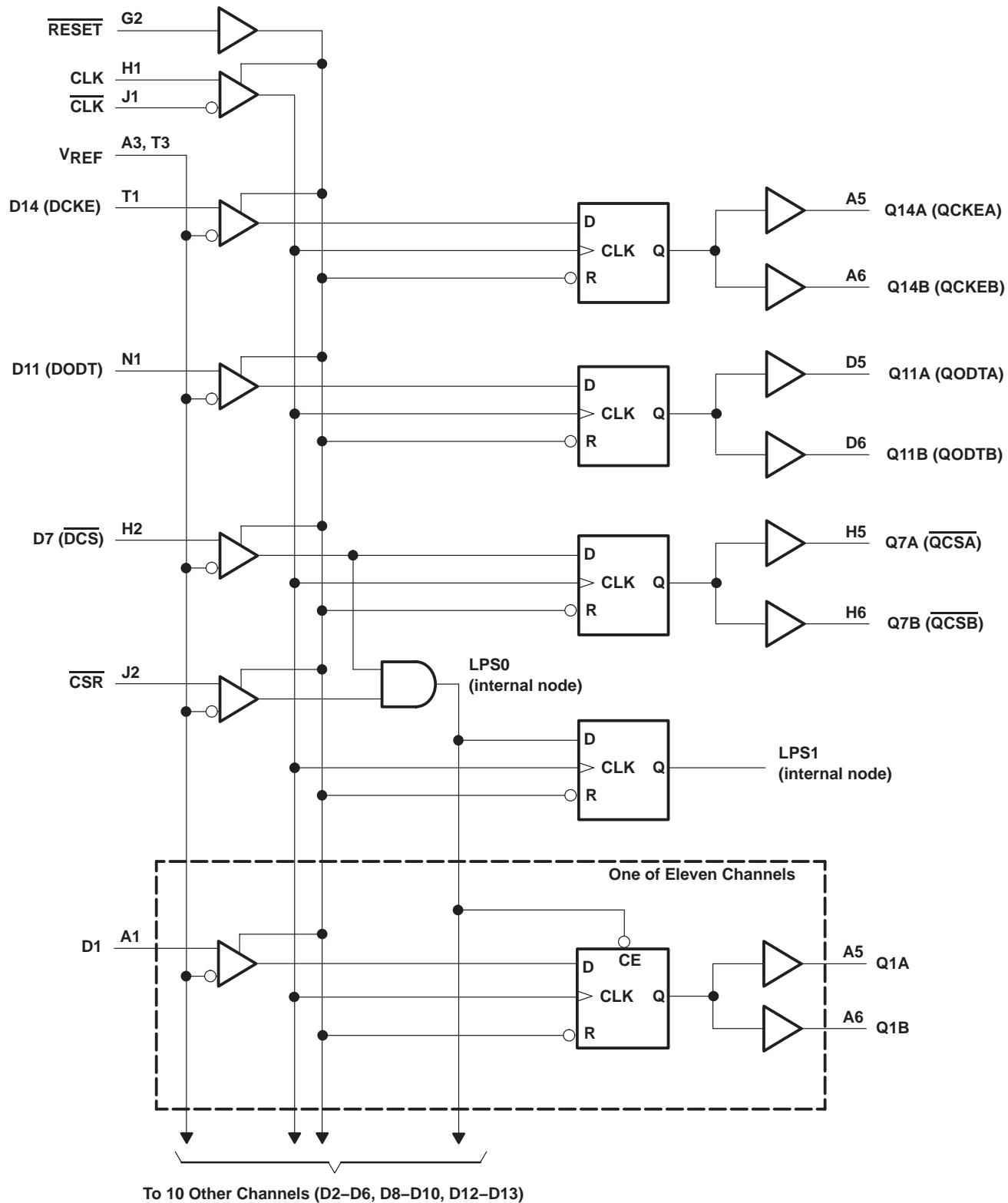
# SN74SSTU32866

## 25-BIT CONFIGURABLE REGISTERED BUFFER

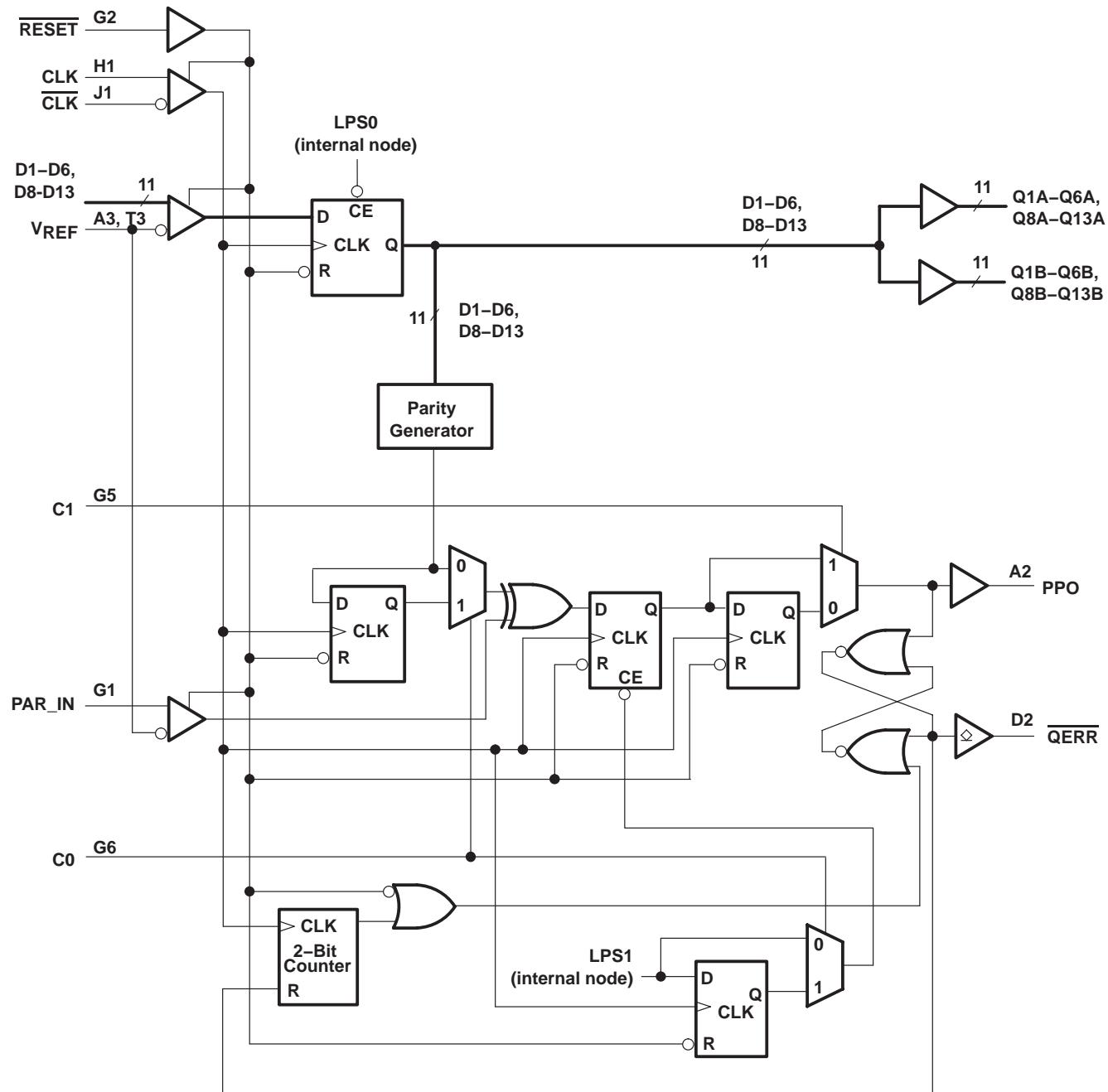
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logic diagram for 1:2 register-B configuration (positive logic); C0 = 1, C1 = 1



parity logic diagram for 1:2 register-B configuration (positive logic); C0 = 1, C1 = 1



**SN74SSTU32866****25-BIT CONFIGURABLE REGISTERED BUFFER  
WITH ADDRESS-PARITY TEST**

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**TERMINAL FUNCTIONS**

TERMINAL NAME	DESCRIPTION	ELECTRICAL CHARACTERISTICS
GND	Ground	Ground input
V <sub>CC</sub>	Power-supply voltage	1.8 V nominal
V <sub>REF</sub>	Input reference voltage	0.9 V nominal
CLK	Positive master clock input	Differential input
$\overline{\text{CLK}}$	Negative master clock input	Differential input
C0, C1	Configuration control input. Register A or Register B and 1:1 mode or 1:2 mode select.	LVCMS input
<u>RESET</u>	Asynchronous reset input. Resets registers and disables V <sub>REF</sub> , data, and clock differential-input receivers. When <u>RESET</u> is low, all Q outputs are forced low and the <u>QERR</u> output is forced high.	LVCMS input
D1–D25	Data input. Clocked in on the crossing of the rising edge of CLK and the falling edge of $\overline{\text{CLK}}$ .	SSTL_18 inputs
<u>CSR</u> , <u>DCS</u>	Chip select inputs. Disables D1–D25 <sup>†</sup> outputs switching when both inputs are high	SSTL_18 inputs
DODT	The outputs of this register bit will not be suspended by the <u>DCS</u> and <u>CSR</u> control.	SSTL_18 input
DCKE	The outputs of this register bit will not be suspended by the <u>DCS</u> and <u>CSR</u> control.	SSTL_18 input
PAR_IN	Parity input. Arrives one clock cycle after the corresponding data input.	SSTL_18 input
Q1–Q25 <sup>‡</sup>	Data outputs that are suspended by the <u>DCS</u> and <u>CSR</u> control.	1.8 V CMOS outputs
PPO	Partial parity out. Indicates odd parity of inputs D1–D25. <sup>†</sup>	1.8 V CMOS output
QCS	Data output that will not be suspended by the <u>DCS</u> and <u>CSR</u> control	1.8 V CMOS output
QODT	Data output that will not be suspended by the <u>DCS</u> and <u>CSR</u> control	1.8 V CMOS output
QCKE	Data output that will not be suspended by the <u>DCS</u> and <u>CSR</u> control	1.8 V CMOS output
<u>QERR</u>	Output error bit. Timing is determined by the device mode.	Open-drain output
NC	No internal connection	
DNU	Do not use. Inputs are in standby-equivalent mode, and outputs are driven low.	

<sup>†</sup> Data inputs = D2, D3, D5, D6, D8–D25 when C0 = 0 and C1 = 0

Data inputs = D2, D3, D5, D6, D8–D14 when C0 = 0 and C1 = 1

Data inputs = D1–D6, D8–D10, D12, D13 when C0 = 1 and C1 = 1.

<sup>‡</sup> Data outputs = Q2, Q3, Q5, Q6, Q8–Q25 when C0 = 0 and C1 = 0

Data outputs = Q2, Q3, Q5, Q6, Q8–Q14 when C0 = 0 and C1 = 1

Data outputs = Q1–Q6, Q8–Q10, Q12, Q13 when C0 = 1 and C1 = 1.

**FUNCTION TABLES**

INPUTS						OUTPUTS
RESET	DCS	<u>CSR</u>	CLK	$\overline{\text{CLK}}$	D <sub>n</sub>	Q <sub>n</sub>
H	L	X	↑	↓	L	L
H	L	X	↑	↓	H	H
H	X	L	↑	↓	L	L
H	X	L	↑	↓	H	H
H	H	H	↑	↓	X	Q <sub>0</sub>
H	X	X	L or H	L or H	X	Q <sub>0</sub>
L	X or floating	X or floating	X or floating	X or floating	X or floating	L

**Function Tables (Continued)**

INPUTS				OUTPUTS
RESET	CLK	$\overline{\text{CLK}}$	$\overline{\text{DCS}}$ , $\overline{\text{DODT}}$	$\overline{\text{QCKE}}$ , $\overline{\text{QCS}}$ , $\overline{\text{QDT}}$
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	$Q_0$
L	X or floating	X or floating	X or floating	L

**PARITY AND STANDBY FUNCTION**

INPUTS							OUTPUTS	
RESET	CLK	$\overline{\text{CLK}}$	$\overline{\text{DCS}}$	$\overline{\text{CSR}}$	$\Sigma \text{ OF INPUTS} = \text{H}$ $\text{D1-D25}^{\dagger}$	PAR_IN $^{\ddagger}$	PPO	$\overline{\text{QERR}}^{\$}$
H	↑	↓	L	X	Even	L	L	H
H	↑	↓	L	X	Odd	L	H	L
H	↑	↓	L	X	Even	H	H	L
H	↑	↓	L	X	Odd	H	L	H
H	↑	↓	H	L	Even	L	L	H
H	↑	↓	H	L	Odd	L	H	L
H	↑	↓	H	L	Even	H	H	L
H	↑	↓	H	L	Odd	H	L	H
H	↑	↓	H	H	X	X	PPO <sub>0</sub>	$\overline{\text{QERR}}_0$
H	L or H	L or H	X	X	X	X	PPO <sub>0</sub>	$\overline{\text{QERR}}_0$
L	X or floating	X or floating	X or floating	X or floating	X	X or floating	L	H

<sup>†</sup> Data inputs = D2–D3, D5–D6, D8–D25 when C0 = 0 and C1 = 0

Data inputs = D2–D3, D5–D6, D8–D14 when C0 = 0 and C1 = 1

Data inputs = D1–D6, D8–D13 when C0 = 1 and C1 = 1

<sup>‡</sup> PAR\_IN arrives one clock cycle (C0 = 0) or two clock cycles (C0 = 1) after the data to which it applies.

<sup>§</sup> This transition assumes that QERR is high at the crossing of CLK going high and  $\overline{\text{CLK}}$  going low. If QERR goes low, it stays latched low for a minimum of two clock cycles or until RESET is driven low. If two or more consecutive parity errors occur, the QERR output is driven low and latched low for a clock duration equal to the parity duration or until RESET is driven low.

**PARITY ERROR DETECT IN LOW-POWER MODE<sup>¶</sup>**

ERROR POSITION	1:1 MODE (C0 = 0, C1 = 0)		1:2 REGISTER-A MODE (C0 = 0, C1 = 1)		1:2 REGISTER-B MODE (C0 = 0, C1 = 0)		CASCADED MODE (Registers A and B)	
	PPO DURATION	QERR DURATION	PPO DURATION	QERR DURATION	PPO DURATION	QERR DURATION	PPO DURATION	QERR DURATION
n – 4	1 Cycle	2 Cycles	1 Cycle	2 Cycles	1 Cycle	2 Cycles	1 Cycle	2 Cycles
n – 3	1 Cycle	2 Cycles	1 Cycle	2 Cycles	1 Cycle	2 Cycles	1 Cycle	2 Cycles
n – 2	1 Cycle	2 Cycles	1 Cycle	2 Cycles	1 Cycle	2 Cycles	1 Cycle	2 Cycles
n – 1	LPM + 2	LPM + 2	LPM + 1	LPM + 1	LPM + 2	LPM + 2	LPM + 2	LPM + 2
n	Not detected	Not detected	Not detected	Not detected	Not detected	Not detected	Not detected	Not detected

<sup>¶</sup> If a parity error occurs before the device enters the low-power mode (LPM), the behavior of PPO and QERR is dependent on the mode of the device and the position of the parity error occurrence. This table illustrates the low-power-mode effect on parity detect. The low-power mode is activated on the n clock cycle when DCS and CSR go high.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$ .....	–0.5 V to 2.5 V
Input voltage range, $V_I$ (see Notes 1 and 2) .....	–0.5 V to 2.5 V
Output voltage range, $V_O$ (see Notes 1 and 2) .....	–0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	±50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	±50 mA
Continuous current through each $V_{CC}$ or GND .....	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3) .....	36°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. This value is limited to 2.5 V maximum.  
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 4)

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	1.7	1.9		V
$V_{REF}$	Reference voltage	$0.49 \times V_{CC}$	$0.5 \times V_{CC}$	$0.51 \times V_{CC}$	V
$V_{TT}$	Termination voltage	$V_{REF} - 40$ mV	$V_{REF}$	$V_{REF} + 40$ mV	V
$V_I$	Input voltage	0		$V_{CC}$	V
$V_{IH}$	AC high-level input voltage	Data inputs, $\overline{CSR}$ , $\overline{PAR\_IN}$	$V_{REF} + 250$ mV		V
$V_{IL}$	AC low-level input voltage	Data inputs, $\overline{CSR}$ , $\overline{PAR\_IN}$		$V_{REF} - 250$ mV	V
$V_{IH}$	DC high-level input voltage	Data inputs, $\overline{CSR}$ , $\overline{PAR\_IN}$	$V_{REF} + 125$ mV		V
$V_{IL}$	DC low-level input voltage	Data inputs, $\overline{CSR}$ , $\overline{PAR\_IN}$		$V_{REF} - 125$ mV	V
$V_{IH}$	High-level input voltage	$\overline{RESET}$ , $C_n$	$0.65 \times V_{CC}$		V
$V_{IL}$	Low-level input voltage	$\overline{RESET}$ , $C_n$		$0.35 \times V_{CC}$	V
$V_{ICR}$	Common-mode input voltage range	$\overline{CLK}$ , $\overline{CLK}$	0.675	1.125	V
$V_{I(PP)}$	Peak-to-peak input voltage	$\overline{CLK}$ , $\overline{CLK}$	600		mV
$I_{OH}$	High-level output current	Q outputs, $\overline{PPO}$		–8	mA
$I_{OL}$	Low-level output current	Q outputs, $\overline{PPO}$		8	mA
		$\overline{QERR}$ output		8	
$T_A$	Operating free-air temperature	0	70		°C

NOTE 4: The  $\overline{RESET}$  and  $C_n$  inputs of the device must be held at valid logic voltage levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless  $\overline{RESET}$  is low. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP†	MAX	UNIT	
V <sub>OH</sub>	Q outputs, PPO	I <sub>OH</sub> = -100 $\mu$ A	1.7 V to 1.9 V	V <sub>CC</sub> -0.2		1.3	V	
		I <sub>OH</sub> = -6 mA	1.7 V					
V <sub>OL</sub>	Q outputs, PPO	I <sub>OL</sub> = 100 $\mu$ A	1.7 V to 1.9 V	0.2		0.4	V	
		I <sub>OL</sub> = 6 mA	1.7 V					
	QERR output	I <sub>OL</sub> = 8 mA	1.7 V	0.35				
I <sub>I</sub>	All inputs‡	V <sub>I</sub> = V <sub>CC</sub> or GND	1.9 V	±5		μA		
I <sub>OZ</sub>	QERR output	V <sub>O</sub> = V <sub>CC</sub> or GND	1.9 V	±10		μA		
I <sub>CC</sub>	Static standby	RESET = GND	I <sub>O</sub> = 0	1.9 V	100		μA	
	Static operating	RESET = V <sub>CC</sub> , V <sub>I</sub> = V <sub>IH(AC)</sub> or V <sub>IL(AC)</sub>			50		mA	
I <sub>CCD</sub>	Dynamic operating – clock only	RESET = V <sub>CC</sub> , V <sub>I</sub> = V <sub>IH(AC)</sub> or V <sub>IL(AC)</sub> , CLK and CLK switching 50% duty cycle	I <sub>O</sub> = 0	1.8 V	42		μA/ MHz	
	Dynamic operating – per each data input, 1:1 configuration	RESET = V <sub>CC</sub> , V <sub>I</sub> = V <sub>IH(AC)</sub> or V <sub>IL(AC)</sub> , CLK and CLK switching 50% duty cycle, one data input switching at one-half clock frequency, 50% duty cycle			18		μA/ clock MHz/ D input	
	Dynamic operating – per each data input, 1:2 configuration				35			
I <sub>CCDLP</sub>	Chip-select-enabled low-power active mode – clock only	RESET = V <sub>CC</sub> , V <sub>I</sub> = V <sub>IH(AC)</sub> or V <sub>IL(AC)</sub> , CLK and CLK switching 50% duty cycle	I <sub>O</sub> = 0	1.8 V	42		μA/ MHz	
	Chip-select-enabled low-power active mode – 1:1 configuration	RESET = V <sub>CC</sub> , V <sub>I</sub> = V <sub>IH(AC)</sub> or V <sub>IL(AC)</sub> , CLK and CLK switching 50% duty cycle, one data input switching at one-half clock frequency, 50% duty cycle			2		μA/ clock MHz/ D input	
	Chip-select-enabled low-power active mode – 1:2 configuration				2			
C <sub>i</sub>	Data inputs, CSR, PAR_IN	V <sub>I</sub> = V <sub>REF</sub> ± 250 mV	1.8 V		2.5	3	3.5	pF
	CLK, CLK	V <sub>ICR</sub> = 0.9 V, V <sub>I(PP)</sub> = 600 mV			2		3	
	RESET	V <sub>I</sub> = V <sub>CC</sub> or GND			2.5			

† All typical values are at V<sub>CC</sub> = 1.8 V, T<sub>A</sub> = 25°C.

‡ Each V<sub>REF</sub> pin (A3 or T3) should be tested independently, with the other (untested) pin open.

**SN74SSTU32866****25-BIT CONFIGURABLE REGISTERED BUFFER  
WITH ADDRESS-PARITY TEST**

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**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 and Note 5)**

		$V_{CC} = 1.8 \text{ V} \pm 0.1 \text{ V}$	UNIT	
$f_{clock}$	Clock frequency	500	MHz	
$t_w$	Pulse duration, CLK, $\overline{CLK}$ high or low	1	ns	
$t_{act}$	Differential inputs active time (see Note 6)	10	ns	
$t_{inact}$	Differential inputs inactive time (see Note 7)	15	ns	
$t_{su}$	Setup time	DCS before $CLK\uparrow$ , $\overline{CLK}\downarrow$ , CSR high; CSR before $CLK\uparrow$ , $\overline{CLK}\downarrow$ , DCS high	0.6	ns
		DCS before $CLK\uparrow$ , $\overline{CLK}\downarrow$ , CSR low	0.5	
		DODT, DCKE, and Data before $CLK\uparrow$ , $\overline{CLK}\downarrow$	0.5	
		PAR_IN before $CLK\uparrow$ , $\overline{CLK}\downarrow$	0.5	
$t_h$	Hold time	DCS, DODT, DCKE, and Data after $CLK\uparrow$ , $\overline{CLK}\downarrow$	0.5	ns
		PAR_IN after $CLK\uparrow$ , $\overline{CLK}\downarrow$	0.5	

NOTES: 5. All inputs slew rate is 1 V/ns  $\pm 20\%$ .6. VREF must be held at a valid input level, and data inputs must be held low for a minimum time of  $t_{act}$  max, after  $\overline{RESET}$  is taken high.7. VREF, data, and clock inputs must be held at valid voltage levels (not floating) for a minimum time of  $t_{inact}$  max, after  $\overline{RESET}$  is taken low.**switching characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8 \text{ V} \pm 0.1 \text{ V}$	UNIT
$f_{max}$ (see Figure 1)				500	MHz
$t_{pdm}^{\dagger}$ (see Figure 1)		CLK and $\overline{CLK}$	Q	1.4 2.5	ns
$t_{pd}$	see Figure 4	CLK and $\overline{CLK}$	PPO	0.6 1.6	ns
$t_{PLH}$	see Figure 3	CLK and $\overline{CLK}$	QERR	1.2 3	ns
$t_{PHL}$				1 2.4	
$t_{pdmss}^{\dagger}$ (see Figure 1)		CLK and $\overline{CLK}$	Q	2.7	ns
$t_{RPHL}^{\dagger}$ (see Figure 1)		RESET	Q	3	ns
$t_{RPHL}$ (see Figure 4)			PPO	3	
$t_{RPLH}$ (see Figure 3)		RESET	QERR	3	ns

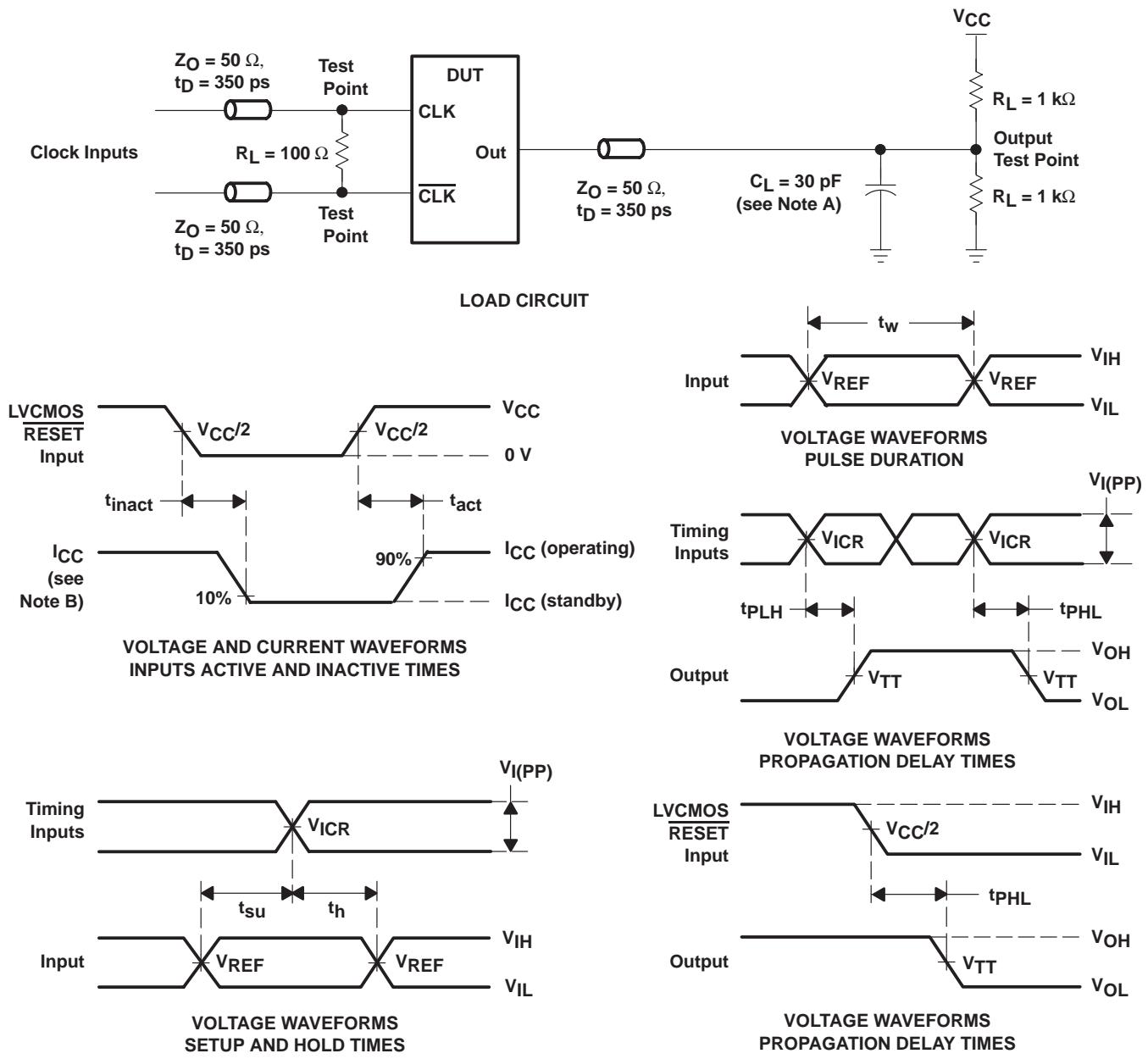
<sup>†</sup> Includes 350-ps test-load transmission-line delay.**output slew rates over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)**

PARAMETER		FROM	TO	$V_{CC} = 1.8 \text{ V} \pm 0.1 \text{ V}$	UNIT
$dV/dt_r$		20%	80%	1.9 4.9	V/ns
$dV/dt_f$		80%	20%	1.9 4.9	V/ns
$dV/dt_{\Delta}^{\ddagger}$		20% or 80%	80% or 20%	1.5	V/ns

<sup>‡</sup> Difference between  $dV/dt_r$  (rising edge rate) and  $dV/dt_f$  (falling edge rate).

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PARAMETER MEASUREMENT INFORMATION

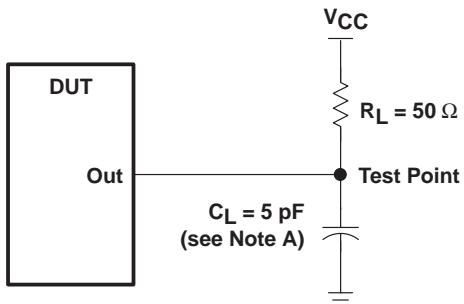


NOTES:

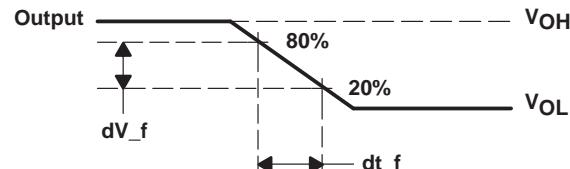
- $C_L$  includes probe and jig capacitance.
- $I_{CC}$  tested with clock and data inputs held at  $V_{CC}$  or GND, and  $I_O = 0 \text{ mA}$ .
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ , input slew rate =  $1 \text{ V/ns} \pm 20\%$  (unless otherwise noted).
- The outputs are measured one at a time, with one transition per measurement.
- $V_{REF} = V_{TT} = V_{CC}/2$
- $V_{IH} = V_{REF} + 250 \text{ mV}$  (ac voltage levels) for differential inputs.  $V_{IH} = V_{CC}$  for LVCMS input.
- $V_{IL} = V_{REF} - 250 \text{ mV}$  (ac voltage levels) for differential inputs.  $V_{IL} = \text{GND}$  for LVCMS input.
- $V_{I(PP)} = 600 \text{ mV}$
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Data Output Load Circuit and Voltage Waveforms

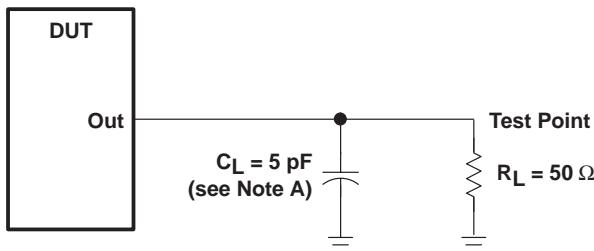
## PARAMETER MEASUREMENT INFORMATION



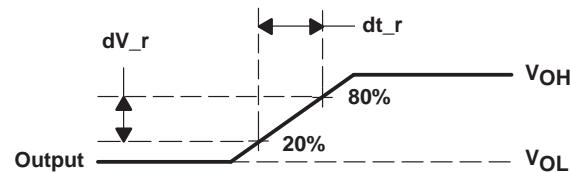
LOAD CIRCUIT  
HIGH-TO-LOW SLEW-RATE MEASUREMENT



VOLTAGE WAVEFORMS  
HIGH-TO-LOW SLEW-RATE MEASUREMENT



LOAD CIRCUIT  
LOW-TO-HIGH SLEW-RATE MEASUREMENT



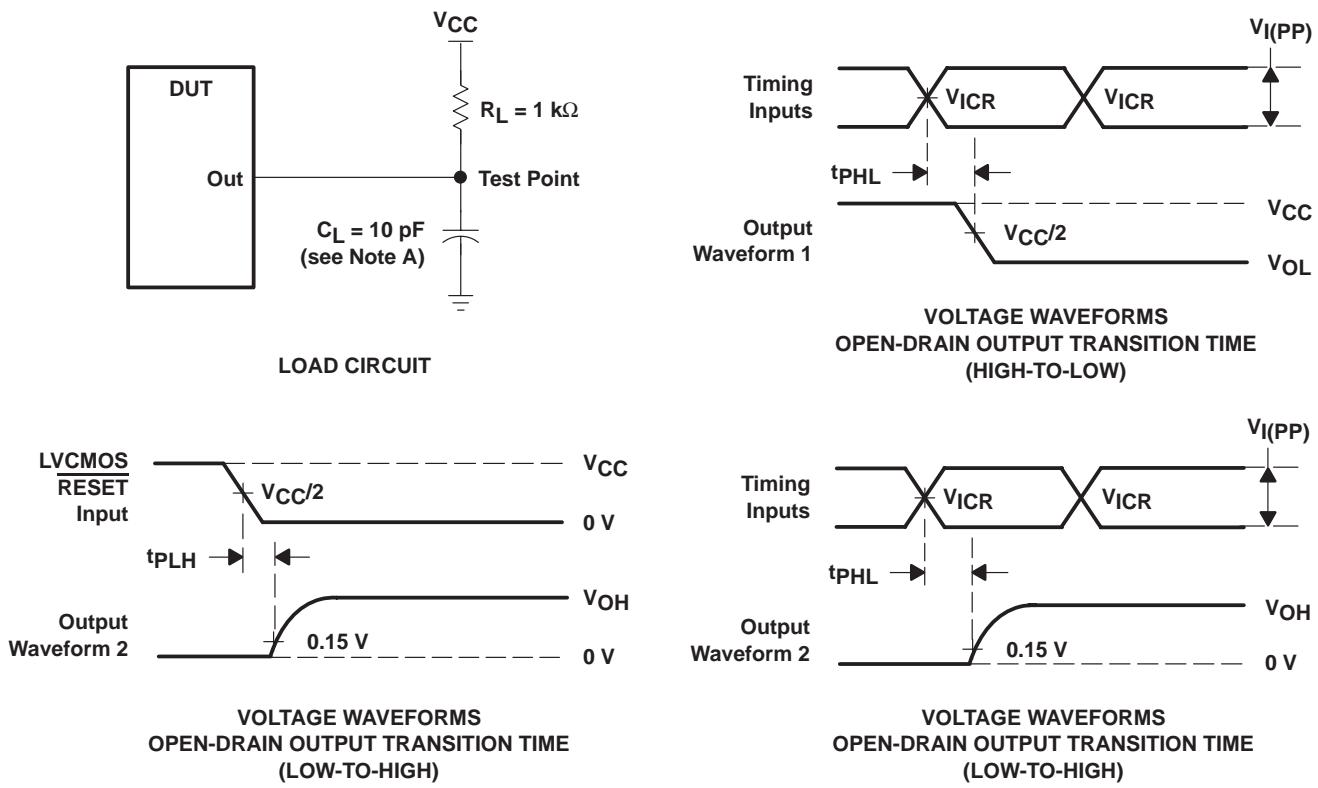
VOLTAGE WAVEFORMS  
LOW-TO-HIGH SLEW-RATE MEASUREMENT

NOTES: A.  $C_L$  includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ , input slew rate = 1 V/ns  $\pm 20\%$  (unless otherwise specified).

Figure 2. Data Output Slew-Rate Measurement Information

PARAMETER MEASUREMENT INFORMATION

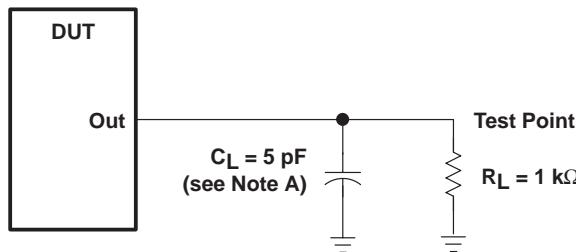


NOTES:

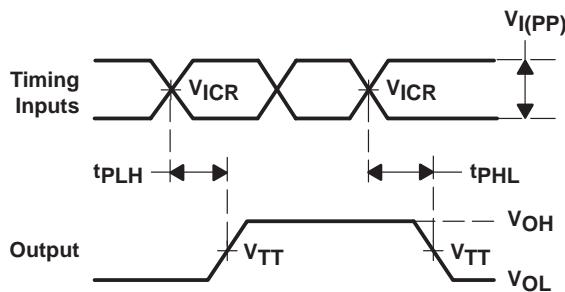
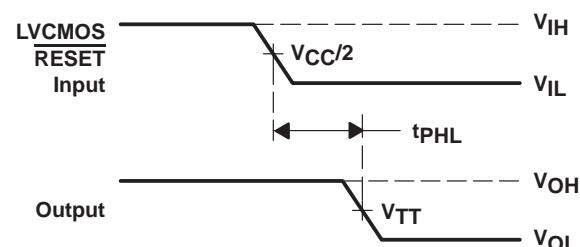
- $C_L$  includes probe and jig capacitance.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ , input slew rate =  $1 \text{ V/ns} \pm 20\%$  (unless otherwise noted).
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 3. Error Output Load Circuit and Voltage Waveforms

## PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMESVOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES

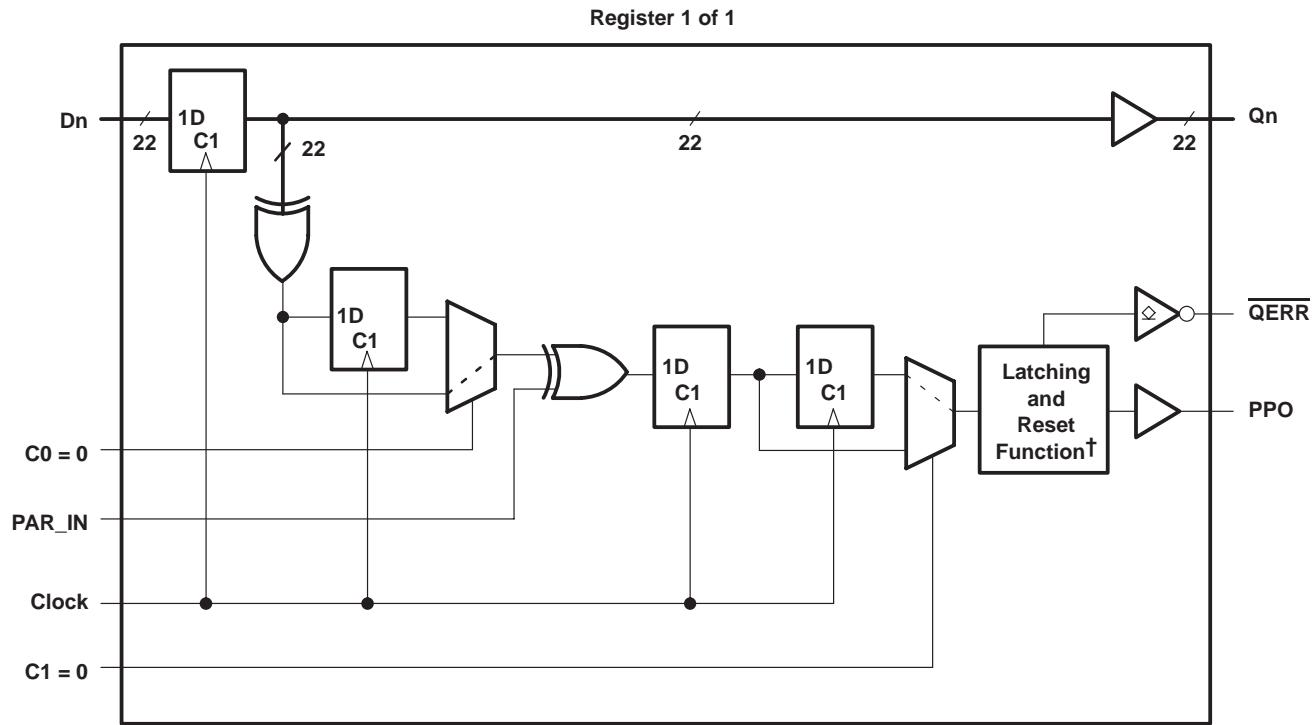
NOTES:

- $C_L$  includes probe and jig capacitance.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ , input slew rate =  $1 \text{ V/ns} \pm 20\%$  (unless otherwise noted).
- $V_{REF} = V_{TT} = V_{CC}/2$
- $V_{IH} = V_{REF} + 250 \text{ mV}$  (ac voltage levels) for differential inputs.  $V_{IH} = V_{CC}$  for LVC MOS input.
- $V_{IL} = V_{REF} - 250 \text{ mV}$  (ac voltage levels) for differential inputs.  $V_{IL} = GND$  for LVC MOS input.
- $V_{(PP)} = 600 \text{ mV}$
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 4. Partial-Parity-Out Load Circuit and Voltage Waveforms

## APPLICATION INFORMATION

SN74SSTU32866 used as a single device in the 1:1 register configuration; C0 = 0, C1 = 0



† This function holds the error for two cycles. For details, see the parity logic diagram.

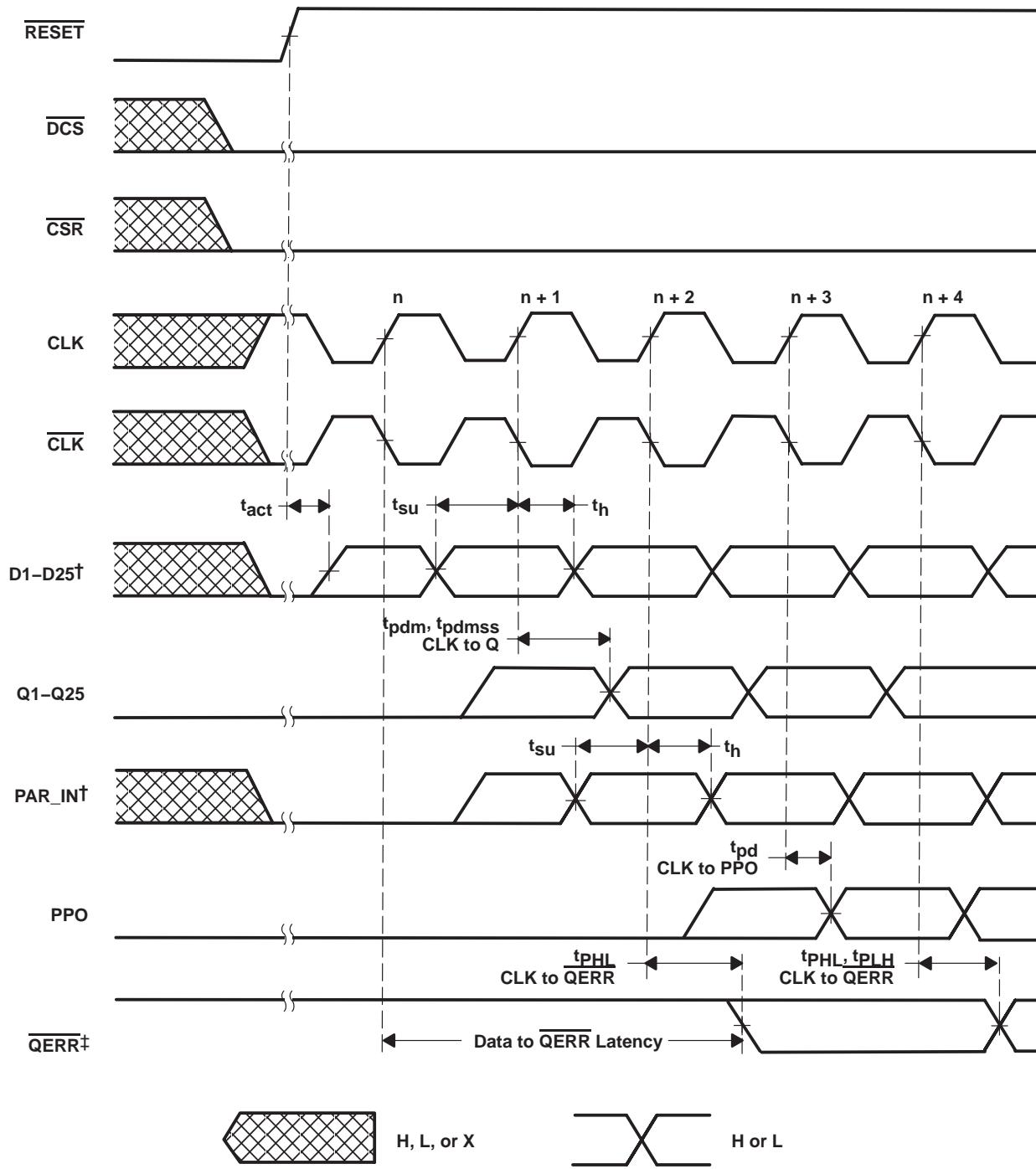
# SN74SSTU32866

## 25-BIT CONFIGURABLE REGISTERED BUFFER

### WITH ADDRESS-PARITY TEST

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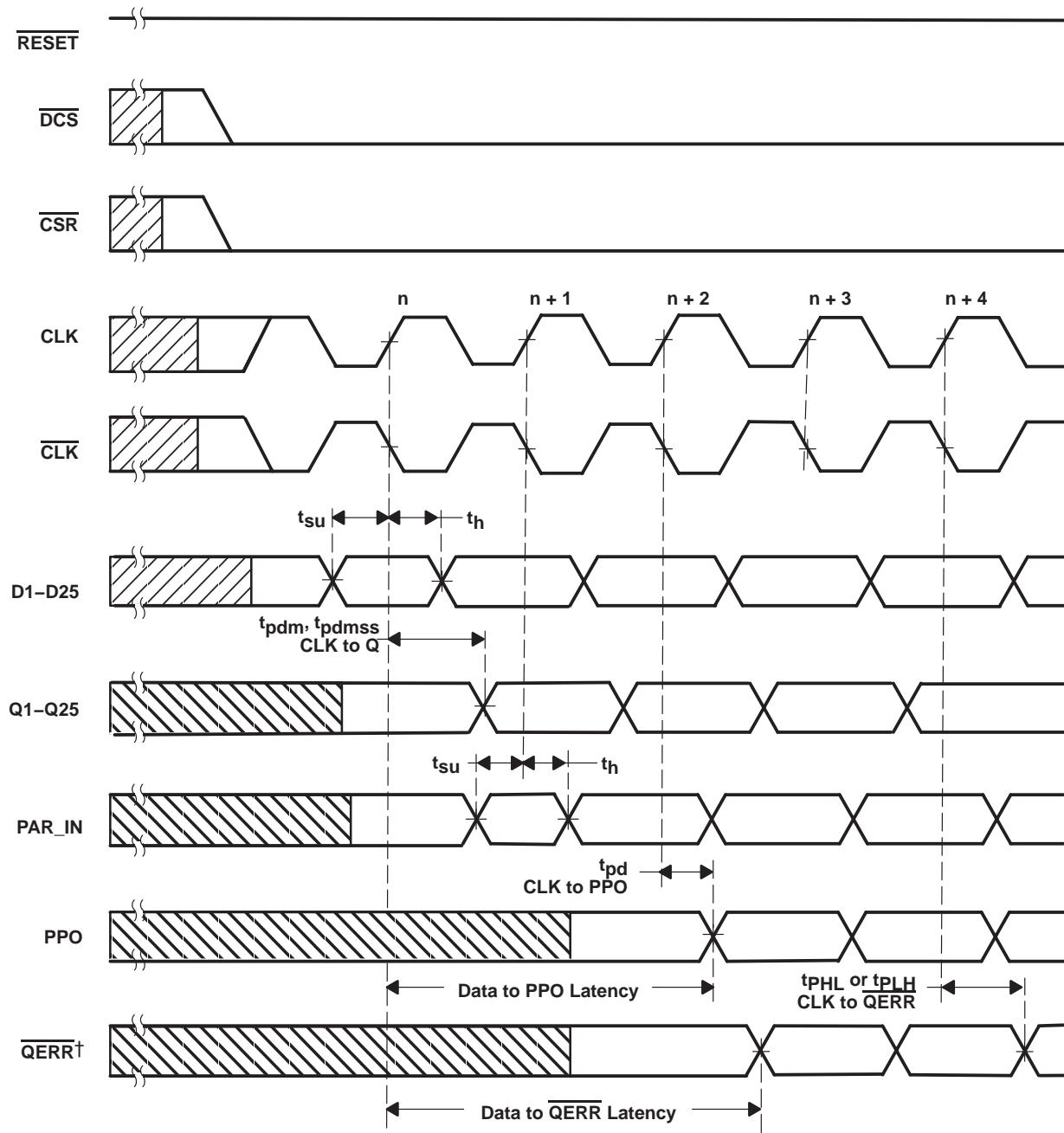
timing diagram for SN74SSTU32866 used as a single device; C0 = 0, C1 = 0  
(RESET switches from L to H)



† After **RESET** is switched from low to high, all data and PAR\_IN input signals must be set and held low for a minimum time of  $t_{act}$  max, to avoid false error.

‡ If the data is clocked in on the n clock pulse, the **QERR** output signal will be generated on the n + 2 clock pulse, and it will be valid on the n + 3 clock pulse.

timing diagram for SN74SSTU32866 used as a single device; C0 = 0, C1 = 0  
 (RESET = H)



Unknown input event

Output signal is dependent on the prior unknown input event

H or L

† If the data is clocked in on the n clock pulse, the **QERR** output signal will be generated on the n + 2 clock pulse, and it will be valid on n + 3 clock pulse. If an error occurs and the **QERR** output is driven low, it stays latched low for a minimum of two clock cycles or until **RESET** is driven low.

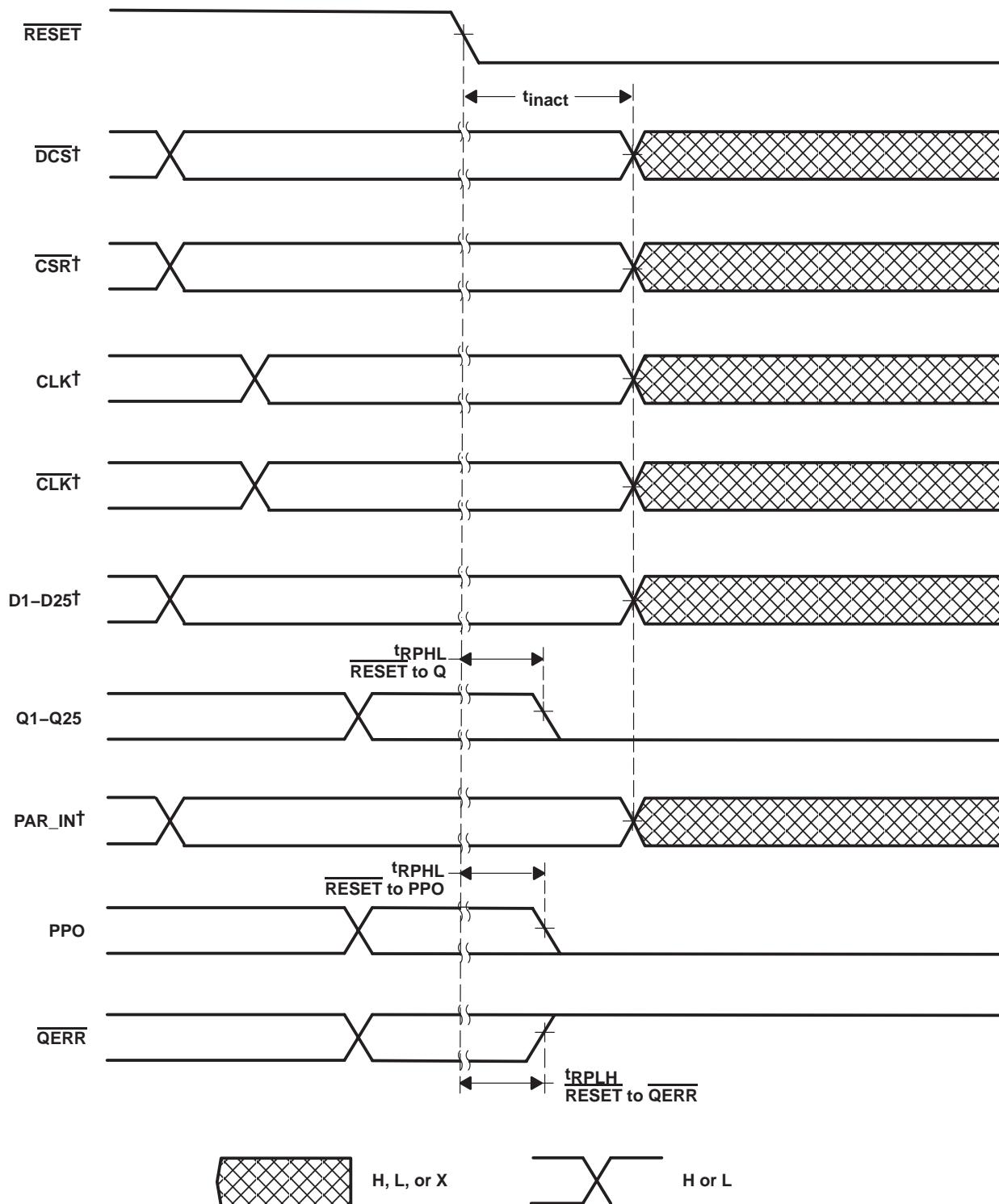
# SN74SSTU32866

## 25-BIT CONFIGURABLE REGISTERED BUFFER

### WITH ADDRESS-PARITY TEST

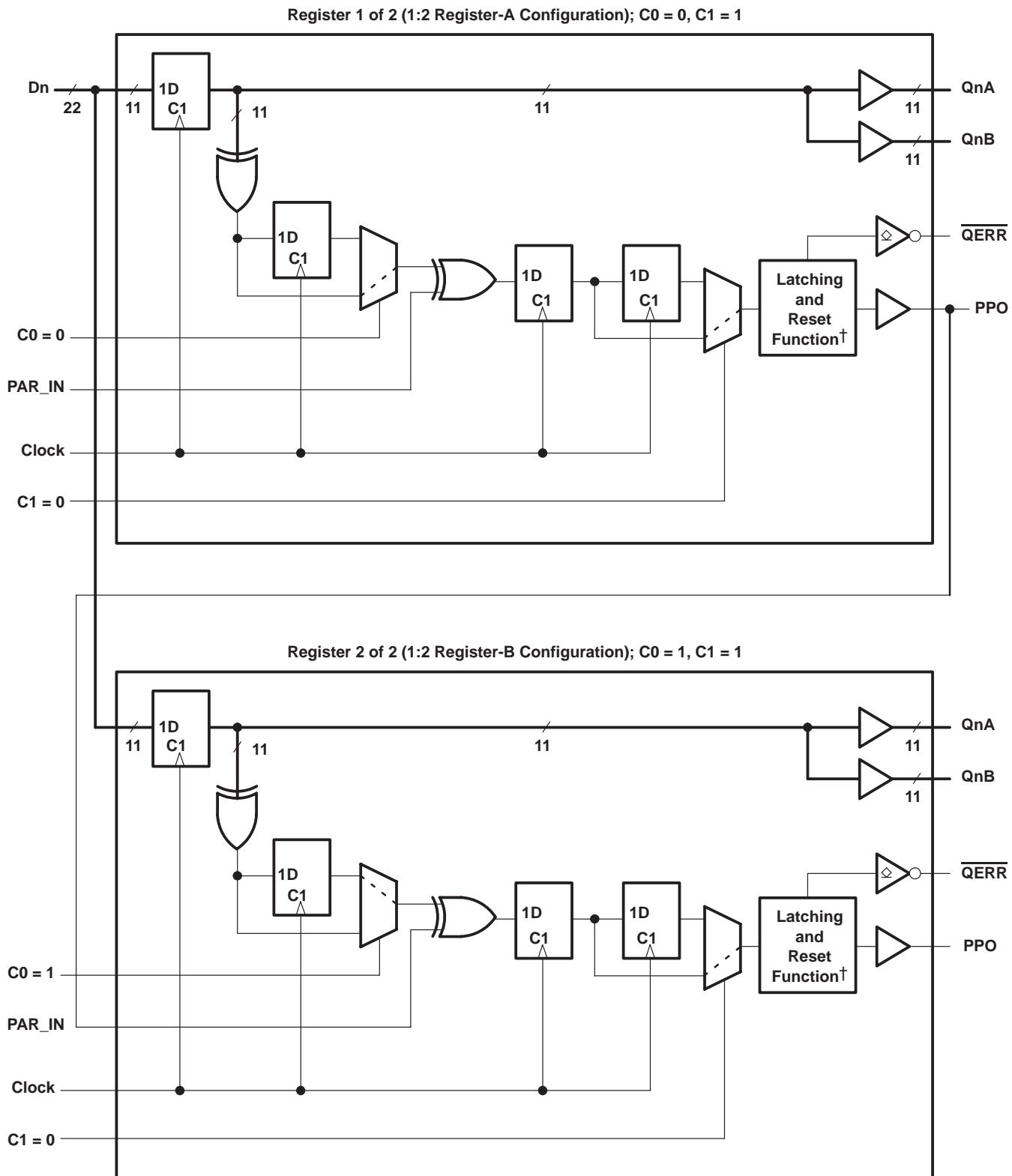
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timing diagram for SN74SSTU32866 used as a single device; C0 = 0, C1 = 0  
(RESET switches from H to L)



† After **RESET** is switched from high to low, all data and clock input signals must be held at valid logic levels (not floating) for a minimum time of  $t_{inact}$  max.

SN74SSTU32866 used in pair in the 1:2 register configuration



† This function holds the error for two cycles. For details, see the parity logic diagram.

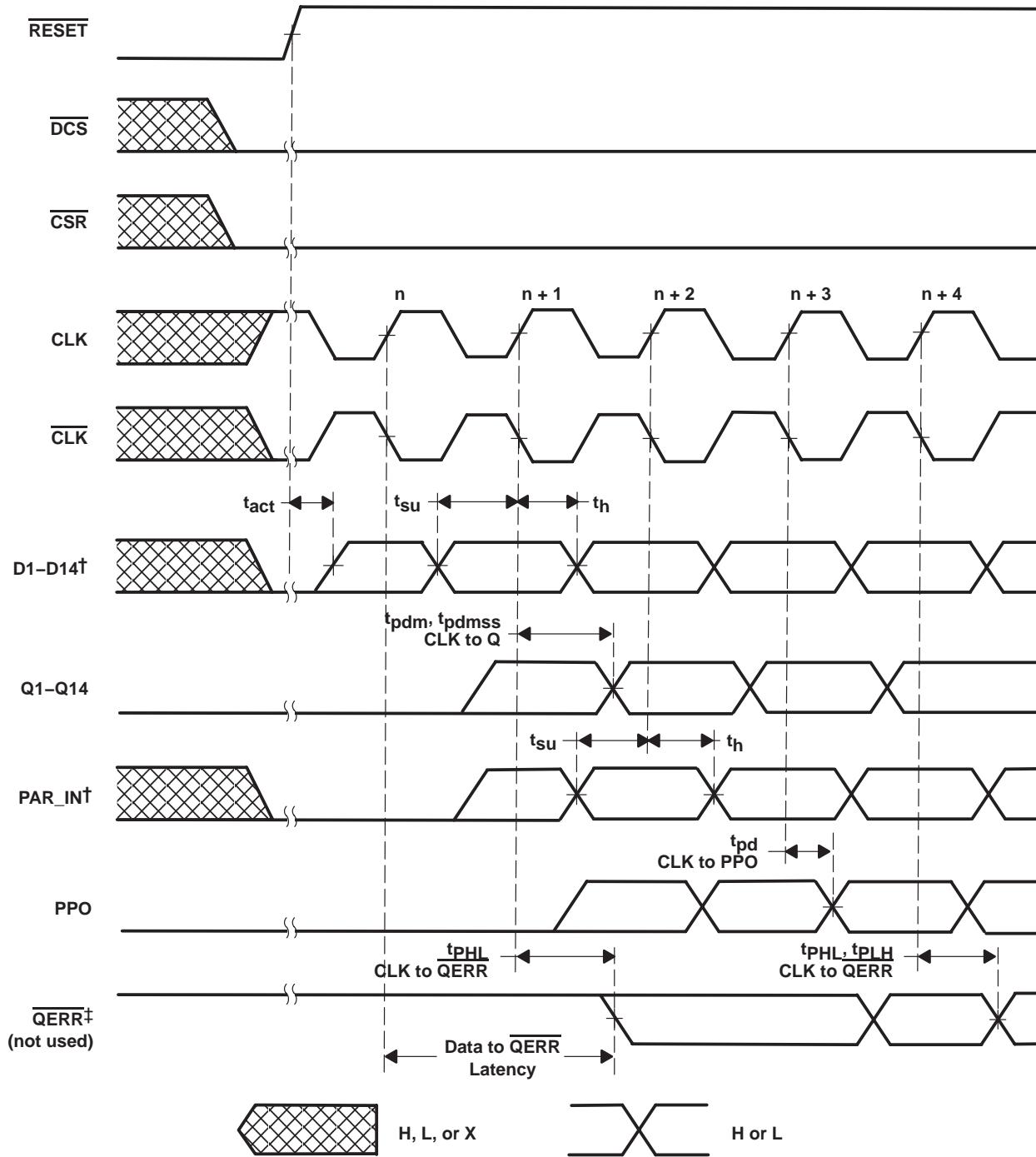
# SN74SSTU32866

## 25-BIT CONFIGURABLE REGISTERED BUFFER

### WITH ADDRESS-PARITY TEST

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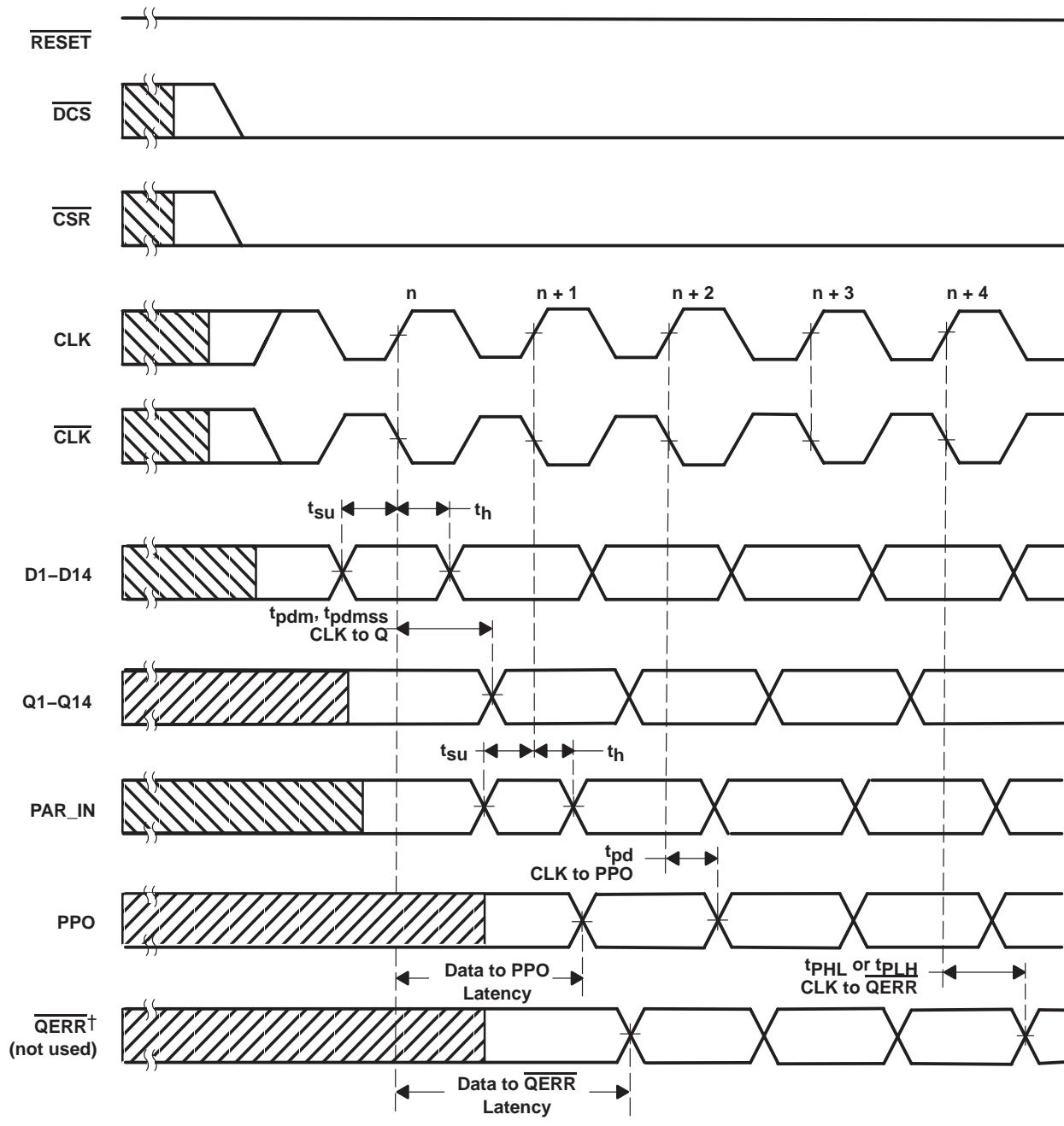
timing diagram for the first SN74SSTU32866 (1:2 Register-A configuration) device used in pair;  
 $C_0 = 0$ ,  $C_1 = 1$  (RESET switches from L to H)



† After RESET is switched from low to high, all data and PAR\_IN input signals must be set and held low for a minimum time of  $t_{act}$  max, to avoid false error.

‡ If the data is clocked in on the  $n$  clock pulse, the QERR output signal will be generated on the  $n + 1$  clock pulse, and it will be valid on the  $n + 2$  clock pulse.

timing diagram for the first SN74SSTU32866 (1:2 Register-A configuration) device used in pair;  
C0 = 0, C1 = 1 (RESET = H)



Unknown input event

Output signal is dependent on the prior unknown input event

H or L

† If the data is clocked in on the  $n$  clock pulse, the **QERR** output signal will be generated on the  $n + 1$  clock pulse, and it will be valid on  $n + 2$  clock pulse. If an error occurs and the **QERR** output is driven low, it stays latched low for a minimum of two clock cycles or until **RESET** is driven low.

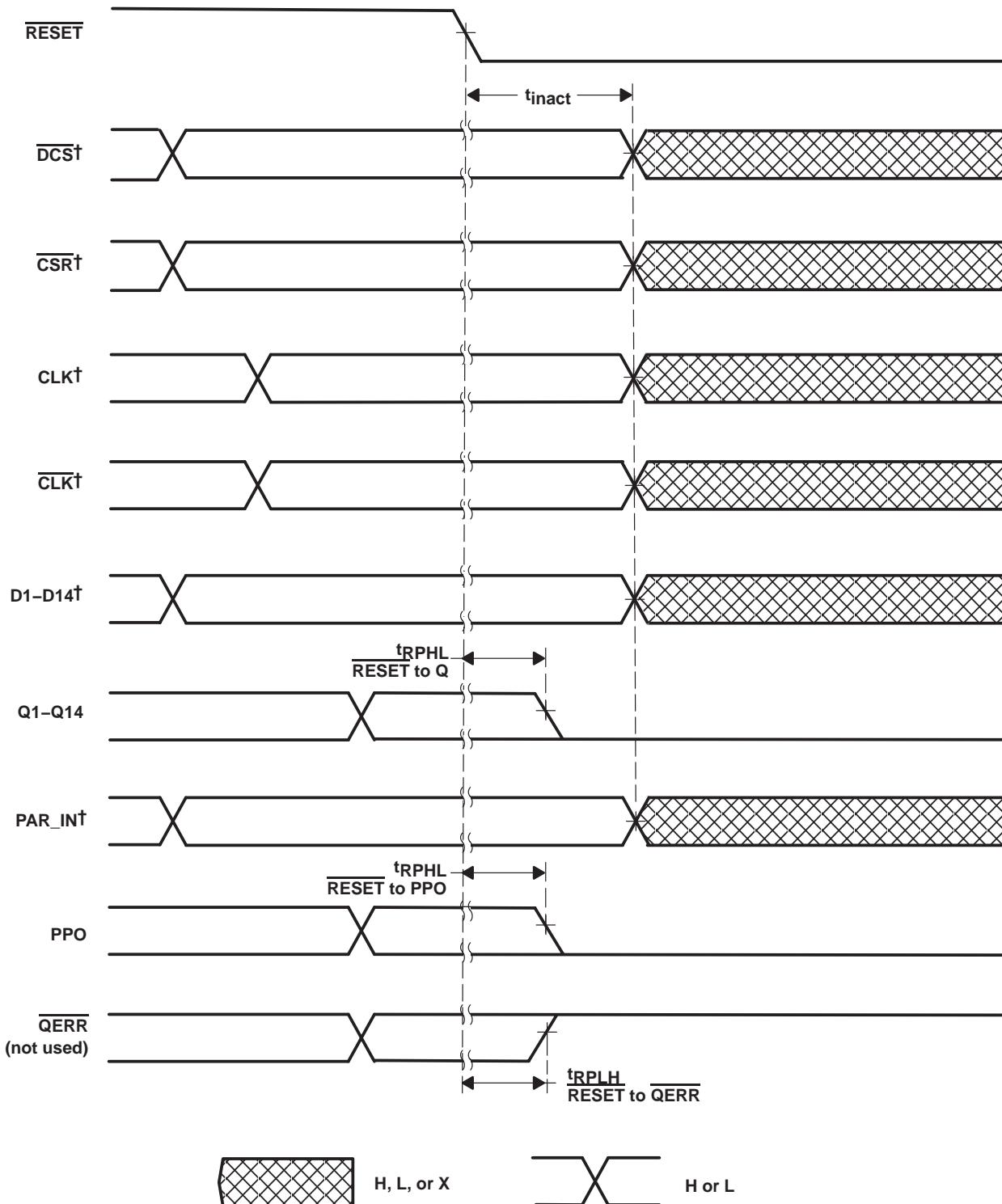
# SN74SSTU32866

## 25-BIT CONFIGURABLE REGISTERED BUFFER

### WITH ADDRESS-PARITY TEST

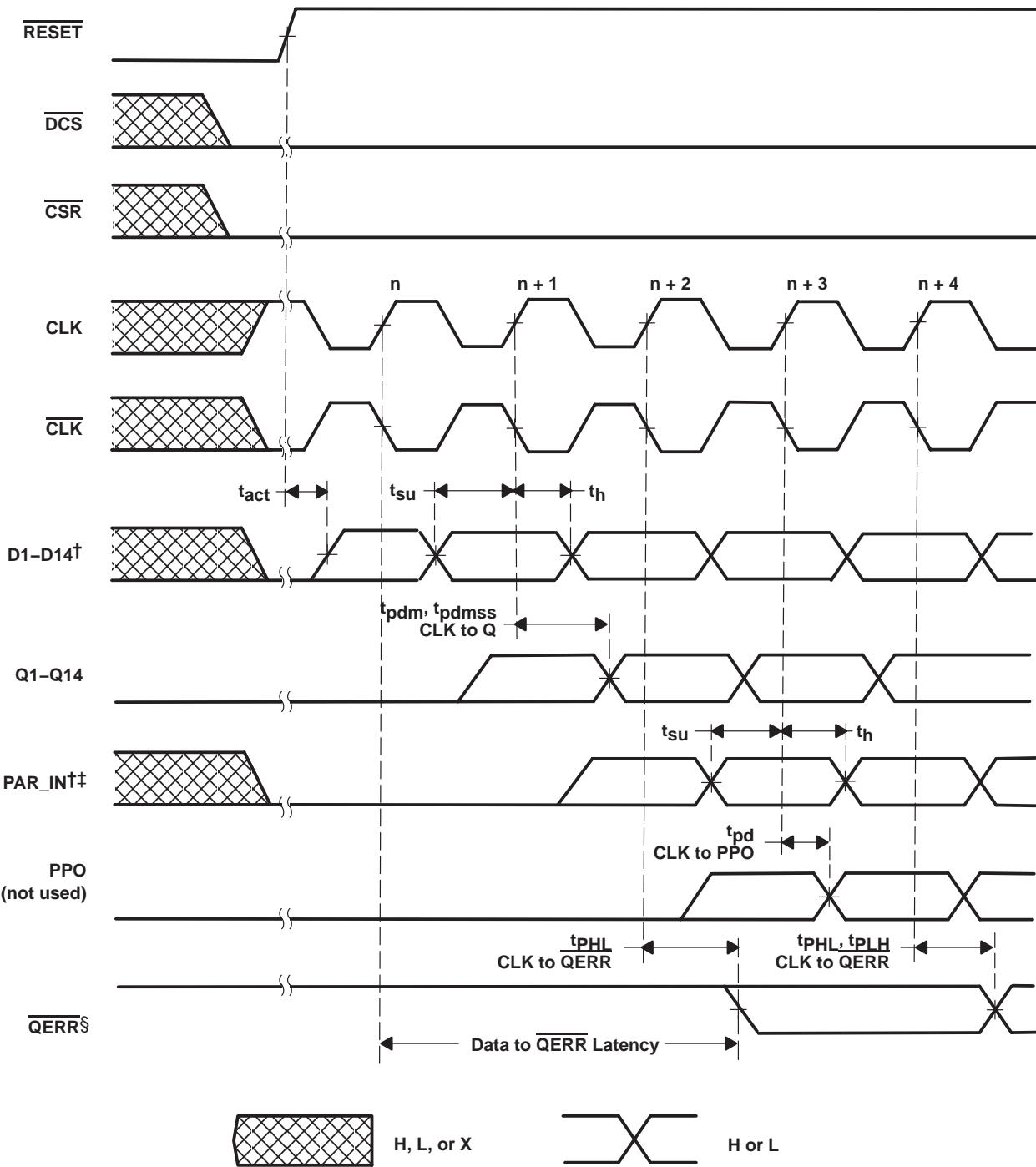
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timing diagram for the first SN74SSTU32866 (1:2 Register-A configuration) device used in pair;  
 $C_0 = 0$ ,  $C_1 = 1$  (RESET switches from H to L)



† After RESET is switched from high to low, all data and clock input signals must be held at valid logic levels (not floating) for a minimum time of  $t_{inact}$  max.

timing diagram for the second SN74SSTU32866 (1:2 Register-B configuration) device used in pair;  
C0 = 1, C1 = 1 (RESET switches from L to H)



† After RESET is switched from low to high, all data and PAR\_IN input signals must be set and held low for a minimum time of  $t_{act}$  max, to avoid false error.

‡ PAR\_IN is driven from PPO of the first SN74SSTU32866 device.

§ If the data is clocked in on the n clock pulse, the QERR output signal will be generated on the n + 2 clock pulse, and it will be valid on the n + 3 clock pulse.

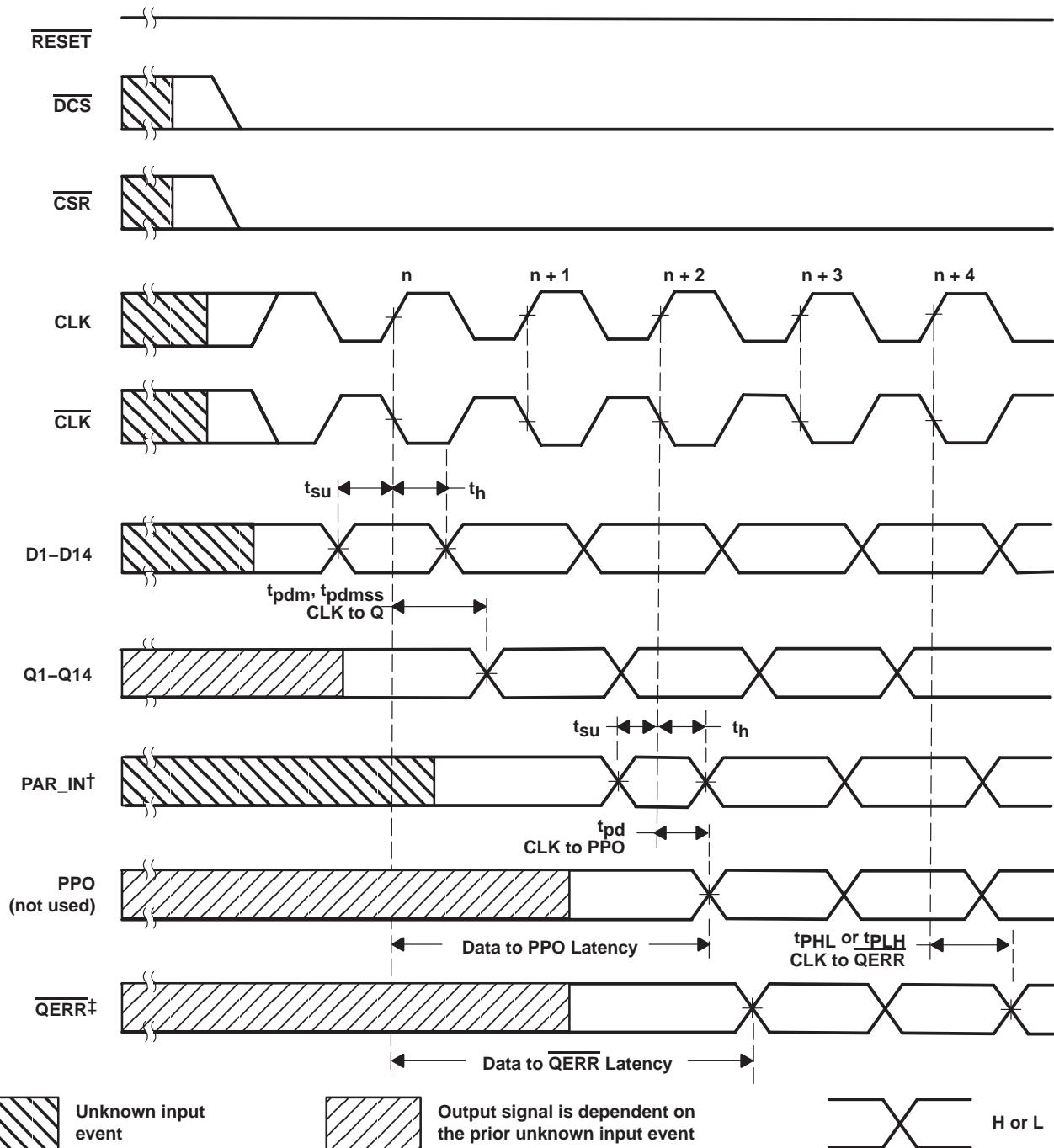
# SN74SSTU32866

## 25-BIT CONFIGURABLE REGISTERED BUFFER

### WITH ADDRESS-PARITY TEST

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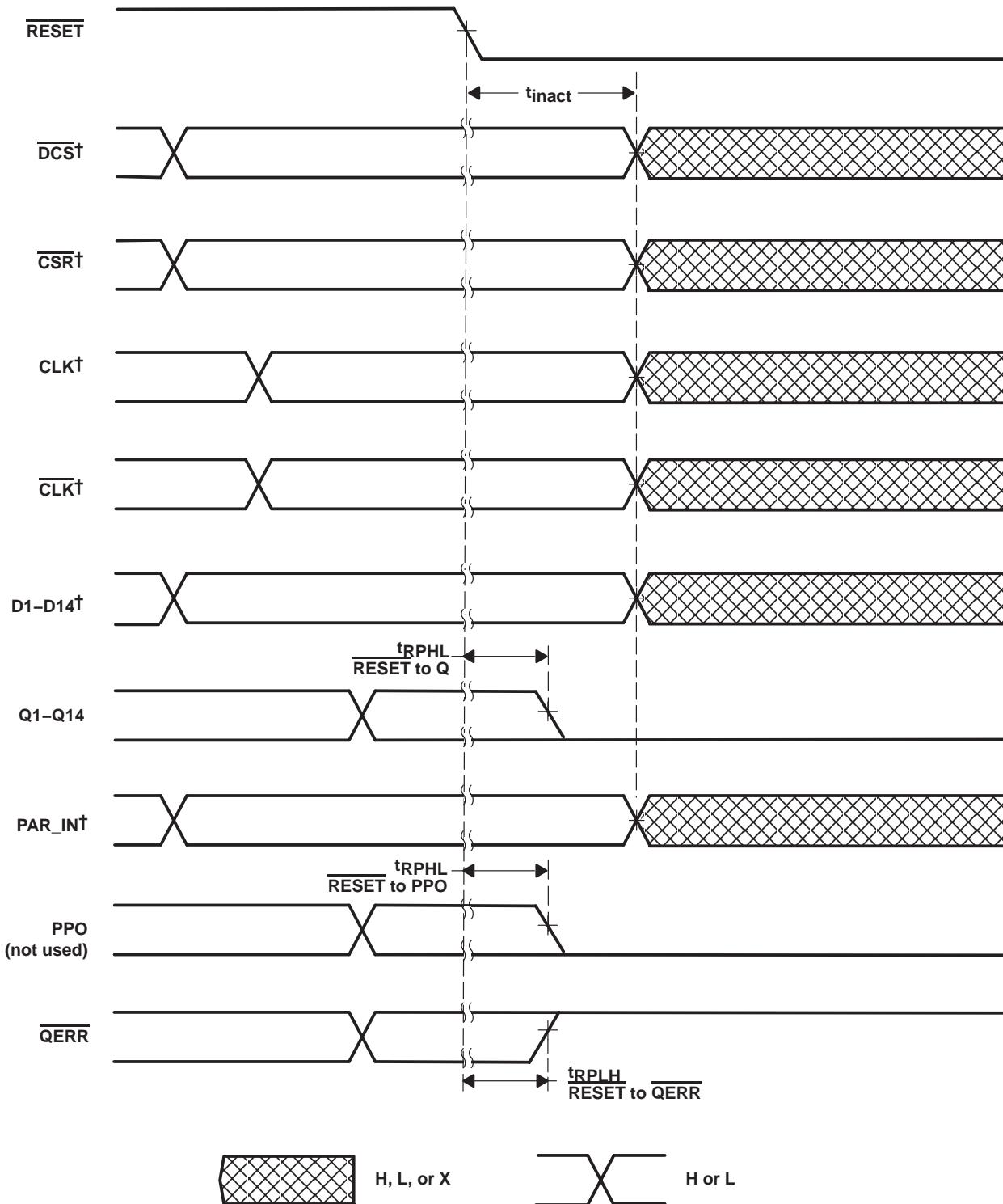
timing diagram for the second SN74SSTU32866 (1:2 Register-B configuration) device used in pair;  
 $C_0 = 1$ ,  $C_1 = 1$  (RESET = H)



<sup>†</sup> PAR\_IN is driven from PPO of the first SN74SSTU32866 device.

<sup>‡</sup> If the data is clocked in on the n clock pulse, the QERR output signal will be generated on the n + 2 clock pulse, and it will be valid on n + 3 clock pulse. If an error occurs and the QERR output is driven low, it stays latched low for a minimum of two clock cycles or until RESET is driven low.

timing diagram for the second SN74SSTU32866 (1:2 Register-B configuration) device used in pair;  
C0 = 1, C1 = 1 (RESET switches from H to L)



† After **RESET** is switched from high to low, all data and clock input signals must be held at valid logic levels (not floating) for a minimum time of  $t_{inact}$  max.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74SSTU32866ZKER	ACTIVE	LFBGA	ZKE	96	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 70	SU866	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

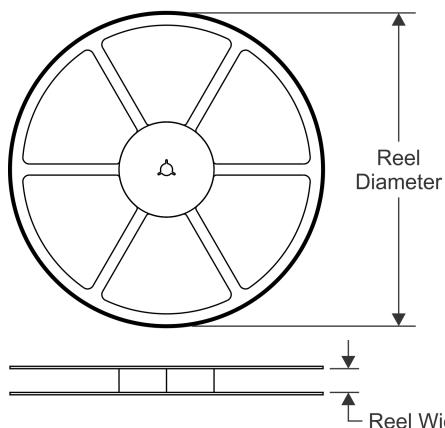
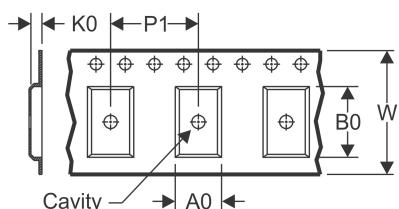
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

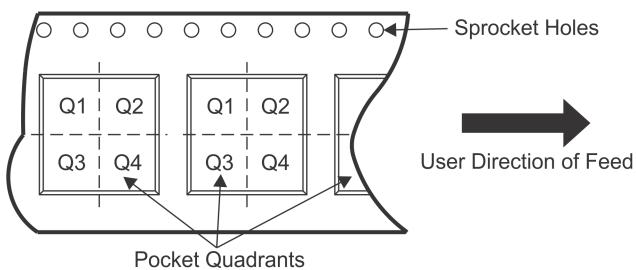
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74SSTU32866ZKER	LFBGA	ZKE	96	1000	330.0	24.4	5.7	13.7	2.0	8.0	24.0	Q1

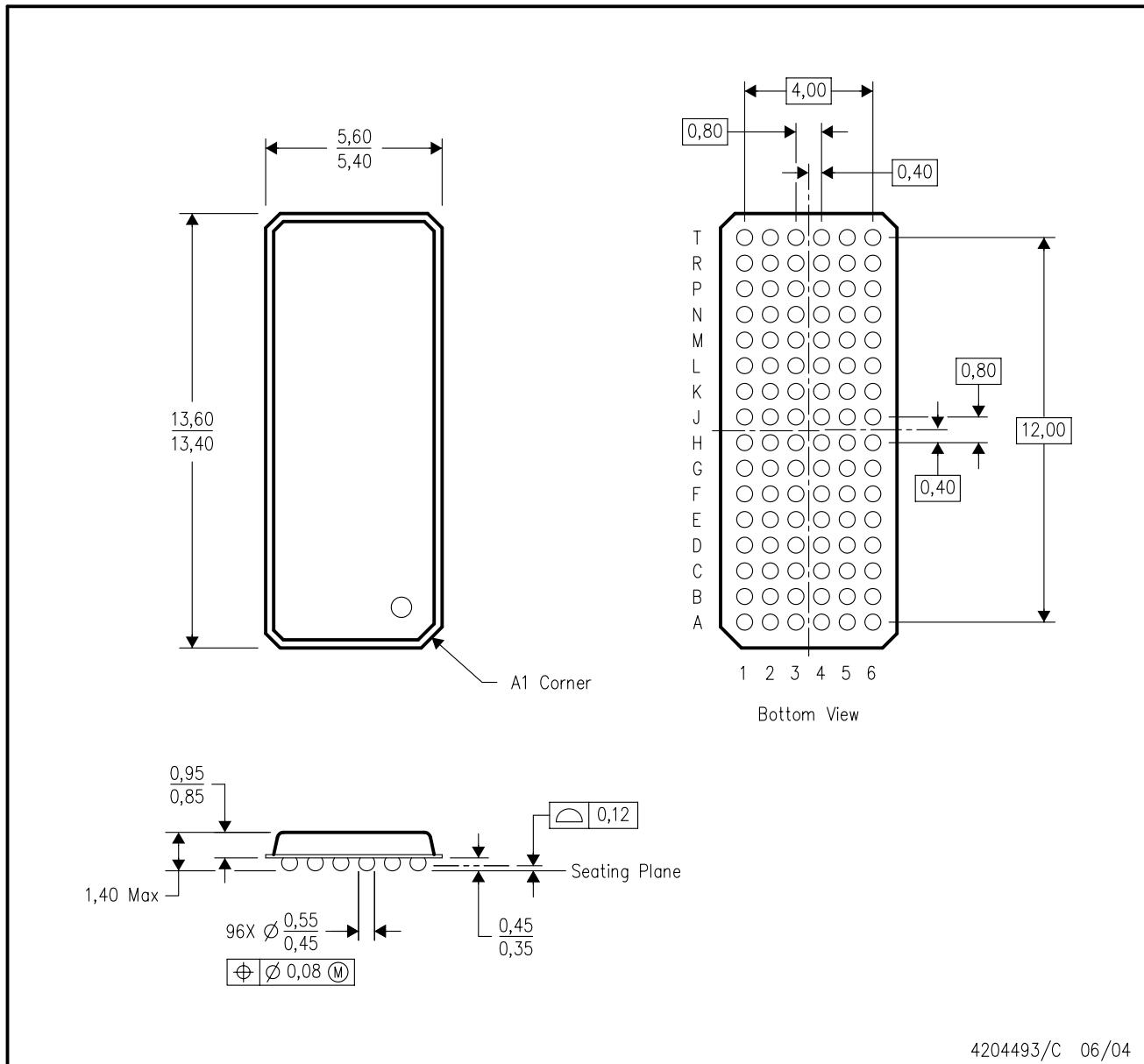
**TAPE AND REEL BOX DIMENSIONS**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74SSTU32866ZKER	LFBGA	ZKE	96	1000	336.6	336.6	41.3

## ZKE (R-PBGA-N96)

## PLASTIC BALL GRID ARRAY



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Falls within JEDEC MO-205 variation CC.
- This package is lead-free. Refer to the 96 GKE package (drawing 4188953) for tin-lead (SnPb).

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