

6 W hi-fi audio power amplifier

TDA2614

FEATURES

- Requires very few external components
- No switch-on/switch-off clicks
- Input mute during switch-on and switch-off
- Low offset voltage between output and ground
- Hi-fi in accordance with IEC 268 and DIN 45500
- Short-circuit proof and thermal protected
- Mute possibility.

GENERAL DESCRIPTION

The TDA2614 is a power amplifier in a 9-lead single-in-line (SIL9) plastic medium power package. It has been especially designed for mains fed applications, such as TV and radio.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_p	positive supply voltage range		15	—	42	V
P_o	output power	$V_s = 24 \text{ V}$; THD = 0.5%	—	6.5	—	W
G_v	internal voltage gain		—	30	—	dB
SVRR	supply voltage ripple rejection		—	45	—	dB
V_{no}	noise output voltage		—	70	—	μV

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA2614	9	SIL	plastic	SOT110

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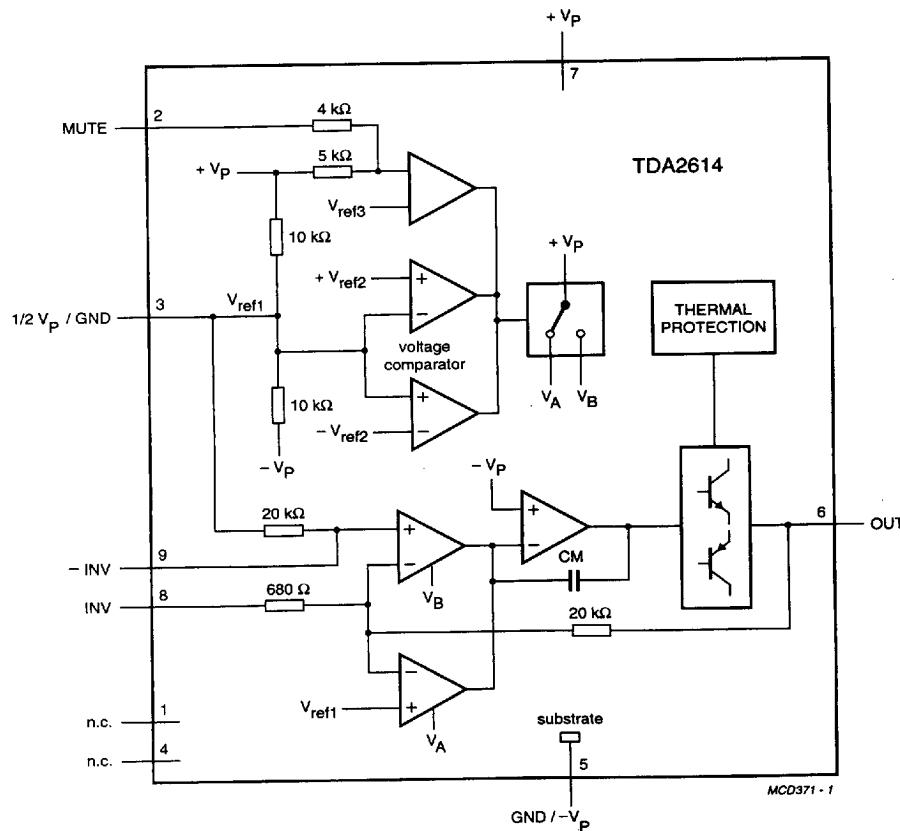


Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
MUTE	2	mute input
1/2V _P /GND	3	1/2 supply (or ground at symmetrical power supplies)
n.c.	4	not connected
GND/-V _P	5	ground (or negative supply rail at symmetrical power supplies)
OUT	6	output
V _P	7	supply voltage
INV	8	inverting input
-INV	9	non-inverting input

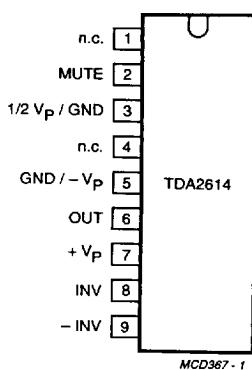


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA2614 is a hi-fi power amplifier designed for mains fed applications, such as radio and TV. The circuit is optimally designed for asymmetrical power supplies, but is also well-suited to symmetrical power supply systems.

An output power of 6 W (THD = 0.5%) can be delivered into an 8 Ω load with a supply of 24 V. The gain is internally fixed at 30 dB, thus offering a low gain spread.

A special feature is the input mute circuit. This circuit disconnects the non-inverting input when the supply voltage drops below 10 V, while the amplifier still retains its DC operating adjustment. The circuit features suppression of unwanted signals at the input, during switch-on and switch-off.

The mute circuit can also be activated via pin 2. When a current of 300 μA is present at pin 2, the circuit is in the mute condition.

The device is provided with two thermal protection circuits. One circuit measures the average temperature of the crystal and the other measures the momentary temperature of the power transistors. These control circuits activate at temperatures in excess of 150 °C, so a crystal operating temperature of max. 150 °C can be used without extra distortion.

With the derating value of 8 K/W, the heatsink can be calculated as follows:

at $R_L = 8 \Omega$ and $V_S = 24$ V, dissipation is 4.1 W.

With a maximum ambient temperature of 60 °C, the thermal resistance of the heatsink is:

$$R_{th} = \frac{150 - 60}{4.1} - 8 = 14 \text{ K/W.}$$

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LIMITING VALUES

In accordance with the Absolute maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_p	positive supply voltage		—	42	V
I_{osm}	non-repetitive peak output current		—	4	A
P_{tot}	total power dissipation	see Fig.3	—	15	W
T_{stg}	storage temperature range		-55	+150	°C
T_{XTAL}	crystal temperature		—	+150	°C
T_{amb}	ambient operating temperature range		-25	+150	°C
t_{sc}	short circuit time	short circuit to ground; note 1	—	1	h

Note to the limiting values

1. For asymmetrical power supplies (with the load short-circuited), the maximum unloaded supply voltage is limited to $V_p = 28$ V, and with an internal supply resistance of $R_s \geq 4 \Omega$, the maximum unloaded supply voltage is limited to 32 V (with the load short-circuited). For symmetrical power supplies, the circuit is short-circuit-proof up to $V_p = \pm 21$ V.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th, jc}$	from junction to case	8 K/W

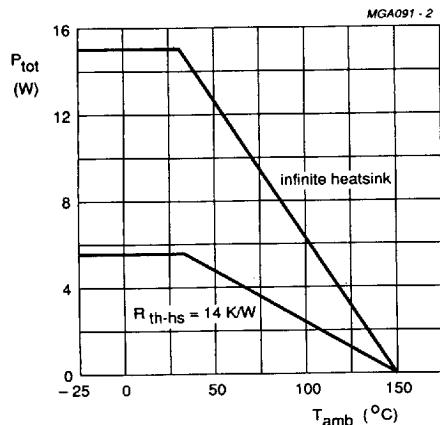


Fig.3 Power derating curve.

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CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage range		-	24	42	V
I_{ORM}	repetitive peak output current		-	2.2	-	A
Operating position; note 1						
V_P	supply voltage range		15	24	42	V
I_P	total quiescent current		10	20	35	mA
P_O	output power	THD = 0.5% THD = 10% THD = 0.5%; $R_L = 4 \Omega$ THD = 10%; $R_L = 4 \Omega$	5 6.5 - -	6.5 8.5 10 14	- - - -	W W W W
THD	total harmonic distortion	$P_O = 4 \text{ W}$	-	0.15	0.2	%
B	power bandwidth	THD = 0.5%; note 2	-	30 to 20 000	-	Hz
G_V	voltage gain		29	30	31	dB
$ \Delta V_{3-6} $	DC output offset voltage		-	30	200	mV
V_{no}	noise output voltage	note 3	-	70	140	μV
$ Z_i $	input impedance		14	20	26	$\text{k}\Omega$
SVRR	supply voltage ripple rejection	note 4	35	45	-	dB
I_{bias}	input bias current		-	0.3	-	μA
MUTE POSITION (AT $I_{MUTE} \geq 300 \mu\text{A}$)						
V_o	output voltage	$V_i = 600 \text{ mV}$	-	0.1	1.0	mV
Z_{2-7}	mute input impedance		-	9	-	$\text{k}\Omega$
I_P	total quiescent current		10	20	35	mA
V_{no}	noise output voltage	note 3	-	70	140	μV
SVRR	supply voltage ripple rejection	note 4	35	44	-	dB
$ \Delta V_{3-6} $	DC output offset voltage		-	40	200	mV
$ \Delta V_{off} $	offset voltage with respect to operating position		-	4	150	mV
I_2	current if pin 2 is connected to pin 5		-	-	6	mA
Mute position; note 5						
V_P	positive supply voltage range		4	-	10	V
I_P	total quiescent current	$R_L = \delta$	5	15	20	mA
V_o	output voltage	$V_i = 600 \text{ mV}$	-	0.1	1.0	mV
V_{no}	noise output voltage	note 3	-	70	140	μV
SVRR	supply voltage ripple rejection	note 4	35	44	-	dB
$ \Delta V_{3-6} $	DC output offset voltage		-	40	200	mV

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating position; note 6						
$\pm V_p$	supply voltage range		7.5	12	21	V
I_p	total quiescent current		10	20	35	mA
P_o	output power	THD = 0.5% THD = 10% $P_o = 4 \text{ W}$	5 6.5	6.5 8	— —	W W
THD	total harmonic distortion	$P_o = 4 \text{ W}$	—	0.13	0.2	%
B	power bandwidth	THD = 0.5%; note 2	—	40 to 20 000	—	Hz
G_v	voltage gain		29	30	31	dB
V_{no}	noise output voltage	note 3	—	70	140	μV
$ Z_i $	input impedance		14	20	26	$\text{k}\Omega$
SVRR	supply voltage ripple rejection		40	55	—	dB
I_{bias}	input bias current		—	0.3	—	μA
$ \Delta V_{GND} $	DC output offset voltage		—	30	200	mV
MUTE POSITION (AT $I_{MUTE} \geq 300 \mu\text{A}$)						
V_o	output voltage	$V_i = 600 \text{ mV}$	—	0.1	1.0	mV
$Z_{2.7}$	mute input impedance	note 7	6.7	9	11.3	$\text{k}\Omega$
I_p	total quiescent current	$R_L = \infty$	10	20	35	mA
V_{no}	noise output voltage	note 3	—	70	140	μV
SVRR	supply voltage ripple rejection	note 4	40	55	—	dB
$ \Delta V_{GND} $	DC output offset voltage		—	40	200	mV
$ \Delta V_{off} $	offset voltage with respect to operating position		—	4	150	mV
I_2	current if pin 2 is connected to pin 5		—	—	6	mA

Notes to the characteristics

1. $V_p = 24 \text{ V}$; $R_L = 8 \Omega$; $T_{amb} = 25^\circ\text{C}$; $f = 1 \text{ kHz}$; asymmetrical power supply $I_{MUTE} < 30 \mu\text{A}$. See Fig.5
2. The power bandwidth is measured at an output power of $P_o \text{ max} - 3 \text{ dB}$.
3. The noise output voltage (RMS value) is measured at $R_s = 2 \text{ k}\Omega$, unweighted (20 Hz to 20 kHz).
4. The ripple rejection is measured at $R_s = 0$ and $f = 100 \text{ Hz}$ to 20 kHz , at a ripple voltage of 200 mV . With symmetrical power supplies, the ripple (200 mV) is applied in phase to the positive and the negative supply rails. With asymmetrical power supplies, the ripple rejection is measured at $f = 1 \text{ kHz}$.
5. $V_p = 8 \text{ V}$; $R_L = 8 \Omega$; $T_{amb} = 25^\circ\text{C}$; $f = 1 \text{ kHz}$; asymmetrical power supply. See Fig.5
6. $\pm V_p = 12 \text{ V}$; $R_L = 8 \Omega$; $T_{amb} = 25^\circ\text{C}$; $f = 1 \text{ kHz}$; symmetrical power supply $I_{MUTE} < 30 \mu\text{A}$. See Fig.4
7. The internal network at pin 2 is a resistor divider of typical $4 \text{ k}\Omega$ and $5 \text{k}\Omega$ to the positive supply rail. At the connection of the $4 \text{ k}\Omega$ and $5 \text{k}\Omega$ resistor a zener diode of typical 6.6 V is also connected to the positive supply rail. The spread of the zener voltage is 6.1 to 7.1 V .

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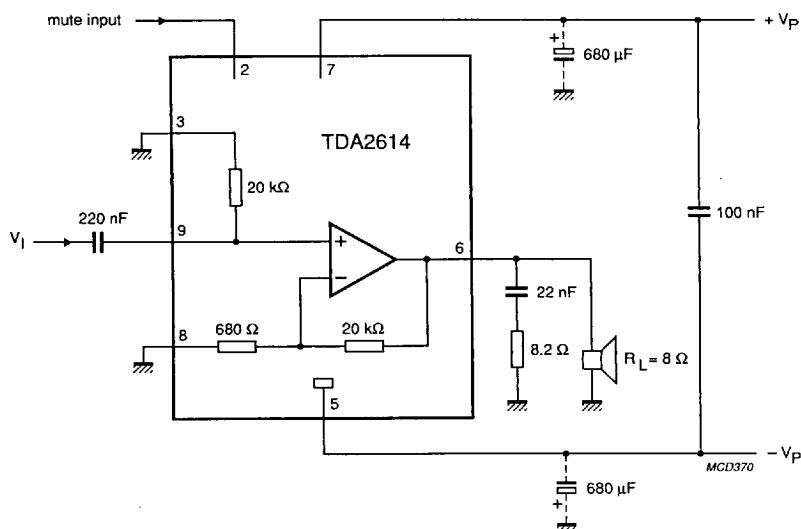


Fig.4 Test and application circuit with symmetrical power supply.

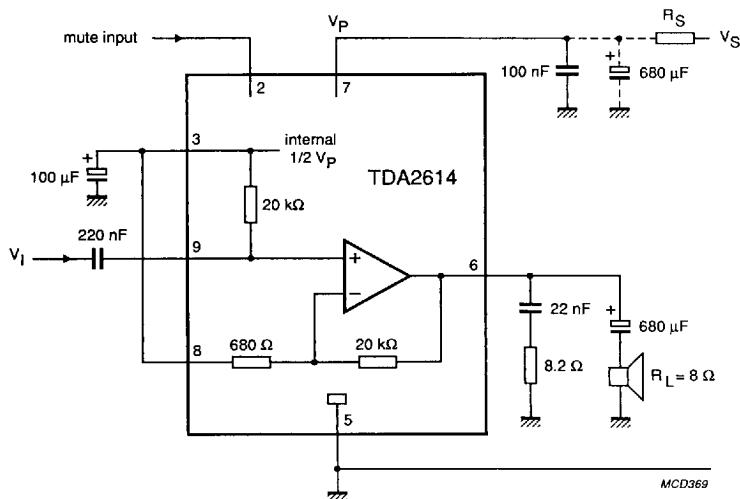


Fig.5 Test and application circuit with asymmetrical power supply.