

325MHz, Single/Dual, Rail-to-Rail Input and Output, Low Distortion, Low Noise Precision Op Amps

FEATURES

- **Gain-Bandwidth Product: 325MHz**
- **Slew Rate: 140V/μs**
- **Wide Supply Range: 2.5V to 12.6V**
- **Large Output Current: 85mA**
- **Low Distortion, 5MHz: -80dBc**
- **Low Voltage Noise: 3.5nV/√Hz**
- Input Common Mode Range Includes Both Rails
- Output Swings Rail-to-Rail
- Input Offset Voltage (Rail-to-Rail): 550μV Max
- Common Mode Rejection: 106dB Typ
- Power Supply Rejection: 105dB Typ
- Unity-Gain Stable
- Power Down Pin (LT1806)
- Operating Temperature Range: -40°C to 85°C
- Single in SO-8 and 6-Pin Low Profile (1mm) ThinSOT™ Packages
- Dual in SO-8 and 8-Pin MSOP Packages

APPLICATIONS

- Low Voltage, High Frequency Signal Processing
- Driving A/D Converters
- Rail-to-Rail Buffer Amplifiers
- Active Filters
- Video Line Driver

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DESCRIPTION

The LT®1806/LT1807 are single/dual low noise rail-to-rail input and output unity-gain stable op amps that feature a 325MHz gain-bandwidth product, a 140V/μs slew rate and a 85mA output current. They are optimized for low voltage, high performance signal conditioning systems.

The LT1806/LT1807 have a very low distortion of -80dBc at 5MHz, a low input referred noise voltage of 3.5nV/√Hz and a maximum offset voltage of 550μV that allows them to be used in high performance data acquisition systems.

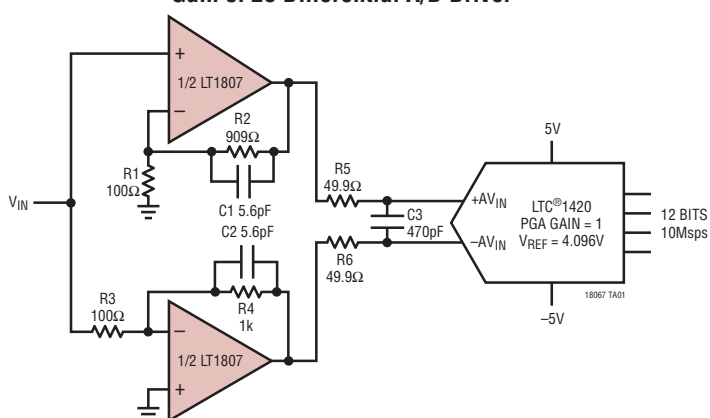
The LT1806/LT1807 have an input range that includes both supply rails and an output that swings within 20mV of either supply rail to maximize the signal dynamic range in low supply applications.

The LT1806/LT1807 maintain their performance for supplies from 2.5V to 12.6V and are specified at 3V, 5V and ±5V supplies. The inputs can be driven beyond the supplies without damage or phase reversal of the output.

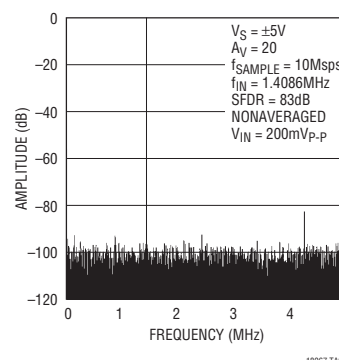
The LT1806 is available in an 8-pin SO package with the standard op amp pinout and a 6-pin TSOT-23 package. The LT1807 features the standard dual op amp pinout and is available in 8-pin SO and MSOP packages. These devices can be used as plug-in replacements for many op amps to improve input/output range and performance.

TYPICAL APPLICATION

Gain of 20 Differential A/D Driver



4096 Point FFT Response



18067fc

LT1806/LT1807

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 12.6V
Input Voltage (Note 2) $\pm V_S$
Input Current (Note 2) $\pm 10\text{mA}$
Output Short-Circuit Duration (Note 3) Indefinite
Operating Temperature Range (Note 4) ... -40°C to 85°C

Specified Temperature Range (Note 5) -40°C to 85°C
Junction Temperature 150°C
Storage Temperature Range -65°C to 150°C
Lead Temperature (Soldering, 10 sec) 300°C

PIN CONFIGURATION

TOP VIEW S6 PACKAGE 6-LEAD PLASTIC TSOT-23 $T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 160^\circ\text{C/W}$ (Note 9)	TOP VIEW S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 100^\circ\text{C/W}$ (Note 9)
TOP VIEW MS8 PACKAGE 8-LEAD PLASTIC MSOP $T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 135^\circ\text{C/W}$ (Note 9)	TOP VIEW S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 100^\circ\text{C/W}$ (Note 9)

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT1806CS6#PBF	LT1806CS6#TRPBF	LTNK	6-Lead Plastic TSOT-23	0°C to 70°C
LT1806IS6#PBF	LT1806IS6#TRPBF	LTNL	6-Lead Plastic TSOT-23	-40°C to 85°C
LT1806CS8#PBF	LT1806CS8#TRPBF	1806	8-Lead Plastic SO	0°C to 70°C
LT1806IS8#PBF	LT1806IS8#TRPBF	1806I	8-Lead Plastic SO	-40°C to 85°C
LT1807CMS8#PBF	LT1807CMS8#TRPBF	LTTT	8-Lead Plastic MSOP	0°C to 70°C
LT1807IMS8#PBF	LT1807IMS8#TRPBF	LTTV	8-Lead Plastic MSOP	-40°C to 85°C
LT1807CS8#PBF	LT1807CS8#TRPBF	1807	8-Lead Plastic SO	0°C to 70°C
LT1807IS8#PBF	LT1807IS8#TRPBF	1807I	8-Lead Plastic SO	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>

ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$. $V_S = 5\text{V}$, 0V ; $V_S = 3\text{V}$, 0V ; $V_{\text{SHDN}} = \text{open}$; $V_{\text{CM}} = V_{\text{OUT}} = \text{half supply}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{\text{CM}} = V^+$		100	550	μV
		$V_{\text{CM}} = V^-$		100	550	μV
		$V_{\text{CM}} = V^+$ (LT1806 SOT-23)		100	700	μV
		$V_{\text{CM}} = V^-$ (LT1806 SOT-23)		100	700	μV
ΔV_{OS}	Input Offset Voltage Shift	$V_{\text{CM}} = V^-$ to V^+		50	550	μV
		$V_{\text{CM}} = V^-$ to V^+ (LT1806 SOT-23)		100	700	μV
	Input Offset Voltage Match (Channel-to-Channel) (Note 10)	$V_{\text{CM}} = V^-$ to V^+		200	1000	μV
I_B	Input Bias Current	$V_{\text{CM}} = V^+$		1	4	μA
		$V_{\text{CM}} = V^- + 0.2\text{V}$	-13	-5		μA
ΔI_B	Input Bias Current Shift	$V_{\text{CM}} = V^-$ to V^+		6	17	μA
	Input Bias Current Match (Channel-to-Channel) (Note 10)	$V_{\text{CM}} = V^+$		0.03	1.2	μA
		$V_{\text{CM}} = V^- + 0.2\text{V}$		0.05	3.0	μA
I_{OS}	Input Offset Current	$V_{\text{CM}} = V^+$		0.03	0.6	μA
		$V_{\text{CM}} = V^- + 0.2\text{V}$		0.05	1.5	μA
ΔI_{OS}	Input Offset Current Shift	$V_{\text{CM}} = V^- + 0.2\text{V}$ to V^+		0.08	2.1	μA
	Input Noise Voltage	0.1Hz to 10Hz		800		$\text{nV}_{\text{P-P}}$
e_n	Input Noise Voltage Density	$f = 10\text{kHz}$		3.5		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f = 10\text{kHz}$		1.5		$\text{pA}/\sqrt{\text{Hz}}$
C_{IN}	Input Capacitance			2		pF
A_{VOL}	Large-Signal Voltage Gain	$V_S = 5\text{V}$, $V_O = 0.5\text{V}$ to 4.5V , $R_L = 1\text{k}$ to $V_S/2$	75	220		V/mV
		$V_S = 5\text{V}$, $V_O = 1\text{V}$ to 4V , $R_L = 100$ to $V_S/2$	9	22		V/mV
		$V_S = 3\text{V}$, $V_O = 0.5\text{V}$ to 2.5V , $R_L = 1\text{k}$ to $V_S/2$	60	150		V/mV
CMRR	Common Mode Rejection Ratio	$V_S = 5\text{V}$, $V_{\text{CM}} = V^-$ to V^+	79	100		dB
		$V_S = 3\text{V}$, $V_{\text{CM}} = V^-$ to V^+	74	95		dB
	CMRR Match (Channel-to-Channel) (Note 10)	$V_S = 5\text{V}$, $V_{\text{CM}} = V^-$ to V^+	73	100		dB
		$V_S = 3\text{V}$, $V_{\text{CM}} = V^-$ to V^+	68	95		dB
	Input Common Mode Range		V^-		V^+	V
PSRR	Power Supply Rejection Ratio	$V_S = 2.5\text{V}$ to 10V , $V_{\text{CM}} = 0\text{V}$	90	105		dB
		$V_S = 2.5\text{V}$ to 10V , $V_{\text{CM}} = 0\text{V}$	84	105		dB
		Minimum Supply Voltage (Note 6)		2.3	2.5	V
V_{OL}	Output Voltage Swing Low (Note 7)	No Load		8	50	mV
		$I_{\text{SINK}} = 5\text{mA}$		50	130	mV
		$I_{\text{SINK}} = 25\text{mA}$		170	375	mV
V_{OH}	Output Voltage Swing High (Note 7)	No Load		15	65	mV
		$I_{\text{SOURCE}} = 5\text{mA}$		85	180	mV
		$I_{\text{SOURCE}} = 25\text{mA}$		350	650	mV

ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$. $V_S = 5\text{V}$, 0V ; $V_S = 3\text{V}$, 0V ; $V_{\text{SHDN}} = \text{open}$; $V_{\text{CM}} = V_{\text{OUT}} = \text{half supply}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{SC}	Short-Circuit Current	$V_S = 5\text{V}$ $V_S = 3\text{V}$	± 35 ± 30	± 85 ± 65		mA mA
I_S	Supply Current per Amplifier			9	13	mA
	Disable Supply Current	$V_S = 5\text{V}$, $V_{\text{SHDN}} = 0.3\text{V}$ $V_S = 3\text{V}$, $V_{\text{SHDN}} = 0.3\text{V}$		0.40 0.22	0.9 0.7	mA mA
I_{SHDN}	SHDN Pin Current	$V_S = 5\text{V}$, $V_{\text{SHDN}} = 0.3\text{V}$ $V_S = 3\text{V}$, $V_{\text{SHDN}} = 0.3\text{V}$		150 100	350 300	μA μA
	Shutdown Output Leakage Current	$V_{\text{SHDN}} = 0.3\text{V}$		0.1	75	μA
V_L	SHDN Pin Input Voltage LOW				0.3	V
V_H	SHDN Pin Input Voltage HIGH		$V^+ - 0.5$			V
t_{ON}	Turn-On Time	$V_{\text{SHDN}} = 0.3\text{V}$ to 4.5V , $R_L = 100\Omega$		80		ns
t_{OFF}	Turn-Off Time	$V_{\text{SHDN}} = 4.5\text{V}$ to 0.3V , $R_L = 100\Omega$		50		ns
GBW	Gain-Bandwidth Product	Frequency = 6MHz		325		MHz
SR	Slew Rate	$V_S = 5\text{V}$, $A_V = -1$, $R_L = 1\text{k}$, $V_O = 4\text{V}$		125		V/ μs
FPBW	Full-Power Bandwidth	$V_S = 5\text{V}$, $V_{\text{OUT}} = 4V_{\text{P-P}}$		10		MHz
HD	Harmonic Distortion	$V_S = 5\text{V}$, $A_V = 1$, $R_L = 1\text{k}$, $V_O = 2V_{\text{P-P}}$, $f_C = 5\text{MHz}$		-78		dBc
t_S	Settling Time	0.01%, $V_S = 5\text{V}$, $V_{\text{STEP}} = 2\text{V}$, $A_V = 1$, $R_L = 1\text{k}$		60		ns
ΔG	Differential Gain (NTSC)	$V_S = 5\text{V}$, $A_V = 2$, $R_L = 150$		0.015		%
$\Delta\theta$	Differential Phase (NTSC)	$V_S = 5\text{V}$, $A_V = 2$, $R_L = 150$		0.05		Deg

The ● denotes the specifications which apply over the $0^\circ\text{C} < T_A < 70^\circ\text{C}$ temperature range. $V_S = 5\text{V}$, 0V ; $V_S = 3\text{V}$, 0V ; $V_{\text{SHDN}} = \text{open}$; $V_{\text{CM}} = V_{\text{OUT}} = \text{half supply}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{\text{CM}} = V^+$		200	700	μV
		$V_{\text{CM}} = V^-$		200	700	μV
		$V_{\text{CM}} = V^+$ (LT1806 SOT-23)		200	850	μV
		$V_{\text{CM}} = V^-$ (LT1806 SOT-23)		200	850	μV
$V_{\text{OS TC}}$	Input Offset Voltage Drift (Note 8)	$V_{\text{CM}} = V^+$		1.5	5	$\mu\text{V}/^\circ\text{C}$
		$V_{\text{CM}} = V^-$		1.5	5	$\mu\text{V}/^\circ\text{C}$
ΔV_{OS}	Input Offset Voltage Shift	$V_{\text{CM}} = V^-$ to V^+		100	700	μV
		$V_{\text{CM}} = V^-$ to V^+ (LT1806 SOT-23)		100	850	μV
	Input Offset Voltage Match (Channel-to-Channel) (Note 10)	$V_{\text{CM}} = V^-$, $V_{\text{CM}} = V^+$		300	1200	μV
I_B	Input Bias Current	$V_{\text{CM}} = V^+ - 0.2\text{V}$		1	5	μA
		$V_{\text{CM}} = V^- + 0.4\text{V}$	-15	-5		μA
ΔI_B	Input Bias Current Shift	$V_{\text{CM}} = V^- + 0.4\text{V}$ to $V^+ - 0.2\text{V}$		6	20	μA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the $0^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$ temperature range. $V_S = 5\text{V}$, 0V ; $V_S = 3\text{V}$, 0V ; $V_{\text{SHDN}} = \text{open}$; $V_{\text{CM}} = V_{\text{OUT}} = \text{half supply}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Input Bias Current Match (Channel-to-Channel) (Note 10)	$V_{\text{CM}} = V^+ - 0.2\text{V}$ $V_{\text{CM}} = V^- + 0.4\text{V}$	●	0.03	1.5	μA
			●	0.05	3.5	μA
I_{OS}	Input Offset Current	$V_{\text{CM}} = V^+ - 0.2\text{V}$ $V_{\text{CM}} = V^- + 0.4\text{V}$	●	0.03	0.75	μA
			●	0.05	1.80	μA
ΔI_{OS}	Input Offset Current Shift	$V_{\text{CM}} = V^- + 0.4\text{V}$ to $V^+ - 0.2\text{V}$	●	0.08	2.55	μA
A_{VOL}	Large-Signal Voltage Gain	$V_S = 5\text{V}$, $V_O = 0.5\text{V}$ to 4.5V , $R_L = 1\text{k}$ to $V_S/2$ $V_S = 5\text{V}$, $V_O = 1\text{V}$ to 4V , $R_L = 100\Omega$ to $V_S/2$ $V_S = 3\text{V}$, $V_O = 0.5\text{V}$ to 2.5V , $R_L = 1\text{k}$ to $V_S/2$	●	60	175	V/mV
			●	7.5	20	V/mV
			●	45	140	V/mV
CMRR	Common Mode Rejection Ratio	$V_S = 5\text{V}$, $V_{\text{CM}} = V^-$ to V^+ $V_S = 3\text{V}$, $V_{\text{CM}} = V^-$ to V^+	●	77	94	dB
			●	72	89	dB
	CMRR Match (Channel-to-Channel) (Note 10)	$V_S = 5\text{V}$, $V_{\text{CM}} = V^-$ to V^+ $V_S = 3\text{V}$, $V_{\text{CM}} = V^-$ to V^+	●	71	94	dB
			●	66	89	dB
	Input Common Mode Range		●	V^-	V^+	V
PSRR	Power Supply Rejection Ratio	$V_S = 2.5\text{V}$ to 10V , $V_{\text{CM}} = 0\text{V}$	●	88	105	dB
	PSRR Match (Channel-to-Channel) (Note 10)	$V_S = 2.5\text{V}$ to 10V , $V_{\text{CM}} = 0\text{V}$	●	82	105	dB
	Minimum Supply Voltage (Note 6)	$V_{\text{CM}} = V_O = 0.5\text{V}$	●	2.3	2.5	V
V_{OL}	Output Voltage Swing Low (Note 7)	No Load $I_{\text{SINK}} = 5\text{mA}$ $I_{\text{SINK}} = 25\text{mA}$	●	12	60	mV
			●	60	140	mV
			●	180	425	mV
V_{OH}	Output Voltage Swing High (Note 7)	No Load $I_{\text{SOURCE}} = 5\text{mA}$ $I_{\text{SOURCE}} = 25\text{mA}$	●	30	120	mV
			●	110	220	mV
			●	360	700	mV
I_{SC}	Short-Circuit Current	$V_S = 5\text{V}$ $V_S = 3\text{V}$	●	± 30	± 65	mA
			●	± 25	± 55	mA
I_S	Supply Current per Amplifier		●	10	14	mA
	Disable Supply Current	$V_S = 5\text{V}$, $V_{\text{SHDN}} = 0.3\text{V}$ $V_S = 3\text{V}$, $V_{\text{SHDN}} = 0.3\text{V}$	●	0.40	1.1	mA
			●	0.22	0.9	mA
I_{SHDN}	SHDN Pin Current	$V_S = 5\text{V}$, $V_{\text{SHDN}} = 0.3\text{V}$ $V_S = 3\text{V}$, $V_{\text{SHDN}} = 0.3\text{V}$	●	160	400	μA
			●	110	350	μA
	Shutdown Output Leakage Current	$V_{\text{SHDN}} = 0.3\text{V}$	●	1		μA
V_L	SHDN Pin Input Voltage Low		●		0.3	V
V_H	SHDN Pin Input Voltage High		●	$V^+ - 0.5$		V
t_{ON}	Turn-On Time	$V_{\text{SHDN}} = 0.3\text{V}$ to 4.5V , $R_L = 100\Omega$	●	80		ns
t_{OFF}	Turn-Off Time	$V_{\text{SHDN}} = 4.5\text{V}$ to 0.3V , $R_L = 100\Omega$	●	50		ns
GBW	Gain-Bandwidth Product	Frequency = 6MHz	●	300		MHz
SR	Slew Rate	$V_S = 5\text{V}$, $A_V = -1$, $R_L = 1\text{k}$, $V_O = 4\text{V}$	●	100		$\text{V}/\mu\text{s}$
FPBW	Full-Power Bandwidth	$V_S = 5\text{V}$, $V_O = 4\text{V}_{\text{P-P}}$	●	8		MHz

LT1806/LT1807

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$ temperature range. $V_S = 5\text{V}$, 0V ; $V_S = 3\text{V}$, 0V ; $V_{\text{SHDN}} = \text{open}$; $V_{\text{CM}} = V_{\text{OUT}} = \text{half supply}$, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{\text{CM}} = V^+$	●	200	800	μV
		$V_{\text{CM}} = V^-$	●	200	800	μV
		$V_{\text{CM}} = V^+$ (LT1806 SOT-23)	●	200	950	μV
		$V_{\text{CM}} = V^-$ (LT1806 SOT-23)	●	200	950	μV
$V_{\text{OS TC}}$	Input Offset Voltage Drift (Note 8)	$V_{\text{CM}} = V^+$	●	1.5	5	$\mu\text{V}/^{\circ}\text{C}$
		$V_{\text{CM}} = V^-$	●	1.5	5	$\mu\text{V}/^{\circ}\text{C}$
ΔV_{OS}	Input Offset Voltage Shift	$V_{\text{CM}} = V^- \text{ to } V^+$	●	100	800	μV
		$V_{\text{CM}} = V^- \text{ to } V^+$ (LT1806 SOT-23)	●	100	950	μV
	Input Offset Voltage Match (Channel-to-Channel) (Note 10)	$V_{\text{CM}} = V^-$, $V_{\text{CM}} = V^+$	●	200	1400	μV
I_B	Input Bias Current	$V_{\text{CM}} = V^+ - 0.2\text{V}$	●	1	6	μA
		$V_{\text{CM}} = V^- + 0.4\text{V}$	●	-16	-5	μA
ΔI_B	Input Bias Current Shift	$V_{\text{CM}} = V^- + 0.4\text{V} \text{ to } V^+ - 0.2\text{V}$	●	6	22	μA
	Input Bias Current Match (Channel-to-Channel) (Note 10)	$V_{\text{CM}} = V^+ - 0.2\text{V}$	●	0.02	1.8	μA
		$V_{\text{CM}} = V^- + 0.4\text{V}$	●	0.05	4	μA
I_{OS}	Input Offset Current	$V_{\text{CM}} = V^+ - 0.2\text{V}$	●	0.02	0.9	μA
		$V_{\text{CM}} = V^- + 0.4\text{V}$	●	0.05	2.1	μA
ΔI_{OS}	Input Offset Current Shift	$V_{\text{CM}} = V^- + 0.4\text{V} \text{ to } V^+ - 0.2\text{V}$	●	0.07	3	μA
A_{VOL}	Large-Signal Voltage Gain	$V_S = 5\text{V}$, $V_O = 0.5\text{V} \text{ to } 4.5\text{V}$, $R_L = 1\text{k} \text{ to } V_S/2$	●	50	140	V/mV
		$V_S = 5\text{V}$, $V_O = 1\text{V} \text{ to } 4\text{V}$, $R_L = 100\Omega \text{ to } V_S/2$	●	6	16	V/mV
		$V_S = 3\text{V}$, $V_O = 0.5\text{V} \text{ to } 2.5\text{V}$, $R_L = 1\text{k} \text{ to } V_S/2$	●	35	100	V/mV
CMRR	Common Mode Rejection Ratio	$V_S = 5\text{V}$, $V_{\text{CM}} = V^- \text{ to } V^+$	●	75	94	dB
		$V_S = 3\text{V}$, $V_{\text{CM}} = V^- \text{ to } V^+$	●	71	89	dB
	CMRR Match (Channel-to-Channel) (Note 10)	$V_S = 5\text{V}$, $V_{\text{CM}} = V^- \text{ to } V^+$	●	69	94	dB
		$V_S = 3\text{V}$, $V_{\text{CM}} = V^- \text{ to } V^+$	●	65	89	dB
	Input Common Mode Range		●	V^-	V^+	V
PSRR	Power Supply Rejection Ratio	$V_S = 2.5\text{V} \text{ to } 10\text{V}$, $V_{\text{CM}} = 0\text{V}$	●	86	105	dB
		$V_S = 2.5\text{V} \text{ to } 10\text{V}$, $V_{\text{CM}} = 0\text{V}$	●	80	105	dB
	Minimum Supply Voltage (Note 6)	$V_{\text{CM}} = V_O = 0.5\text{V}$	●	2.3	2.5	V
V_{OL}	Output Voltage Swing Low (Note 7)	No Load	●	15	70	mV
		$I_{\text{SINK}} = 5\text{mA}$	●	65	150	mV
		$I_{\text{SINK}} = 20\text{mA}$	●	170	400	mV
V_{OH}	Output Voltage Swing High (Note 7)	No Load	●	30	130	mV
		$I_{\text{SOURCE}} = 5\text{mA}$	●	110	240	mV
		$I_{\text{SOURCE}} = 20\text{mA}$	●	350	700	mV
I_{SC}	Short-Circuit Current	$V_S = 5\text{V}$	●	± 22	± 45	mA
		$V_S = 3\text{V}$	●	± 20	± 40	mA
I_S	Supply Current per Amplifier		●	11	16	mA
			●	0.4	1.2	mA
	Disable Supply Current	$V_S = 5\text{V}$, $V_{\text{SHDN}} = 0.3\text{V}$	●	0.3	1	mA
		$V_S = 3\text{V}$, $V_{\text{SHDN}} = 0.3\text{V}$	●			mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$ temperature range. $V_S = 5\text{V}$, 0V ; $V_S = 3\text{V}$, 0V ; $V_{\text{SHDN}} = \text{open}$; $V_{\text{CM}} = V_{\text{OUT}} = \text{half supply}$, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{SHDN}	SHDN Pin Current	$V_S = 5\text{V}$, $V_{\text{SHDN}} = 0.3\text{V}$ $V_S = 3\text{V}$, $V_{\text{SHDN}} = 0.3\text{V}$	●	170 120	450 400	μA μA
	Shutdown Output Leakage Current	$V_{\text{SHDN}} = 0.3\text{V}$	●	1.2		μA
V_L	SHDN Pin Input Voltage Low		●		0.3	V
V_H	SHDN Pin Input Voltage High		●	$V^+ - 0.5$		V
t_{ON}	Turn-On Time	$V_{\text{SHDN}} = 0.3\text{V}$ to 4.5V , $R_L = 100\Omega$	●	80		ns
t_{OFF}	Turn-Off Time	$V_{\text{SHDN}} = 4.5\text{V}$ to 0.3V , $R_L = 100\Omega$	●	50		ns
GBW	Gain-Bandwidth Product	Frequency = 6MHz	●	250		MHz
SR	Slew Rate	$V_S = 5\text{V}$, $A_V = -1$, $R_L = 1\text{k}$, $V_O = 4\text{V}$	●	80		V/ μs
FPBW	Full-Power Bandwidth	$V_S = 5\text{V}$, $V_O = 4V_{\text{P-P}}$	●	6		MHz

$T_A = 25^{\circ}\text{C}$. $V_S = \pm 5\text{V}$, $V_{\text{SHDN}} = \text{open}$; $V_{\text{CM}} = 0\text{V}$, $V_{\text{OUT}} = 0\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{\text{CM}} = V^+$ $V_{\text{CM}} = V^-$ $V_{\text{CM}} = V^+$ (LT1806 SOT-23) $V_{\text{CM}} = V^-$ (LT1806 SOT-23)		100 100 100 100	700 700 750 750	μV μV μV μV
ΔV_{OS}	Input Offset Voltage Shift	$V_{\text{CM}} = V^-$ to V^+ $V_{\text{CM}} = V^-$ to V^+ (LT1806 SOT-23)		50 50	700 750	μV μV
	Input Offset Voltage Match (Channel-to-Channel) (Note 10)	$V_{\text{CM}} = V^-$, $V_{\text{CM}} = V^+$		200	1200	μV
I_B	Input Bias Current	$V_{\text{CM}} = V^+$ $V_{\text{CM}} = V^- + 0.2\text{V}$	-14	1 -5	5	μA μA
ΔI_B	Input Bias Current Shift	$V_{\text{CM}} = V^- + 0.2\text{V}$ to V^+		6	19	μA
	Input Bias Current Match (Channel-to-Channel) (Note 10)	$V_{\text{CM}} = V^+$ $V_{\text{CM}} = V^- + 0.2\text{V}$		0.03 0.05	1.4 3.2	μA μA
I_{OS}	Input Offset Current	$V_{\text{CM}} = V^+$ $V_{\text{CM}} = V^- + 0.2\text{V}$		0.03 0.04	0.7 1.6	μA μA
ΔI_{OS}	Input Offset Current Shift	$V_{\text{CM}} = V^- + 0.2\text{V}$ to V^+		0.07	2.3	μA
	Input Noise Voltage	0.1Hz to 10Hz		800		nVp-p
e_n	Input Noise Voltage Density	$f = 10\text{kHz}$		3.5		nV/ $\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	$f = 10\text{kHz}$		1.5		pA/ $\sqrt{\text{Hz}}$
C_{IN}	Input Capacitance	$f = 10\text{kHz}$		2		pF
A_{VOL}	Large-Signal Voltage Gain	$V_O = -4\text{V}$ to 4V , $R_L = 1\text{k}$ $V_O = -2.5\text{V}$ to 2.5V , $R_L = 100\Omega$	100 10	300 27		V/mV V/mV

ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$. $V_S = \pm 5\text{V}$, $V_{\text{SHDN}} = \text{open}$; $V_{\text{CM}} = 0\text{V}$, $V_{\text{OUT}} = 0\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = V^- \text{ to } V^+$	83	106		dB
	CMRR Match (Channel-to-Channel) (Note 10)	$V_{\text{CM}} = V^- \text{ to } V^+$	77	106		dB
	Input Common Mode Range		V^-		V^+	V
PSRR	Power Supply Rejection Ratio	$V^+ = 2.5\text{V to } 10\text{V}$, $V^- = 0\text{V}$	90	105		dB
	PSRR Match (Channel-to-Channel) (Note 10)	$V^+ = 2.5\text{V to } 10\text{V}$, $V^- = 0\text{V}$	84	105		dB
V_{OL}	Output Voltage Swing Low (Note 7)	No Load		14	60	mV
		$I_{\text{SINK}} = 5\text{mA}$		55	140	mV
		$I_{\text{SINK}} = 25\text{mA}$		180	450	mV
V_{OH}	Output Voltage Swing High (Note 7)	No Load		20	70	mV
		$I_{\text{SOURCE}} = 5\text{mA}$		90	200	mV
		$I_{\text{SOURCE}} = 25\text{mA}$		360	700	mV
I_{SC}	Short-Circuit Current		± 40	± 85		mA
I_S	Supply Current per Amplifier			11	16	mA
	Disable Supply Current	$V_{\text{SHDN}} = 0.3\text{V}$		0.4	1.2	mA
I_{SHDN}	SHDN Pin Current	$V_{\text{SHDN}} = 0.3\text{V}$		150	350	μA
	Shutdown Output Leakage Current	$V_{\text{SHDN}} = 0.3\text{V}$		0.3	75	μA
V_L	SHDN Pin Input Voltage Low				0.3	V
V_H	SHDN Pin Input Voltage High		$V^+ - 0.5$			V
t_{ON}	Turn-On Time	$V_{\text{SHDN}} = 0.3\text{V to } 4.5\text{V}$, $R_L = 100\Omega$		80		ns
t_{OFF}	Turn-Off Time	$V_{\text{SHDN}} = 4.5\text{V to } 0.3\text{V}$, $R_L = 100\Omega$		50		ns
GBW	Gain-Bandwidth Product	Frequency = 6MHz	170	325		MHz
SR	Slew Rate	$A_V = -1$, $R_L = 1\text{k}$, $V_O = \pm 4\text{V}$, Measured at $V_O = \pm 3\text{V}$	70	140		V/ μs
FPBW	Full-Power Bandwidth	$V_O = 8V_{\text{P-P}}$		5.5		MHz
HD	Harmonic Distortion	$A_V = 1$, $R_L = 1\text{k}$, $V_O = 2V_{\text{P-P}}$, $f_C = 5\text{MHz}$		-80		dBc
t_S	Settling Time	0.01%, $V_{\text{STEP}} = 8\text{V}$, $A_V = 1$, $R_L = 1\text{k}$		120		ns
ΔG	Differential Gain (NTSC)	$A_V = 2$, $R_L = 150$		0.01		%
$\Delta \theta$	Differential Phase (NTSC)	$A_V = 2$, $R_L = 150$		0.01		Deg

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the $0^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$ temperature range. $V_S = \pm 5\text{V}$, $V_{\text{SHDN}} = \text{open}$; $V_{\text{CM}} = 0\text{V}$, $V_{\text{OUT}} = 0\text{V}$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{\text{CM}} = V^+$	●	200	800	μV
		$V_{\text{CM}} = V^-$	●	200	800	μV
		$V_{\text{CM}} = V^+$ (LT1806 SOT-23)	●	200	900	μV
		$V_{\text{CM}} = V^-$ (LT1806 SOT-23)	●	200	900	μV
$V_{\text{OS TC}}$	Input Offset Voltage Drift (Note 8)	$V_{\text{CM}} = V^+$	●	1.5	5	$\mu\text{V}/^{\circ}\text{C}$
		$V_{\text{CM}} = V^-$	●	1.5	5	$\mu\text{V}/^{\circ}\text{C}$
ΔV_{OS}	Input Offset Voltage Shift	$V_{\text{CM}} = V^-$ to V^+	●	100	800	μV
		$V_{\text{CM}} = V^-$ to V^+ (LT1806 SOT-23)	●	100	900	μV
	Input Offset Voltage Match (Channel-to-Channel) (Note 10)	$V_{\text{CM}} = V^-$, $V_{\text{CM}} = V^+$	●	300	1400	μV
I_B	Input Bias Current	$V_{\text{CM}} = V^+ - 0.2\text{V}$	●	1	6	μA
		$V_{\text{CM}} = V^- + 0.4\text{V}$	●	-15	-6	μA
ΔI_B	Input Bias Current Shift	$V_{\text{CM}} = V^- + 0.4\text{V}$ to $V^+ - 0.2\text{V}$	●	7	21	μA
	Input Bias Current Match (Channel-to-Channel) (Note 10)	$V_{\text{CM}} = V^+ - 0.2\text{V}$	●	0.03	1.8	μA
		$V_{\text{CM}} = V^- + 0.4\text{V}$	●	0.04	3.8	μA
I_{OS}	Input Offset Current	$V_{\text{CM}} = V^+ - 0.2\text{V}$	●	0.03	0.9	μA
		$V_{\text{CM}} = V^- + 0.4\text{V}$	●	0.04	1.9	μA
ΔI_{OS}	Input Offset Current Shift	$V_{\text{CM}} = V^- + 0.4\text{V}$ to $V^+ - 0.2\text{V}$	●	0.07	2.8	μA
A_{VOL}	Large-Signal Voltage Gain	$V_O = -4\text{V}$ to 4V , $R_L = 1\text{k}$	●	80	250	V/mV
		$V_O = -2.5\text{V}$ to 2.5V , $R_L = 100\Omega$	●	8	25	V/mV
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = V^-$ to V^+	●	81	100	dB
	CMRR Match (Channel-to-Channel) (Note 10)	$V_{\text{CM}} = V^-$ to V^+	●	75	100	dB
	Input Common Mode Range		●	V^-	V^+	V
PSRR	Power Supply Rejection Ratio	$V^+ = 2.5\text{V}$ to 10V , $V^- = 0\text{V}$	●	88	105	dB
	PSRR Match (Channel-to-Channel) (Note 10)	$V^+ = 2.5\text{V}$ to 10V , $V^- = 0\text{V}$	●	82	106	dB
V_{OL}	Output Voltage Swing Low (Note 7)	No Load	●	18	80	mV
		$I_{\text{SINK}} = 5\text{mA}$	●	60	160	mV
		$I_{\text{SINK}} = 25\text{mA}$	●	185	500	mV
V_{OH}	Output Voltage Swing High (Note 7)	No Load	●	40	140	mV
		$I_{\text{SOURCE}} = 5\text{mA}$	●	110	240	mV
		$I_{\text{SOURCE}} = 25\text{mA}$	●	360	750	mV
I_{SC}	Short-Circuit Current		●	± 35	± 75	mA
I_S	Supply Current per Amplifier		●	14	20	mA
	Disable Supply Current	$V_{\text{SHDN}} = 0.3\text{V}$	●	0.4	1.4	mA
I_{SHDN}	SHDN Pin Current	$V_{\text{SHDN}} = 0.3\text{V}$	●	160	400	μA
	Shutdown Output Leakage Current	$V_{\text{SHDN}} = 0.3\text{V}$	●	1		μA
V_L	SHDN Pin Input Voltage Low		●		0.3	V
V_H	SHDN Pin Input Voltage High		●	$V^+ - 0.5$		V
t_{ON}	Turn-On Time	$V_{\text{SHDN}} = 0.3\text{V}$ to 4.5V , $R_L = 100\Omega$	●	80		ns
t_{OFF}	Turn-Off Time	$V_{\text{SHDN}} = 4.5\text{V}$ to 0.3V , $R_L = 100\Omega$	●	50		ns
GBW	Gain-Bandwidth Product	Frequency = 6MHz	●	150	300	MHz
SR	Slew Rate	$A_V = -1$, $R_L = 1\text{k}$, $V_O = \pm 4\text{V}$, Measure at $V_O = \pm 3\text{V}$	●	60	120	$\text{V}/\mu\text{s}$
FPBW	Full-Power Bandwidth	$V_O = 8V_{\text{P-P}}$	●	4.5		MHz

LT1806/LT1807

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$ temperature range. $V_S = \pm 5\text{V}$, $V_{\text{SHDN}} = \text{open}$; $V_{\text{CM}} = 0\text{V}$, $V_{\text{OUT}} = 0\text{V}$, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{\text{CM}} = V^+$	●	200	900	μV
		$V_{\text{CM}} = V^-$	●	200	900	μV
		$V_{\text{CM}} = V^+$ (LT1806 SOT-23)	●	200	975	μV
		$V_{\text{CM}} = V^-$ (LT1806 SOT-23)	●	200	975	μV
$V_{\text{OS TC}}$	Input Offset Voltage Drift (Note 8)	$V_{\text{CM}} = V^+$	●	1.5	5	$\mu\text{V}/^{\circ}\text{C}$
		$V_{\text{CM}} = V^-$	●	1.5	5	$\mu\text{V}/^{\circ}\text{C}$
ΔV_{OS}	Input Offset Voltage Shift	$V_{\text{CM}} = V^-$ to V^+	●	100	900	μV
		$V_{\text{CM}} = V^-$ to V^+ (LT1806 SOT-23)	●	100	975	μV
	Input Offset Voltage Match (Channel-to-Channel) (Note 10)	$V_{\text{CM}} = V^-$, $V_{\text{CM}} = V^+$	●	300	1600	μV
I_B	Input Bias Current	$V_{\text{CM}} = V^+ - 0.2\text{V}$	●	1.2	7	μA
		$V_{\text{CM}} = V^- + 0.4\text{V}$	●	-16	-5	μA
ΔI_B	Input Bias Current Shift	$V_{\text{CM}} = V^- + 0.4\text{V}$ to $V^+ - 0.2\text{V}$	●	6	23	μA
	Input Bias Current Match (Channel-to-Channel) (Note 10)	$V_{\text{CM}} = V^+ - 0.2\text{V}$	●	0.03	2	μA
		$V_{\text{CM}} = V^- + 0.4\text{V}$	●	0.04	4.5	μA
I_{OS}	Input Offset Current	$V_{\text{CM}} = V^+ - 0.2\text{V}$	●	0.03	1.0	μA
		$V_{\text{CM}} = V^- + 0.4\text{V}$	●	0.04	2.2	μA
ΔI_{OS}	Input Offset Current Shift	$V_{\text{CM}} = V^- + 0.4\text{V}$ to $V^+ - 0.2\text{V}$	●	0.07	3.2	μA
A_{VOL}	Large-Signal Voltage Gain	$V_O = -4\text{V}$ to 4V , $R_L = 1\text{k}$	●	60	175	V/mV
		$V_O = -2\text{V}$ to 2V , $R_L = 100\Omega$	●	7	17	V/mV
CMRR	Common Mode Rejection Ratio	$V_{\text{CM}} = V^-$ to V^+	●	80	100	dB
	CMRR Match (Channel-to-Channel) (Note 10)	$V_{\text{CM}} = V^-$ to V^+	●	74	100	dB
	Input Common Mode Range		●	V^-	V^+	V
PSRR	Power Supply Rejection Ratio	$V^+ = 2.5\text{V}$ to 10V , $V^- = 0\text{V}$	●	86	105	dB
	PSRR Match (Channel-to-Channel) (Note 10)		●	80	105	dB
V_{OL}	Output Voltage Swing Low (Note 7)	No Load	●	20	100	mV
		$I_{\text{SINK}} = 5\text{mA}$	●	65	170	mV
		$I_{\text{SINK}} = 20\text{mA}$	●	200	500	mV
V_{OH}	Output Voltage Swing High (Note 7)	No Load	●	50	160	mV
		$I_{\text{SOURCE}} = 5\text{mA}$	●	115	260	mV
		$I_{\text{SOURCE}} = 20\text{mA}$	●	360	700	mV
I_{SC}	Short-Circuit Current		●	± 25	± 55	mA
I_S	Supply Current per Amplifier		●	15	22	mA
	Disable Supply Current	$V_{\text{SHDN}} = 0.3\text{V}$	●	0.45	1.5	mA
I_{SHDN}	SHDN Pin Current	$V_{\text{SHDN}} = 0.3\text{V}$	●	170	400	μA
	Shutdown Output Leakage Current	$V_{\text{SHDN}} = 0.3\text{V}$	●	1.2		μA
V_L	SHDN Pin Input Voltage Low		●		0.3	V
V_H	SHDN Pin Input Voltage High		●	$V^+ - 0.5$		V
t_{ON}	Turn-On Time	$V_{\text{SHDN}} = 0.3\text{V}$ to 4.5V , $R_L = 100\Omega$	●	80		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the $-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$ temperature range. $V_S = \pm 5\text{V}$, $V_{\text{SHDN}} = \text{open}$; $V_{\text{CM}} = 0\text{V}$, $V_{\text{OUT}} = 0\text{V}$, unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{OFF}	Turn-Off Time	$V_{\text{SHDN}} = 4.5\text{V}$ to 0.3V , $R_L = 100\Omega$	●	50		ns
GBW	Gain-Bandwidth Product	Frequency = 6MHz	●	125	290	MHz
SR	Slew Rate	$A_V = -1$, $R_L = 1\text{k}$, $V_O = \pm 4\text{V}$, Measure at $V_O = \pm 3\text{V}$	●	50	100	V/ μs
FPBW	Full-Power Bandwidth	$V_O = 8V_{\text{P-P}}$	●	4		MHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by back-to-back diodes. If the differential input voltage exceeds 1.4V, the input current should be limited to less than 10mA. This parameter is guaranteed to meet specified performance through design and/or characterization. It is not 100% tested.

Note 3: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 4: The LT1806C/LT1806I and LT1807C/LT1807I are guaranteed functional over the temperature range of -40°C and 85°C .

Note 5: The LT1806C/LT1807C are guaranteed to meet specified performance from 0°C to 70°C . The LT1806C/LT1807C are designed,

characterized and expected to meet specified performance from -40°C to 85°C but are not tested or QA sampled at these temperatures. The LT1806I/LT1807I are guaranteed to meet specified performance from -40°C to 85°C .

Note 6: Minimum supply voltage is guaranteed by power supply rejection ratio test.

Note 7: Output voltage swings are measured between the output and power supply rails.

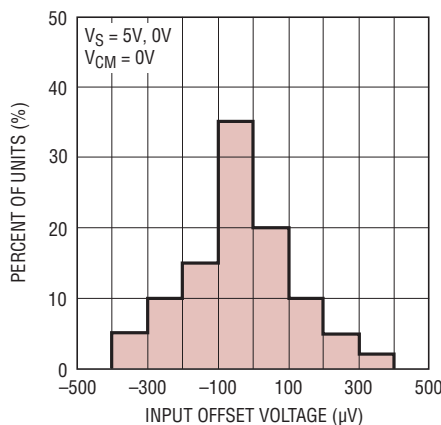
Note 8: This parameter is not 100% tested.

Note 9: Thermal resistance varies depending upon the amount of PC board metal attached to the V^- pin of the device. θ_{JA} is specified for a certain amount of 2oz copper metal trace connecting to the V^- pin as described in the thermal resistance tables in the Applications Information section.

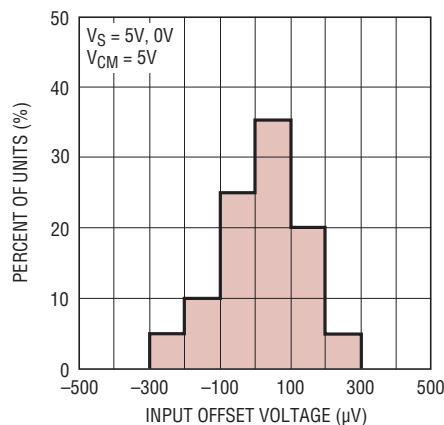
Note 10: Matching parameters are the difference between the two amplifiers of the LT1807.

TYPICAL PERFORMANCE CHARACTERISTICS

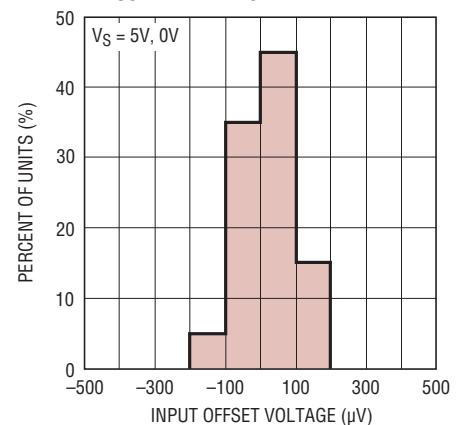
V_{OS} Distribution, $V_{\text{CM}} = 0\text{V}$
(PNP Stage)



V_{OS} Distribution, $V_{\text{CM}} = 5\text{V}$
(NPN Stage)

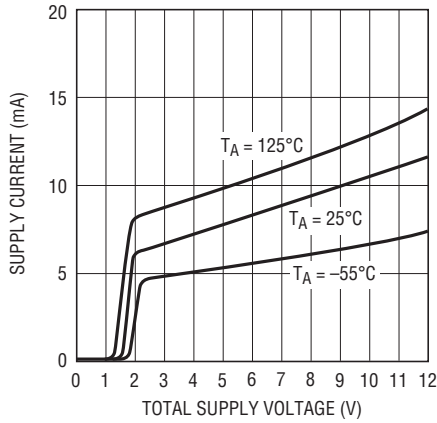


ΔV_{OS} Shift for $V_{\text{CM}} = 0\text{V}$ to 5V



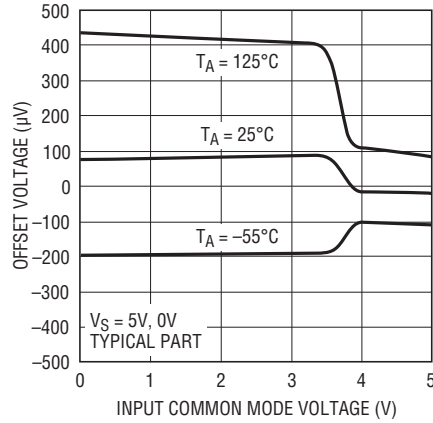
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current per Amp vs Supply Voltage



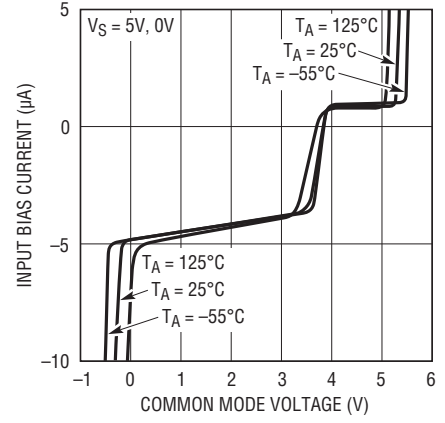
18067 G04

Offset Voltage vs Input Common Mode



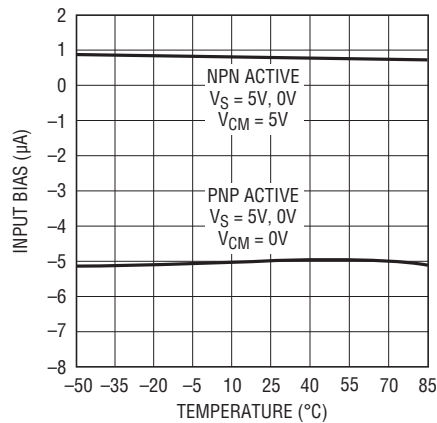
18067 G05

Input Bias Current vs Common Mode Voltage



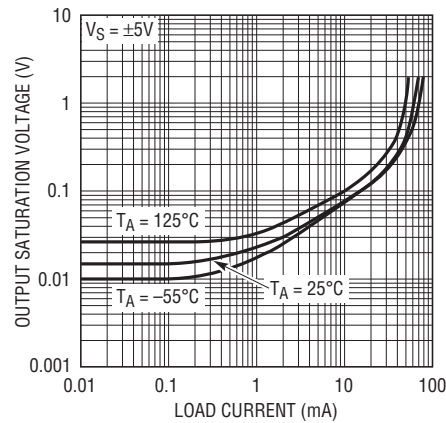
18067 G06

Input Bias Current vs Temperature



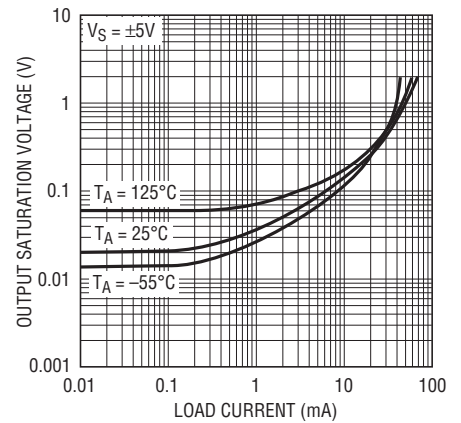
18067 G07

Output Saturation Voltage vs Load Current (Output Low)



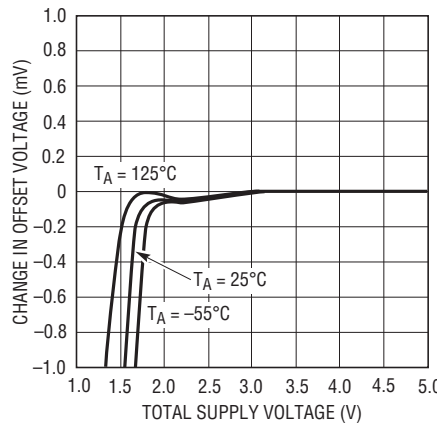
18067 G08

Output Saturation Voltage vs Load Current (Output High)



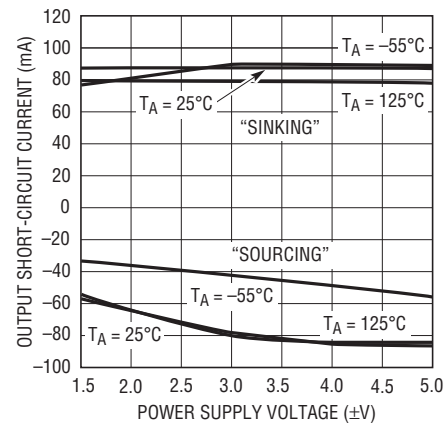
18067 G09

Minimum Supply Voltage



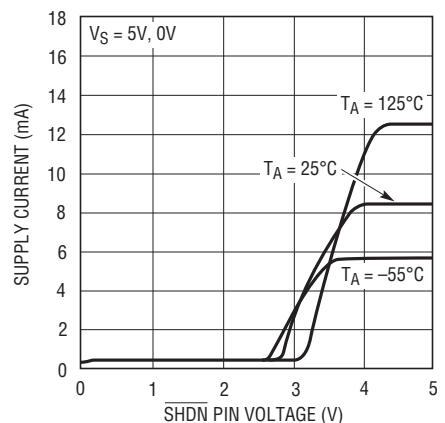
18067 G10

Output Short-Circuit Current vs Power Supply Voltage



18067 G11

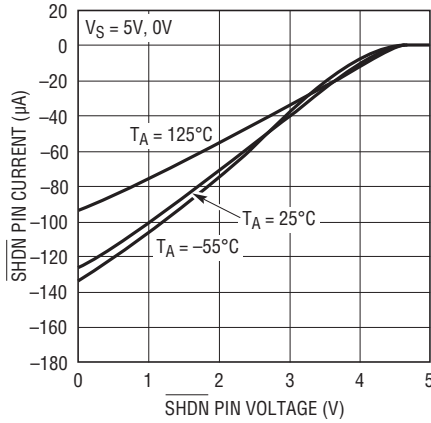
Supply Current vs SHDN Pin Voltage



18067 G12

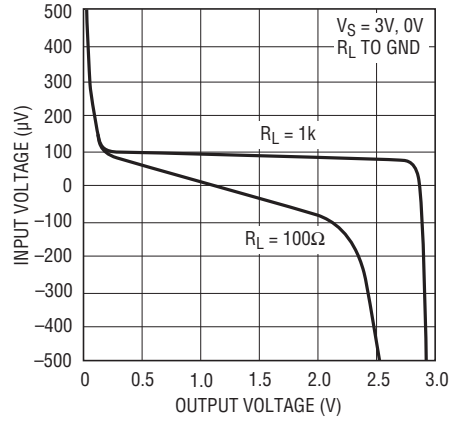
TYPICAL PERFORMANCE CHARACTERISTICS

SHDN Pin Current vs SHDN Pin Voltage



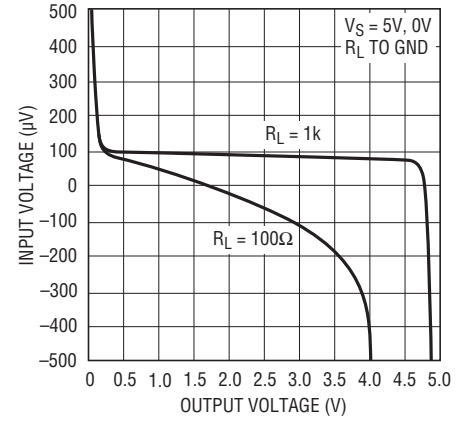
18067 G13

Open-Loop Gain



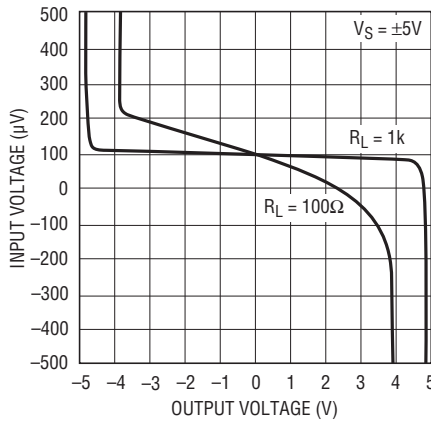
18067 G14

Open-Loop Gain



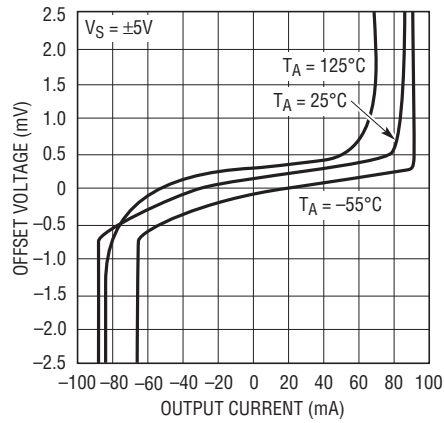
18067 G15

Open-Loop Gain



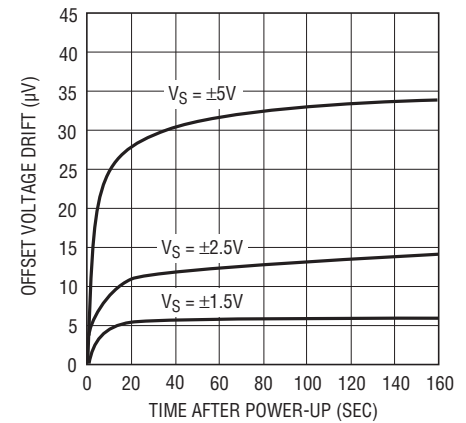
18067 G16

Offset Voltage vs Output Current



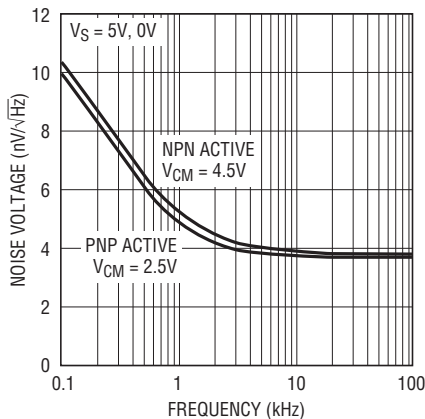
18067 G17

Warm-Up Drift vs Time (LT1806S8)



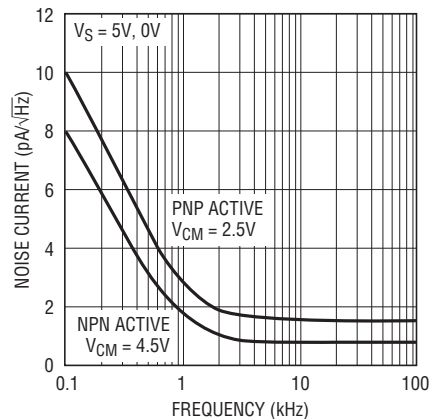
18067 G18

Input Noise Voltage vs Frequency



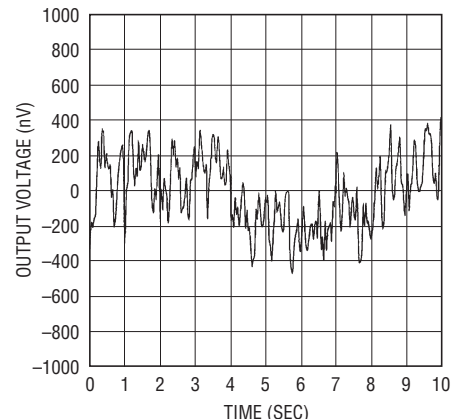
18067 G19

Input Noise Current vs Frequency



18067 G19

0.1Hz to 10Hz Output Voltage Noise



18067 G21

$T_A = 25^\circ\text{C}$

PHASE MARGIN

GAIN BANDWIDTH PRODUCT

Y-axis: GAIN BANDWIDTH (MHz) (200 to 55)

X-axis: TOTAL SUPPLY VOLTAGE (V) (0 to 10)

Total Supply Voltage (V)	Phase Margin (MHz)	Gain Bandwidth Product (MHz)
2.5	33	335
3.0	35	340
4.0	38	345
5.0	41	350
6.0	44	355
7.0	47	358
8.0	49	360
9.0	50	362
10.0	51	365

Figure 10 is a line graph showing the relationship between Temperature (°C) and two performance metrics: Phase Margin (deg) and GBW Product (MHz). The x-axis represents Temperature (°C) from -55 to 125. The y-axis represents both Phase Margin (deg) and GBW Product (MHz) from 200 to 500. The graph is divided into two main sections: the top section for Phase Margin and the bottom section for GBW Product. Each section contains two curves: one for $V_S = \pm 5V$ and one for $V_S = 3V$. The Phase Margin curves are relatively flat, with the $V_S = \pm 5V$ curve around 480-500 degrees and the $V_S = 3V$ curve around 320-340 degrees. The GBW Product curves show a more significant change, with the $V_S = \pm 5V$ curve increasing from approximately 300 MHz at -55°C to 350 MHz at 125°C, and the $V_S = 3V$ curve increasing from approximately 280 MHz at -55°C to 330 MHz at 125°C.

Temperature (°C)	Phase Margin (deg) $V_S = \pm 5V$	Phase Margin (deg) $V_S = 3V$	GBW Product (MHz) $V_S = \pm 5V$	GBW Product (MHz) $V_S = 3V$
-55	~480	~320	~300	~280
-35	~480	~320	~300	~280
-15	~480	~320	~310	~290
5	~480	~320	~340	~320
25	~480	~320	~350	~330
45	~480	~320	~350	~330
65	~480	~320	~350	~330
85	~480	~320	~350	~330
105	~480	~320	~350	~330
125	~480	~320	~350	~330

$A_V = -1$
 $R_F = R_G = 1k$
 $R_L = 1k$

$V_S = \pm 5V$
 $V_S = \pm 2.5V$

PHASE MARGIN (DEG)
 TEMPERATURE (°C)

Figure 10 is a graph showing the frequency response of the common-emitter amplifier. The y-axis is labeled "GAIN (dB)" and ranges from -9 to 21. The x-axis is labeled "FREQUENCY (MHz)" and is on a logarithmic scale from 0.1 to 500. The curve shows a flat gain of approximately 6 dB at low frequencies, a peak gain of about 10.5 dB at 50 MHz, and a roll-off to -9 dB at 500 MHz. Annotations include $C_L = 10\text{ pF}$, $R_L = 100\ \Omega$, $V_S = \pm 5\text{ V}$, and $V_S = 3\text{ V}$.

Figure 10 is a log-log plot showing the output impedance of the 741 op amp as a function of frequency and closed-loop gain. The y-axis represents Output Impedance (Z) in ohms, ranging from 0.001 to 600. The x-axis represents Frequency (Hz), ranging from 100k to 500M. Three curves are plotted for different closed-loop gains: $A_V = 2$, $A_V = 10$, and $A_V = 1$. The curves show that output impedance increases with frequency and decreases with higher closed-loop gain. The plot is for $V_S = 5V, 0V$.

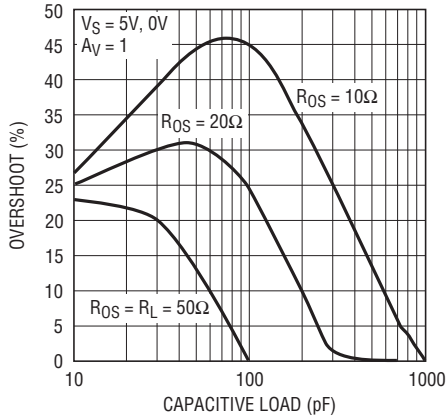
Figure 10 is a graph showing the Common Mode Rejection Ratio (CMRR) in dB versus Frequency in MHz for the 741 op amp. The y-axis is labeled "COMMON MODE REJECTION RATIO (dB)" and ranges from 0 to 100 in increments of 10. The x-axis is labeled "FREQUENCY (MHz)" and is a logarithmic scale ranging from 0.01 to 500. The curve starts at approximately 98 dB at 0.01 MHz and decreases to 0 dB at 500 MHz. A note in the upper right corner indicates $V_S = 5V, 0V$.

Figure 1 is a log-log plot showing the Power Supply Rejection Ratio (PSRR) in dB versus Frequency in MHz. The y-axis ranges from 0 to 100 dB, and the x-axis ranges from 0.001 to 100 MHz. Two curves are plotted: one for the Positive Supply and one for the Negative Supply. Both curves show a peak in PSRR around 0.05 MHz. The Positive Supply curve starts at approximately 92 dB at 0.001 MHz, peaks at 90 dB at 0.05 MHz, and then decreases to 0 dB at 100 MHz. The Negative Supply curve starts at approximately 88 dB at 0.001 MHz, peaks at 85 dB at 0.05 MHz, and then decreases to 0 dB at 100 MHz. The operating conditions are $V_S = 5V, 0V$ and $T_A = 25^\circ C$.

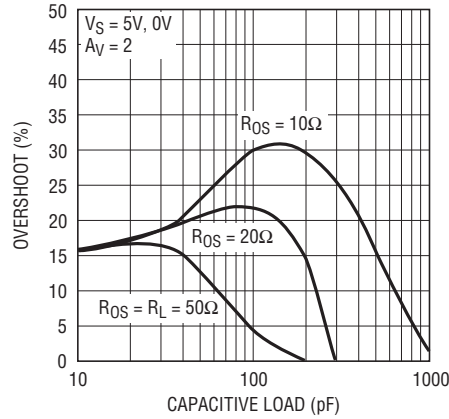
Frequency (MHz)	Positive Supply PSRR (dB)	Negative Supply PSRR (dB)
0.001	92	88
0.01	88	85
0.05	90	85
0.1	80	75
1	55	50
10	35	25
100	0	0

TYPICAL PERFORMANCE CHARACTERISTICS

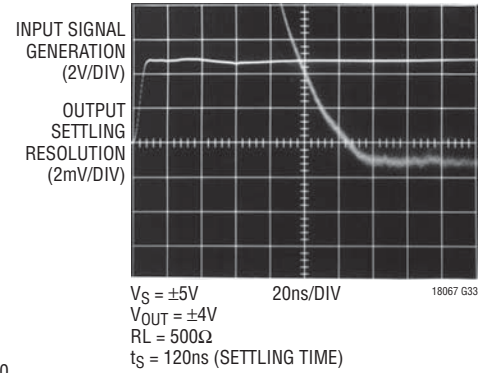
Series Output Resistor vs Capacitive Load



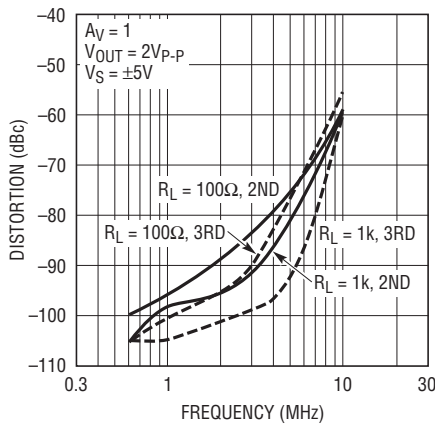
Series Output Resistor vs Capacitive Load



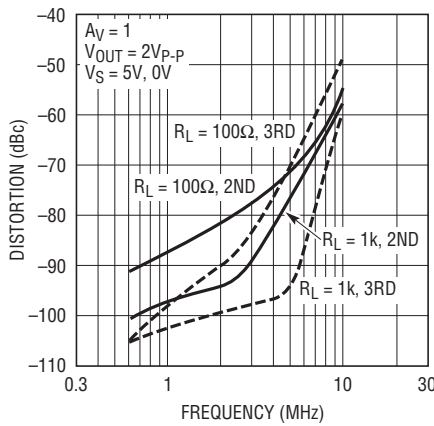
0.01% Settling Time



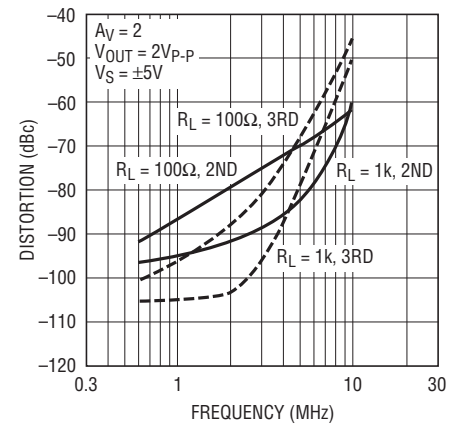
Distortion vs Frequency



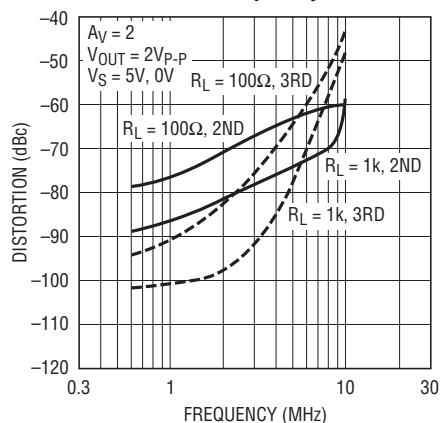
Distortion vs Frequency



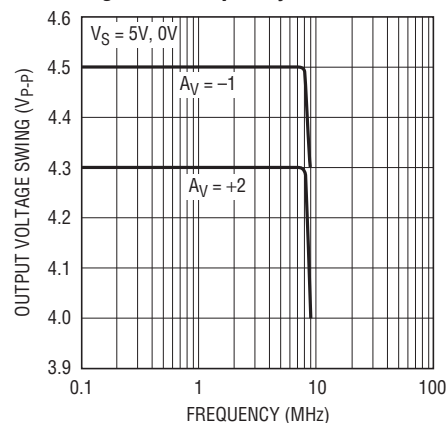
Distortion vs Frequency



Distortion vs Frequency

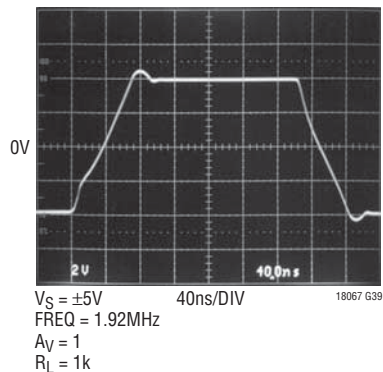


Maximum Undistorted Output Signal vs Frequency

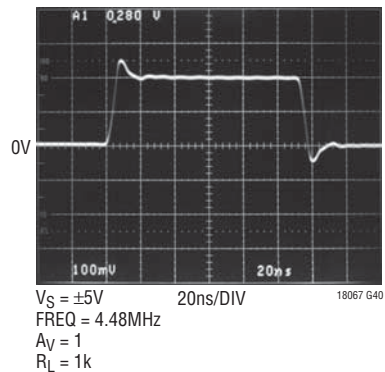


TYPICAL PERFORMANCE CHARACTERISTICS

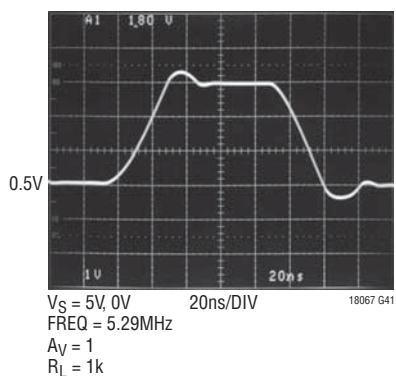
±5V Large-Signal Response



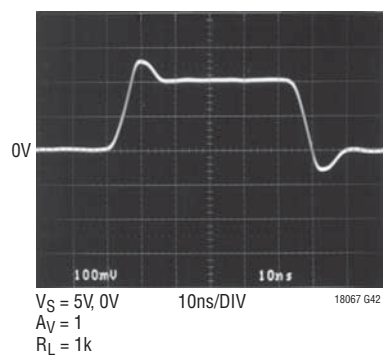
±5V Small-Signal Response



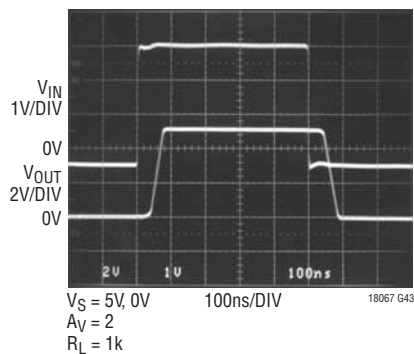
5V Large-Signal Response



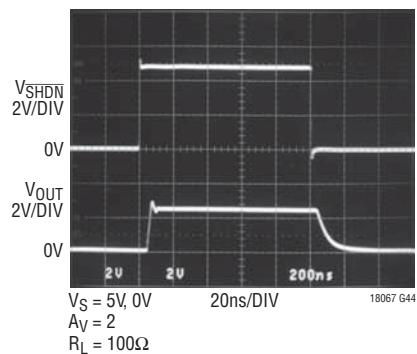
5V Small-Signal Response



Output Overdriven Recovery



Shutdown Response



APPLICATIONS INFORMATION

Rail-to-Rail Characteristics

The LT1806/LT1807 have input and output signal range that covers from negative power supply to positive power supply. Figure 1 depicts a simplified schematic of the amplifier. The input stage is comprised of two differential amplifiers, a PNP stage Q1/Q2 and a NPN stage Q3/Q4 that are active over different ranges of common mode input voltage. The PNP differential pair is active between the negative supply to approximately 1.5V below the positive supply. As the input voltage moves closer toward the positive supply, the transistor Q5 will steer the tail current I_1 to the current mirror Q6/Q7, activating the NPN differential pair. The PNP pair becomes inactive for the rest of the input common mode range up to the positive supply.

A pair of complementary common emitter stages Q14/Q15 that enable the output to swing from rail to rail constructs the output stage. The capacitors C1 and C2 form the local feedback loops that lower the output impedance at high frequency. These devices are fabricated on Linear Technology's proprietary high speed complementary bipolar process.

Power Dissipation

The LT1806/LT1807 amplifiers combine high speed with large output current in a small package, so there is a need to ensure that the die's junction temperature does not exceed 150°C. The LT1806 is housed in an SO-8 package or a 6-lead SOT-23 package and the LT1807 is in an SO-8

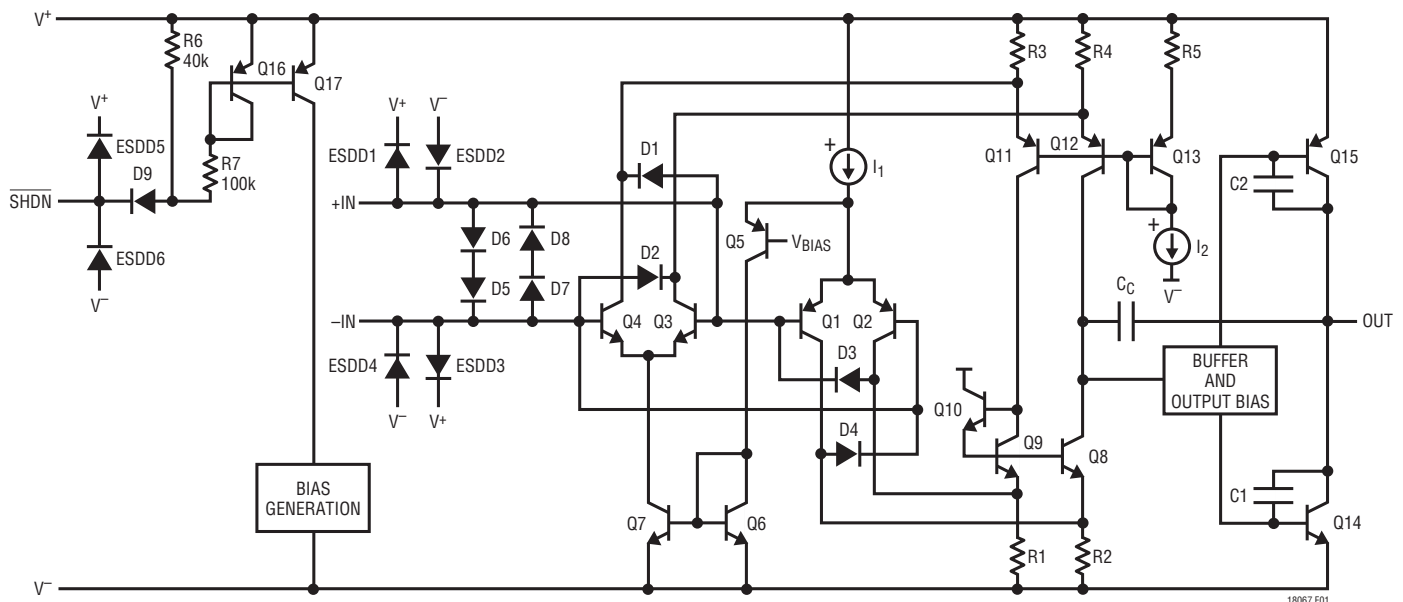


Figure 1. LT1806 Simplified Schematic Diagram

APPLICATIONS INFORMATION

or 8-lead MSOP package. All packages have the V^- supply pin fused to the lead frame to enhance the thermal conductance when connecting to a ground plane or a large metal trace. Metal trace and plated through-holes can be used to spread the heat generated by the device to the backside of the PC board. For example, on a 3/32" FR-4 board with 2oz copper, a total of 660 square millimeters connects to Pin 4 of LT1807 in an SO-8 package (330 square millimeters on each side of the PC board) will bring the thermal resistance, θ_{JA} , to about 85°C/W. Without extra metal trace beside the power line connecting to the V^- pin to provide a heat sink, the thermal resistance will be around 105°C/W. More information on thermal resistance for all packages with various metal areas connecting to the V^- pin is provided in Tables 1, 2 and 3.

Table 1. LT1806 6-Lead SOT-23 Package

COPPER AREA		BOARD AREA (mm ²)	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE (mm ²)	BACKSIDE (mm ²)		
270		2500	135°C/W
100		2500	145°C/W
20		2500	160°C/W
0		2500	200°C/W

Device is mounted on topside.

Table 2. LT1806/LT1807 SO-8 Package

COPPER AREA		BOARD AREA (mm ²)	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE (mm ²)	BACKSIDE (mm ²)		
1100	1100	2500	65°C/W
330	330	2500	85°C/W
35	35	2500	95°C/W
35	0	2500	100°C/W
0	0	2500	105°C/W

Device is mounted on topside.

Table 3. LT1807 8-Lead MSOP Package

COPPER AREA		BOARD AREA (mm ²)	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE (mm ²)	BACKSIDE (mm ²)		
540	540	2500	110°C/W
100	100	2500	120°C/W
100	0	2500	130°C/W
30	0	2500	135°C/W
0	0	2500	140°C/W

Device is mounted on topside.

Junction temperature T_J is calculated from the ambient temperature T_A and power dissipation P_D as follows:

$$T_J = T_A + (P_D \cdot \theta_{JA})$$

The power dissipation in the IC is the function of the supply voltage, output voltage and the load resistance. For a given supply voltage, the worst-case power dissipation $P_{D(MAX)}$ occurs at the maximum quiescent supply current and at the output voltage which is half of either supply voltage (or the maximum swing if it is less than 1/2 the supply voltage). $P_{D(MAX)}$ is given by:

$$P_{D(MAX)} = (V_S \cdot I_{S(MAX)}) + (V_S/2)^2/R_L$$

Example: An LT1807 in SO-8 mounted on a 2500mm² area of PC board without any extra heat spreading plane connected to its V^- pin has a thermal resistance of 105°C/W, θ_{JA} . Operating on $\pm 5V$ supplies with both amplifiers simultaneously driving 50Ω loads, the worst-case power dissipation is given by:

$$\begin{aligned} P_{D(MAX)} &= 2 \cdot (10 \cdot 14mA) + 2 \cdot (2.5)^2/50 \\ &= 0.28 + 0.25 = 0.53W \end{aligned}$$

APPLICATIONS INFORMATION

The maximum ambient temperature that the part is allowed to operate is:

$$\begin{aligned} T_A &= T_J - (P_{D(MAX)} \cdot 105^\circ\text{C/W}) \\ &= 150^\circ\text{C} - (0.53\text{W} \cdot 105^\circ\text{C/W}) = 94^\circ\text{C} \end{aligned}$$

To operate the device at higher ambient temperature, connect more metal area to the V^- pin to reduce the thermal resistance of the package as indicated in Table 2.

Input Offset Voltage

The offset voltage will change depending upon which input stage is active and the maximum offset voltage is guaranteed to less than $550\mu\text{V}$. To maintain the precision characteristics of the amplifier, the change of V_{OS} over the entire input common mode range (CMRR) is limited to be less than $550\mu\text{V}$ on a single 5V and 3V supply.

Input Bias Current

The input bias current polarity depends on a given input common voltage at which the input stage is operating. When the PNP input stage is active, the input bias currents flow out of the input pins. When the NPN input stage is activated, the input bias current flows into the input pins. Because the input offset current is less than the input bias current, matching the source resistances at the input pins will reduce total offset error.

Output

The LT1806/LT1807 can deliver a large output current, so the short-circuit current limit is set around 85mA to prevent damage to the device. Attention must be paid to keep the junction temperature of the IC below the absolute maximum rating of 150°C (refer to the Power Dissipation section) when the output is continuously short circuited. The output of the amplifier has reverse-biased diodes connected to each supply. If the output is forced beyond either supply, unlimited current will flow through these diodes. If the current is transient and limited to one hundred milliamps or less, no damage to the device will occur.

Overdrive Protection

When the input voltage exceeds the power supplies, two pairs of crossing diodes D1 to D4 will prevent the output from reversing polarity. If the input voltage exceeds either power supply by 700mV, diode D1/D2 or D3/D4 will turn on to keep the output at the proper polarity. For the phase reversal protection to perform properly, the input current must be limited to less than 5mA. If the amplifier is severely overdriven, an external resistor should be used to limit the overdrive current.

APPLICATIONS INFORMATION

The LT1806/LT1807's input stages are also protected against large differential input voltages of 1.4V or higher by a pair of back-to-back diodes, D5/D8, that prevent the emitter-base breakdown of the input transistors. The current in these diodes should be limited to less than 10mA when they are active. The worst-case differential input voltage usually occurs when the input is driven while the output is shorted to ground in a unity gain configuration. In addition, the amplifier is protected against ESD strikes up to 3kV on all pins by a pair of protection diodes, ESDD1 to ESDD6, on each pin that are connected to the power supplies as shown in Figure 1.

Capacitive Load

The LT1806/LT1807 are optimized for high bandwidth and low distortion applications. They can drive a capacitive load of about 20pF in a unity-gain configuration, and more for higher gain. When driving a larger capacitive load, a resistor of 10 Ω to 50 Ω should be connected between the output and the capacitive load to avoid ringing or oscillation. The feedback should still be taken from the output so that the resistor will isolate the capacitive load to ensure stability. Graphs on capacitive loads indicate the transient response of the amplifier when driving the capacitive load with a specified series resistor.

Feedback Components

When feedback resistors are used to set up gain, care must be taken to ensure that the pole formed by the feedback resistors and the total capacitance at the inverting input does not degrade stability. For instance, the LT1806/LT1807 in a noninverting gain of 2, set up with two 1k resistors and a capacitance of 3pF (part plus PC board) will probably ring in transient response. The pole is formed at 106MHz that will reduce phase margin by 34 degrees when the crossover frequency of the amplifier is around 70MHz. A capacitor of 3pF or higher connected across the feedback resistor will eliminate any ringing or oscillation.

$\overline{\text{SHDN}}$ Pin

The LT1806 has a $\overline{\text{SHDN}}$ pin to reduce the supply current to less than 0.9mA. When the $\overline{\text{SHDN}}$ pin is pulled low, it will generate a signal to power down the device. If the pin is left unconnected, an internal pull-up resistor of 40k will keep the part fully operating as shown in Figure 1. The output will be high impedance during shutdown, and the turn-on and turn-off time is less than 100ns. Because the input is protected by a pair of back-to-back diodes, the input signal will feed through to the output during shutdown mode if the amplitude of signal between the inputs is larger than 1.4V.

TYPICAL APPLICATIONS

Driving A/D Converter

The LT1806/LT1807 have 60ns settling time to 0.01% on a 2V step signal, and 20Ω output impedance at 100MHz, that makes them ideal for driving high speed A/D converters. With the rail-to-rail input and output, and low supply voltage operation, the LT1806/LT1807 are also desirable for single supply applications. As shown in the application on the front page of this data sheet, the LT1807 drives a 10MSPS, 12-bit, LTC1420 ADC in a gain of 20. Driving the LTC1420 differentially will optimize the signal-to-noise ratio, SNR, and the total harmonic distortion, THD, of the A/D converter. The lowpass filter, R5, R6 and C3 reduce

noise or distortion products that might come from the input signal. High quality capacitors and resistors, NPO chip capacitor and metal film surface mount resistors, should be used since these components can add to distortion. The voltage glitch of the converter, due to its sampling nature is buffered by the LT1807, and the ability of the amplifier to settle it quickly will affect the spurious free dynamic range of the system. Figure 2 depicts the LT1806 driving LTC1420 at noninverting gain of 2 configuration. The FFT responses show a better than 92dB of spurious free dynamic range, SFDR.

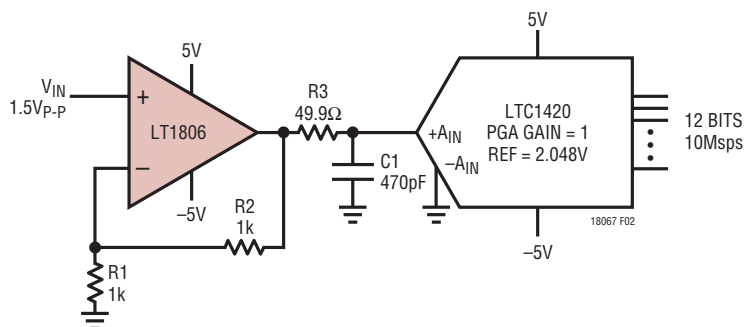


Figure 2. Noninverting A/D Driver

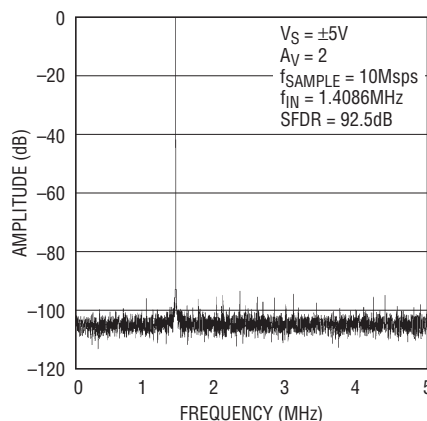


Figure 3. 4096 Point FFT Response

TYPICAL APPLICATIONS

Single Supply Video Line Driver

The LT1806/LT1807 are wideband rail-to-rail op amps with large output current that allows them to drive video signals in low supply applications. Figure 4 depicts a single supply video line driver with AC coupling to minimize the quiescent power dissipation. Resistors R1 and R2 are used to level-shift the input and output to provide the largest signal swing. The gain of 2 is set up with R3 and R4 to restore the signal at V_{OUT} , which is attenuated by 6dB due to the matching of the 75Ω line with the back-terminated resistor,

R5. The back termination will eliminate any reflection of the signal that comes from the load. The input termination resistor, R_T , is optional—it is used only if matching of the incoming line is necessary. The values of C1, C2 and C3 are selected to minimize the droop of the luminance signal. In some less stringent requirements, the value of capacitors could be reduced. The –3dB bandwidth of the driver is about 90MHz on 5V supply, and the amount of peaking will vary upon the value of capacitor C4.

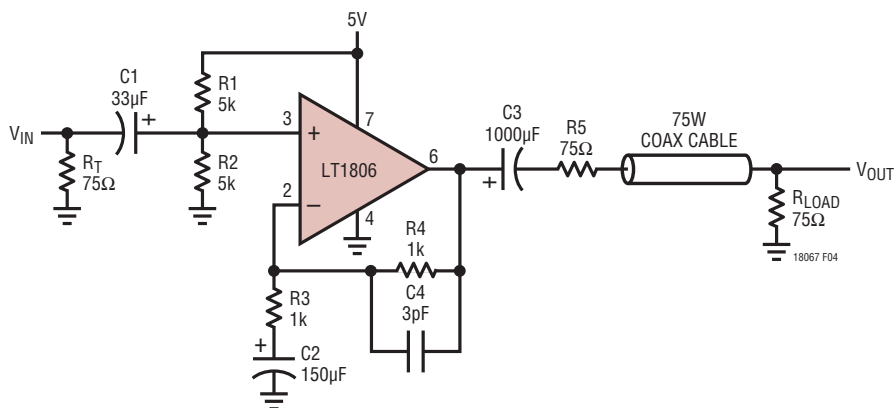


Figure 4. 5V Single Supply Video Line Driver

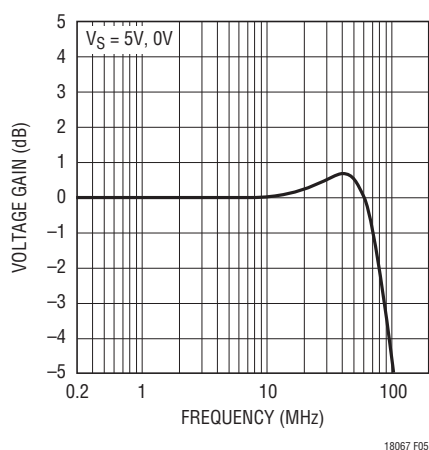


Figure 5. Video Line Driver Frequency Response

TYPICAL APPLICATIONS

Single 3V Supply, 4MHz, 4th Order Butterworth Filter

Benefiting from a low voltage supply operation, low distortion and rail-to-rail output of LT1806/LT1807, a low distortion filter that is suitable for antialiasing can be built as shown in Figure 6.

On a 3V supply, the filter built with LT1807 has a passband of 4MHz with 2.5V_{P-P} signal and stopband that is greater than 70dB to frequency of 100MHz. As an option to minimize the DC offset voltage at the output, connect a series resistor of 365Ω and a bypass capacitor at the noninverting inputs of the amplifiers as shown in Figure 6.

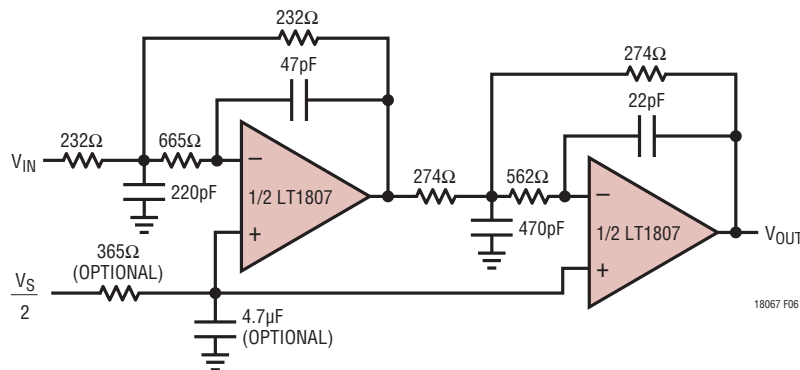


Figure 6. Single 3V Supply, 4MHz, 4th Order Butterworth Filter

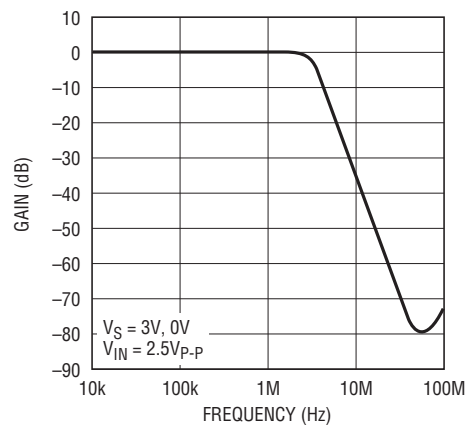


Figure 7. Filter Frequency Response

TYPICAL APPLICATIONS

1MHz Series Resonant Crystal Oscillator with Square and Sinusoid Outputs

Figure 8 shows a classic 1MHz series resonant crystal oscillator. At series resonance, the crystal is a low impedance and the positive feedback connection is what brings about oscillation at the series resonance frequency. The RC feedback around the other path ensures that the circuit does not find a stable DC operating point and refuse to oscillate. The comparator output is a 1MHz square wave with a measured jitter of 28ps_{RMS} with a 5V supply and 40ps_{RMS} with a 3V supply. On the other side of the crystal, however, is an excellent looking sine wave except for the fact of the small high frequency glitch caused by the fast

edge and the crystal capacitance (middle trace of Figure 9). Sinusoid amplitude stability is maintained by the fact that the sine wave is basically a filtered version of the square wave; the usual amplitude control loops associated with sinusoidal oscillators are not immediately necessary.¹ One can make use of this sine wave by buffering and filtering it, and this is the combined task of the LT1806. It is configured as a bandpass filter with a Q of 5 and does a good job of cleaning up and buffering the sine wave. Distortion was measured at -70dBc and -60dBc on the second and third harmonics.

¹Amplitude will be a linear function of comparator output swing, which is supply dependent and therefore controllable. The important difference here is that any added amplitude stabilization loop will not be faced with the classical task of avoiding regions of nonoscillation versus clipping.

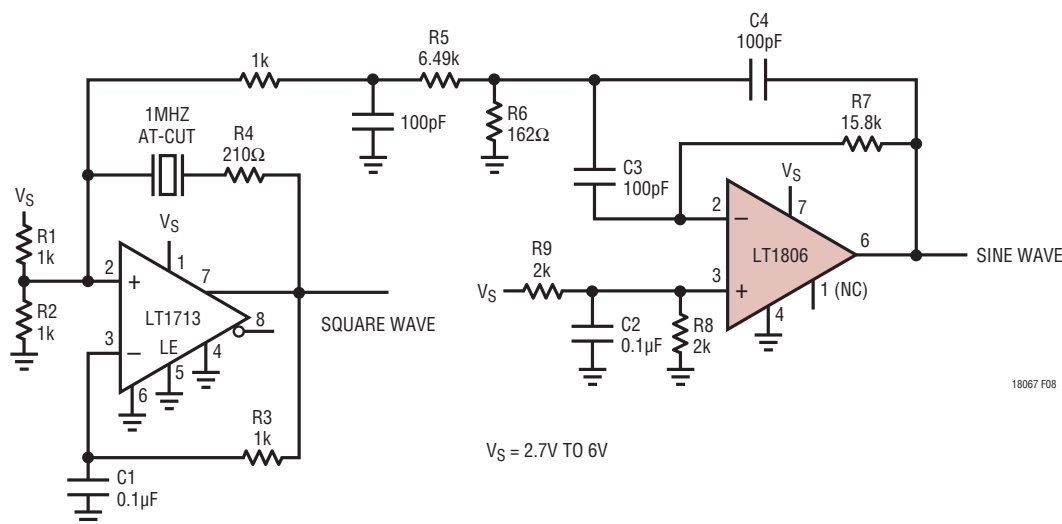


Figure 8. LT1713 Comparator is Configured as a Series Resonant Crystal Oscillator. The LT1806 Op Amp is Configured in a Q = 5 Bandpass Filter with $f_c = 1\text{MHz}$

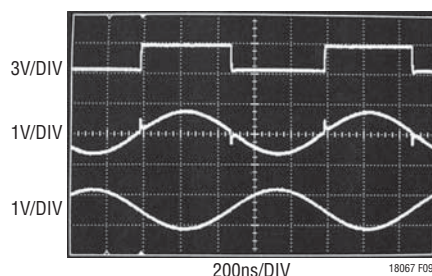
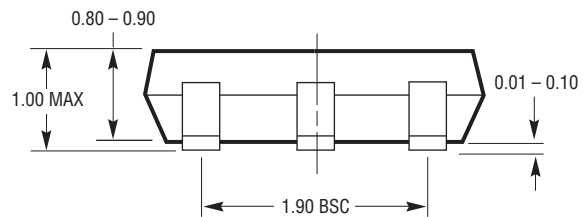
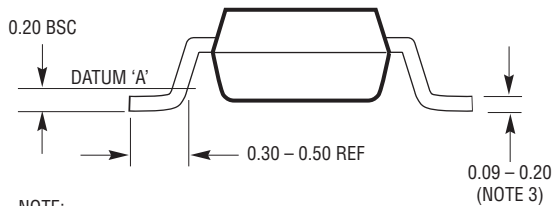
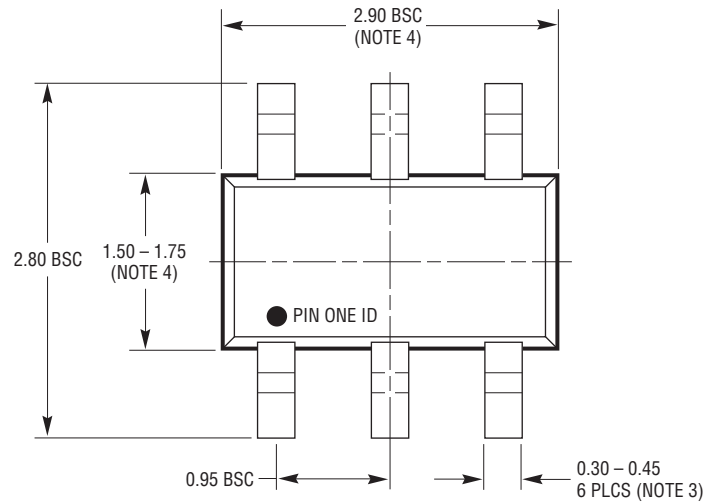
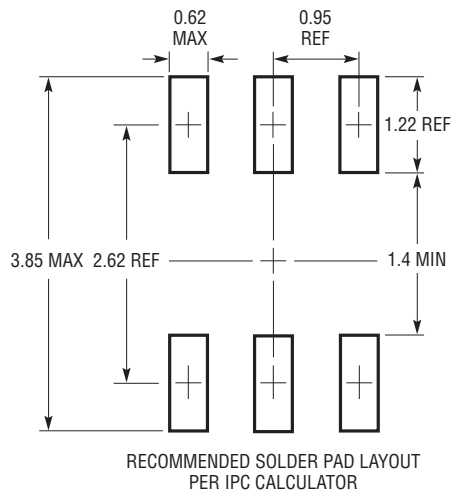


Figure 9. Oscillator Waveforms with $V_S = 3\text{V}$. Top Trace is Comparator Output. Middle Trace is Crystal Feedback to Pin 2 at LT1713. Bottom Trace is Buffered, Inverted and Bandpass Filtered with a Q of 5 by the LT1806

PACKAGE DESCRIPTION

S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)



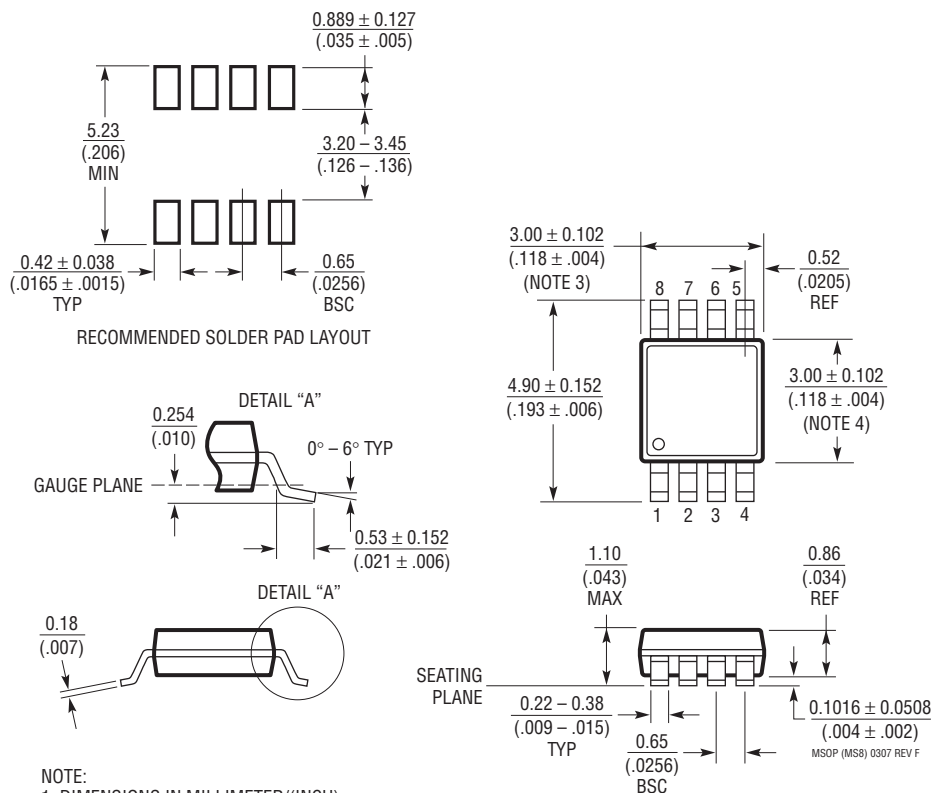
- NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
 2. DRAWING NOT TO SCALE
 3. DIMENSIONS ARE INCLUSIVE OF PLATING
 4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
 5. MOLD FLASH SHALL NOT EXCEED 0.254mm
 6. JEDEC PACKAGE REFERENCE IS MO-193

S6 TSOT-23 0302 REV B

PACKAGE DESCRIPTION

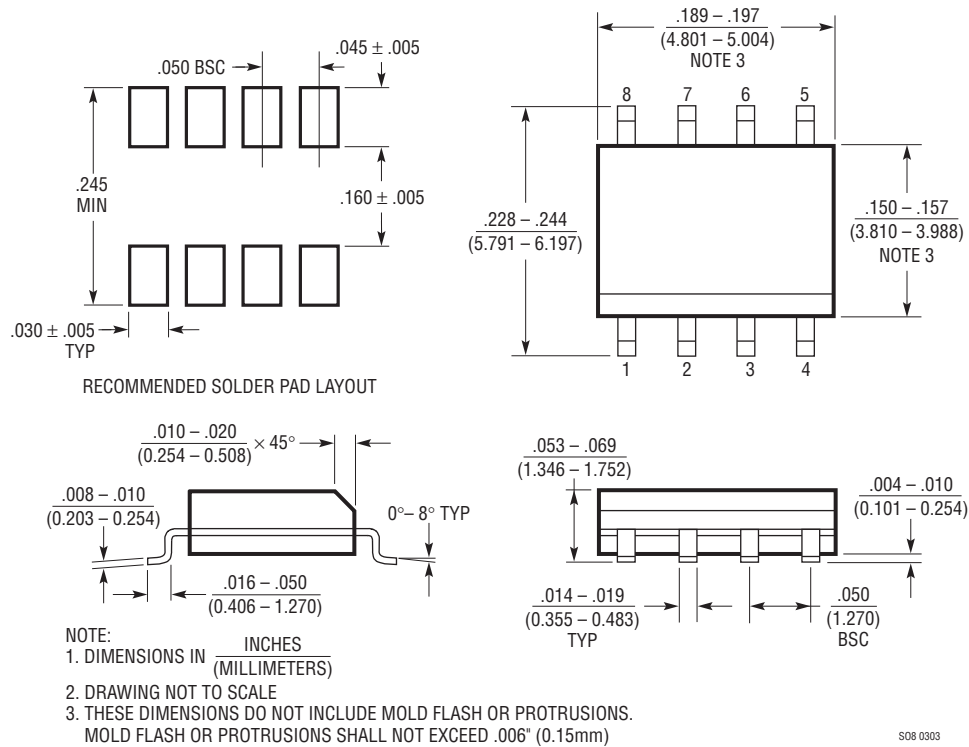
MS8 Package 8-Lead Plastic MSOP

(Reference LTC DWG # 05-08-1660 Rev F)



PACKAGE DESCRIPTION

S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)



S08 0303

TYPICAL APPLICATION

FET Input, Fast, High Gain Photodiode Amplifier

Figure 10 shows a fast, high gain transimpedance amplifier applied to a photodiode. A JFET buffer is used for its extremely low input bias current and high speed. The LT1097 and 2N3904 keep the JFET biased at I_{DSS} for zero offset and lowest voltage noise. The JFET then drives the LT1806, with R_F closing the high speed loop back to the JFET input and setting the transimpedance gain. C4 helps improve the phase margin of the fast loop. Output voltage noise density was measured as $9nV/\sqrt{Hz}$ with R_F short circuited. With R_F varied from 100k to 1M,

total output noise was below $1mV_{RMS}$ measured over a 10MHz bandwidth. Table 4 shows results achieved with various values of R_F and Figure 11 shows the time domain response with $R_F = 499k$.

Table 4. Results Achieved for Various R_F , 1.2V Output Step

R_F	10% to 90% RISE TIME	-3dB BANDWIDTH
100k	64ns	6.8MHz
200k	94ns	4.6MHz
499k	154ns	3MHz
1M	263ns	1.8MHz

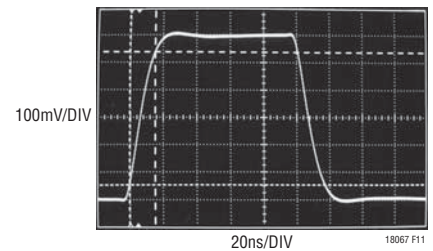
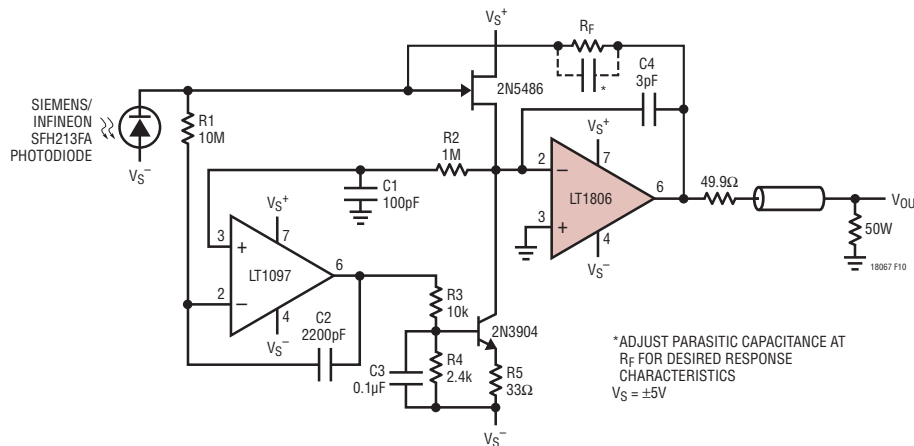


Figure 11. Step Response with $R_F = 499k$

Figure 10. Fast, High Gain Photodiode Amplifier

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1395	400MHz Current Feedback Amplifier	800V/ μs Slew Rate, Shutdown
LT1399	Triple 300MHz Current Feedback Amplifier	0.1dB Gain Flatness to 150MHz, Shutdown
LT1632/LT1633	Dual/Quad 45MHz, 45V/ μs Rail-to-Rail Input and Output Amplifiers	High DC Accuracy 1.35mV $V_{OS(MAX)}$, 70mA Output Current, Max Supply Current 5.2mA/Amp
LT1809/LT1810	Single/Dual 180MHz Input and Output Rail-to-Rail Amplifiers	350V/ μs Slew Rate, Shutdown, Low Distortion -90dBc at 5MHz
LT1812/LT1813	3mA, 100MHz, 750V/ μs Op Amp	High Slew Rate
LT1818/LT1819	9mA, 400MHz, 2500V/ μs Op Amp	Ultrahigh Slew Rate
LT6200/LT6201	165MHz Rail-to-Rail Input and Output, 0.95nV/ $\sqrt{Hz}$ Low Noise Op Amp	Lowest Noise
LT6202/LT6203	100MHz Rail-to-Rail Input and Output, 1.9nV/ $\sqrt{Hz}$ Op Amp	$I_{CC} = 2.5mA$