



CYPRESS

CY7C64601/603/613

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EZ-USB *FX* USB Microcontroller

Data Sheet

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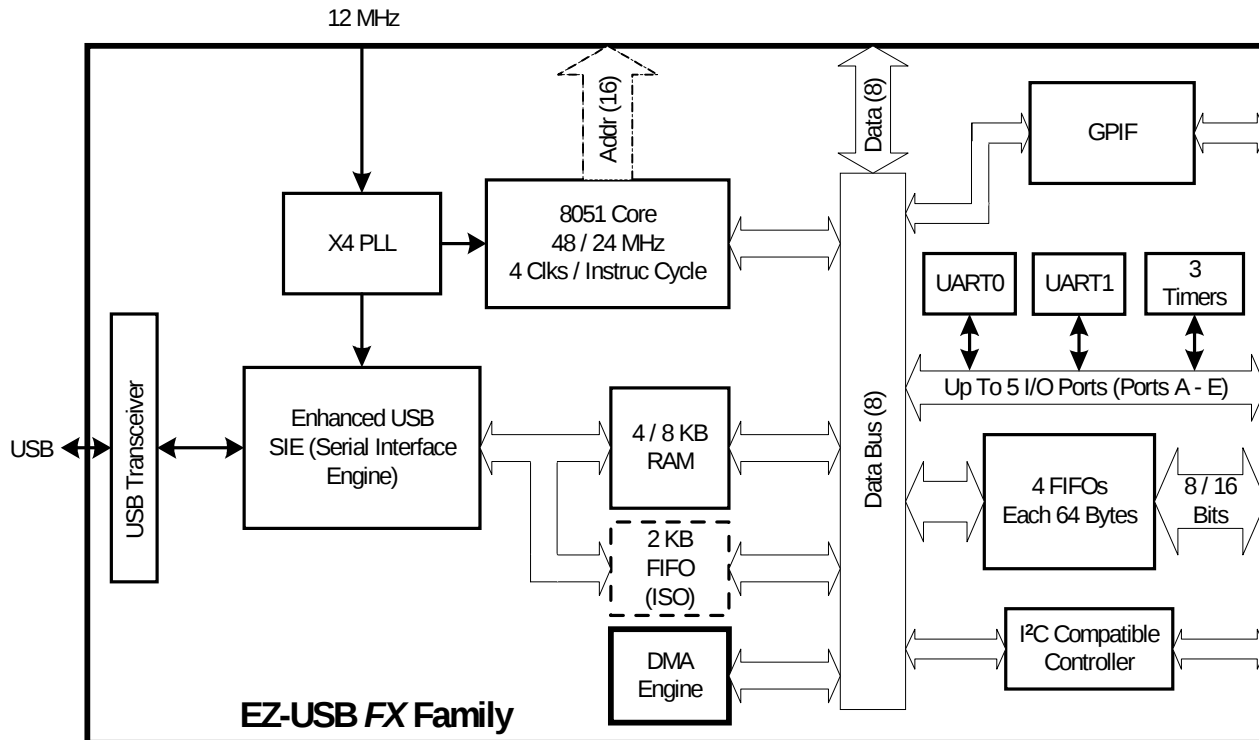
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1.0 Introduction

The EZ-USB FX (CY7C646xx) is Cypress Semiconductor's second-generation Full-speed USB family. EZ-USB FX products offer higher performance and a higher level of integration than first-generation EZ-USB products. The FX builds on the EZ-USB feature set, including an intelligent USB core, enhanced 8051, 8-Kbyte RAM, and high-performance I/O while maintaining upward code compatibility. The EZ-USB FX enhances the EZ-USB family by providing faster operation and more ways to transfer data into and out of the chip at very high speed.



Dotted line means optional feature.

1.1 EZ-USB FX Features

- Single-chip integrated USB Transceiver, SIE (Serial Interface Engine), and Enhanced 8051 Microprocessor
- Compliant with USB Specifications 1.1 and 2.0 (Full-speed device)
- Soft: 8051 runs code from internal or external RAM. Code can be:
 - Downloaded via USB
 - Loaded from EEPROM
 - Executed in-place from external memory (for example, Flash)
- Abundant endpoints and buffers
 - 14 Bulk/Interrupt endpoints, each with a maximum packet size of 64 bytes (per the USB Specification)
 - 16 Isochronous endpoints, with 2 KB of buffer space (1 KB, double buffered) which may be divided among the sixteen isochronous endpoints
 - 1 Control endpoint (bidirectional)
- Integrated, industry standard 8051 with enhanced features:
 - Four clocks per instruction cycle
 - 48-MHz or 24-MHz 8051, selectable by EEPROM configuration bit
 - Two UARTS
 - Three counter/timers

- Expanded interrupt system
- Two data pointers
- 3.3-volt operation
- Smart Serial Interface Engine (SIE)
 - Handles much of the low-level USB protocol in logic, simplifying 8051 code
- General Programmable InterFace (GPIF)
 - Allows direct connection to most parallel interfaces: 8- and 16-bit wide
 - *Eliminates* external glue logic in most applications
 - Programmable Waveform Instructions and Configuration Registers to define waveforms
 - Six Ready (RDY) inputs and six Control (CTL) outputs
- Expanded Vectored interrupt system expanded for USB, FIFO flags and DMA interrupts
- Separate buffers for SETUP and DATA portions of a CONTROL transfer
- Integrated I²C compatible controller
 - 400-kHz or 100-kHz operation
- Enhanced I/O
 - I/O port registers mapped to 8051 SFRs (Special Function Registers) for high speed bit operations
 - Port bits can be controlled using 8051 bit addressing instructions
 - Up to five 8-bit I/O ports
- Four integrated 8-bit-wide FIFOs
 - Each 64 bytes deep
 - Automatic conversion to and from 16-bit buses
 - Easy, glueless interface to ASIC, DSP ICs and external logic
 - Brings glue FIFOs inside for lower system cost
 - Internal or external clock
 - Synchronous (using strobes and a clock) or asynchronous (using strobes only)
- DMA Controller
 - Moves data between slave FIFOs, memory, and ports
 - Very fast transfers—one clock (20.8 ns = 48 MHz) per byte for internal transfers
 - Can use external RAM as additional FIFO (accessed via Address and Data buses)
- Special Autovectors for DMA and FIFO interrupts
- Glueless external memory expansion
 - Up to 16-bit address bus and 8-bit data bus (see *Table 1-1*)
 - Strokes RD#, WR#, OE#, CS# and PSEN#
 - Buses not multiplexed (as in standard 8051), saving one clock per external memory cycle
- Three package options—128-pin PQFP, 80-pin PQFP, and 52-pin PQFP

Table 1-1. EZ-USB FX Family / Ordering Information

Part Number	Package	Ram Size	ISO Support	# Prog I/Os	Max FIFO Width		Addr/Data Bus	Burst I/O Rate	Hardwired PID
					Slave Mode	GPIF (Bus Master) Mode			
CY7C64601-52NC	52-pin PQFP	4 KB	No	16	8 Bits	8 Bits	8-bit Data	48 MB/s	2226h
CY7C64603-52NC	52-pin PQFP	8 KB	No	18	8 Bits	8 Bits	8-bit Data	48 MB/s	2236h
CY7C64613-52NC	52-pin PQFP	8 KB	Yes	18	8 Bits	8 Bits	8-bit Data	48 MB/s	2235h
CY7C64603-80NC	80-pin PQFP	8 KB	No	32	16 Bits	16 Bits	8-bit Data	96 MB/s	2235h
CY7C64613-80NC	80-pin PQFP	8 KB	Yes	32	16 Bits	16 Bits	8-bit Data	96 MB/s	2235h
CY7C64603-128NC	128-pin PQFP	8 KB	No	40	16 Bits	16 Bits	8-bit Data + 16-bit Addr	96 MB/s	2235h
CY7C64613-128NC	128-pin PQFP	8 KB	Yes	40	16 Bits	16 Bits	8-bit Data + 16-bit Addr	96 MB/s	2235h
CY3671	EZ-USB FX Development Kit								

1.2 Example Applications

- DSL modems
- ATAPI interface
- Memory card readers
- Legacy conversion devices
- Cameras
- Scanners
- Home PNA
- Wireless LAN
- MP3 players
- Networking

1.3 Other Resources

Other sources of EZ-USB FX information include:

- EZ-USB FX Technical Reference Manual (TRM), Version 1.1 (March 2000) or later
- CY3671 EZ-USB FX Development Kit
- the site www.cypress.com/usb, which includes information about many Reference Designs, such as USB Mass Storage Device, etc.

2.0 Functional Overview

2.1 Microprocessor

The EZ-USB FX uses a 12-MHz crystal for low EMI. An internal oscillator and PLL develops an internal 48-MHz clock for use by the USB Serial Interface Engine and the 8051 microprocessor. The 8051 can run at either 24 MHz or 48 MHz, controlled by a bit in the EEPROM attached to the I²C compatible bus. The default rate (with no EEPROM connected) is 24 MHz.

The internal microprocessor is an enhanced version of the industry-standard 8051. Enhancements include 4 clock per instruction cycle operation, a second data pointer, and an enhanced interrupt system. The 8051 includes two UARTS, three counter-timers, and 256 bytes of register RAM.

The EZ-USB family implements I/O differently than the standard 8051, by having its I/O control registers in external memory space. The EZ-USB FX preserves this addressing for backward EZ-USB compatibility, and adds the ability to control I/O registers using 8051 SFRs (Special Function Registers). This improves I/O access time. For example, an I/O pin may be toggled using one 8051 instruction, e.g., CPL (bit).

The 8051 CODE and XDATA memory consists of an internal 4 or 8 KB RAM. This RAM is normally downloaded via the USB cable at plug-in, followed by the 8051 starting up and executing the downloaded code. This gives the EZ-USB FX family its 'soft' operation feature, whereby permanent memory such as ROM or Flash memory is not required. Program code updates can easily

be done in the field since the code is loaded from the PC, not by physically changing or reprogramming a memory device. The 8051 program memory can also be loaded from the EEPROM connected to the I²C compatible bus on reset for stand-alone use without the USB connected.

The 128-pin version of the EZ-USB *FX* brings out the full 8051 address and data buses, plus decoded control signals OE#, CS#, RD#, PSEN#, and WR# to allow glueless connection to external memory devices. The 80- and 52-pin packages allow smaller footprints and more cost effective solutions for certain designs, but do not have external access to the 8051 buses.

2.2 USB SIE

The EZ-USB *FX* uses the EZ-USB family enhanced SIE (Serial Interface Engine). This SIE has the intelligence to perform full USB enumeration, creating a default USB device with predefined endpoints and alternate settings. This enhanced SIE is essential in achieving the family's soft operation, since it provides the mechanism to download firmware prior to the 8051 running.

Once the 8051 is in control, it can use advanced features of the SIE to simplify its USB firmware. Endpoint zero SETUP data is placed in a separate 8-byte RAM space for easy access. GET_Descriptor requests are simplified by using a special Setup Data Pointer. The 8051 simply loads a descriptor address into this 16-bit register, and the SIE takes care of the remaining overhead, i.e., dividing the descriptor into packets, sending them via endpoint 0 in response to IN tokens, and providing the necessary handshakes. The 8051 can do other chores while the SIE completes this USB transfer.

2.3 GPIF (General Programmable InterFace)

The GPIF is a flexible 8 or 16-bit parallel interface driven by a user-programmable set of vectors that operate similarly to a finite state machine. It allows the EZ-USB *FX* to perform local bus mastering, and can implement a wide variety of protocols such as ATAPI, printer parallel port, and Utopia.

The GPIF has six programmable Control Outputs (CTL), six Address Outputs (ADR), and six general purpose Ready Inputs (RDY). The data bus width can be 8 or 16 bits. Each GPIF instruction defines the state of the control outputs, or determines what state a ready input (or multiple inputs) must be before proceeding. A sequence of the GPIF instructions make up a single *waveform* that will be executed to perform the desired data move between the EZ-USB *FX* and the external circuit.

2.4 Slave FIFOs

Many high-bandwidth USB designs use a FIFO between the USB interface chip and external logic to match data rates, or to smooth the USB data delivery (which, being packet oriented, occurs in bursts). The EZ-USB *FX* moves this glue logic into the part by providing four 64-byte internal slave FIFOs. The FIFOs also provide two important interface functions, external clocking and bus width conversion.

Using external clocking, external logic (such as a DSP or ASIC) can clock data into or out of the slave FIFOs under control of its own clock, rather than synchronizing with the clock supplied by the EZ-USB *FX* (24 or 48 MHz). The FIFOs can be controlled either synchronously (using strobe signals and a clock) or asynchronously (using strobe signals only). The slave FIFO data is available as two 8-bit buses, which may be used simultaneously to operate as a single 16-bit data bus. The 16-bit connection, along with fast double-byte mode, combine to give fast conversion between 8 and 16 bit buses. A flexible set of FIFO flags (full, empty, and programmable) provide FIFO flow control.

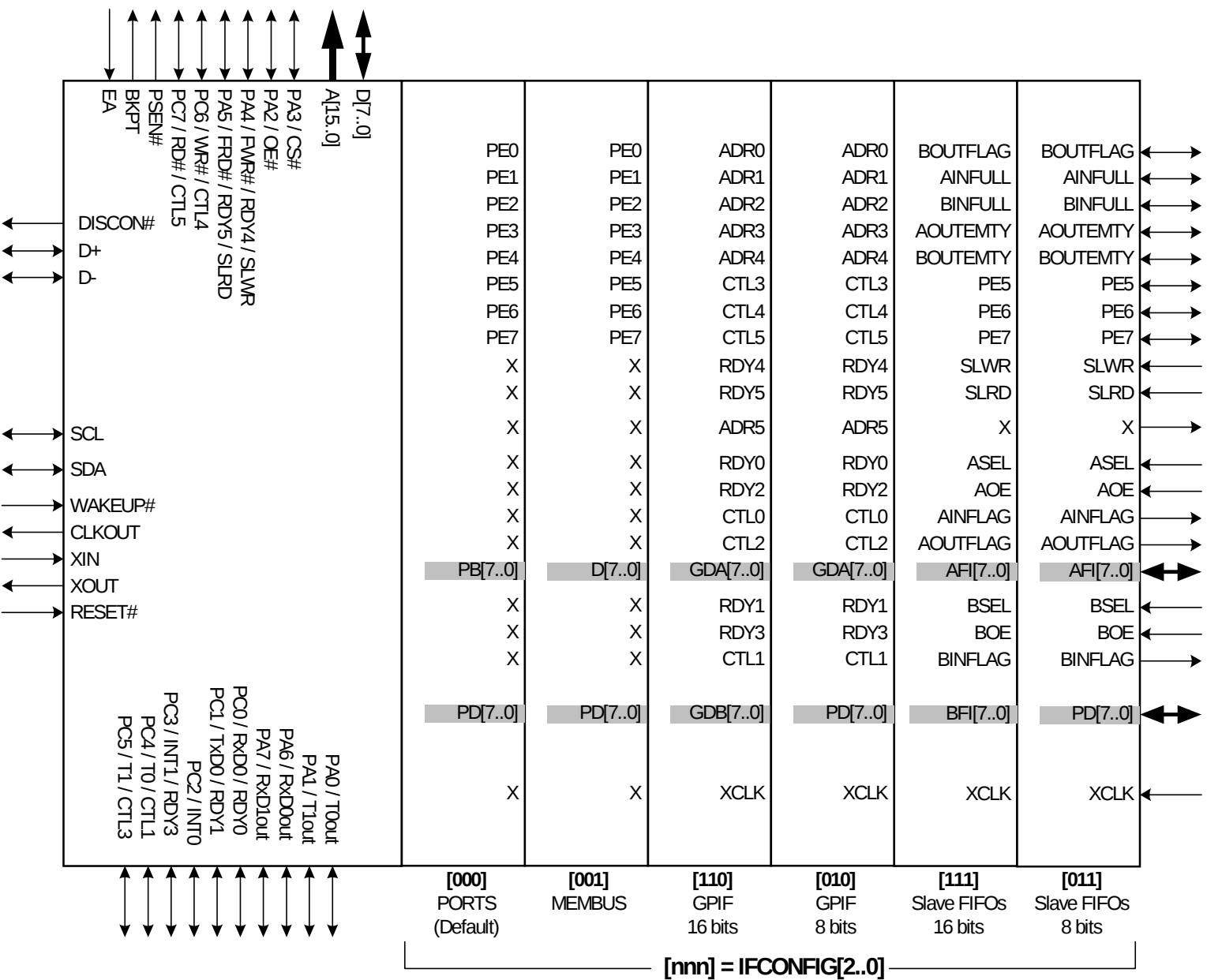
2.5 DMA

With many sources and destinations for USB data, such as endpoint buffers, slave FIFOs, and internal/external RAM buffers, it is important to move blocks of data between them quickly. Using internal DMA, the 8051 sets up source, destination, and transfer length registers, and then initiates a DMA transfer. The maximum DMA transfer rate occurs between internal resources, such as endpoint buffers and slave FIFOs. This maximum rate is one byte per 48-MHz clock, or 48 Mbytes per second.

2.6 Flexible Configuration

The EZ-USB *FX* supports a highly configurable I/O structure. *Figure 2-1* on page 7 shows the *general* scheme of the assignment of pins to I/O Ports. The 80- and 56-pin products are subsets of the 128-pin products, hence they follow a similar scheme.

For details of how to set the configuration registers to configure the I/O Ports, consult Section 3.3 "Pin Description Table" on page 13 of this data sheet *and* the EZ-USB *FX* TRM (primarily Chapter 4).



2.7 Endpoints

Endpoint	Type	Buffer Size (Bytes)
EP0-IN EP0-OUT	Control	64 64
EP1-IN	Bulk/Interrupt	64
EP1-OUT	Bulk/Interrupt	64
EP2-IN	Bulk/Interrupt	64
EP2-OUT	Bulk/Interrupt	64
EP3-IN	Bulk/Interrupt	64
EP3-OUT	Bulk/Interrupt	64
EP4-IN	Bulk/Interrupt	64
EP4-OUT	Bulk/Interrupt	64
EP5-IN	Bulk/Interrupt	64
EP5-OUT	Bulk/Interrupt	64
EP6-IN	Bulk/Interrupt	64
EP6-OUT	Bulk/Interrupt	64
EP7-IN	Bulk/Interrupt	64
EP7-OUT	Bulk/Interrupt	64
EP8-IN	Isochronous	0–1023 ^[1]
EP8-OUT	Isochronous	0–1023 ^[1]
EP9-IN	Isochronous	0–1023 ^[1]
EP9-OUT	Isochronous	0–1023 ^[1]
EP10-IN	Isochronous	0–1023 ^[1]
EP10-OUT	Isochronous	0–1023 ^[1]
EP11-IN	Isochronous	0–1023 ^[1]
EP11-OUT	Isochronous	0–1023 ^[1]
EP12-IN	Isochronous	0–1023 ^[1]
EP12-OUT	Isochronous	0–1023 ^[1]
EP13-IN	Isochronous	0–1023 ^[1]
EP13-OUT	Isochronous	0–1023 ^[1]
EP14-IN	Isochronous	0–1023 ^[1]
EP14-OUT	Isochronous	0–1023 ^[1]
EP15-IN	Isochronous	0–1023 ^[1]
EP15-OUT	Isochronous	0–1023 ^[1]

Note:

1. A total of 1024 FIFO bytes can be divided among all Isochronous endpoints. (1023 is the maximum USB-specified Isochronous packet size.)

The EZ-USB *FX* has 16 Control, Bulk, and Interrupt endpoints. One endpoint pair is dedicated to endpoint zero, with separate EP0-IN and EP0-OUT buffers. Fourteen additional 64-byte buffers may be used as Bulk or Interrupt endpoints. These endpoints may be double-buffered by using an endpoint pairing mechanism. Double buffering allows the 8051 to access a packet as another packet is being transmitted or received over USB. This technique is essential in high-bandwidth applications where NAKs by the USB device would reduce performance.

The EZ-USB *FX* also has sixteen Isochronous (ISO) endpoints which share 1024 bytes of double-buffered endpoint memory (2 KB total). The ISO buffer sizes are programmable in 16-byte increments. The Isochronous endpoint buffers are accessed as FIFOs.

Endpoint data is serviced either directly by the 8051, or moved on- or off-chip using the built in DMA controller. Bulk data is visible either in 64-byte random-access buffers, or as FIFOs (using the AutoPointer feature).

Each endpoint has a its own interrupt vector, allowing ISRs (Interrupt Service Routines) to be called automatically, with minimum overhead and latency.

2.8 Default USB Machine

When the EZ-USB FX is plugged into USB with no EEPROM attached to its I²C compatible port (but **with** the SCL and SDA pull-ups installed), the intelligent SIE enumerates as a generic USB device with the following characteristics:

ID bytes

VID (Vendor ID)	0547h
PID (Product ID)	Varies. See Table 1-1.
DID (Device ID)	0000h

Default Endpoints

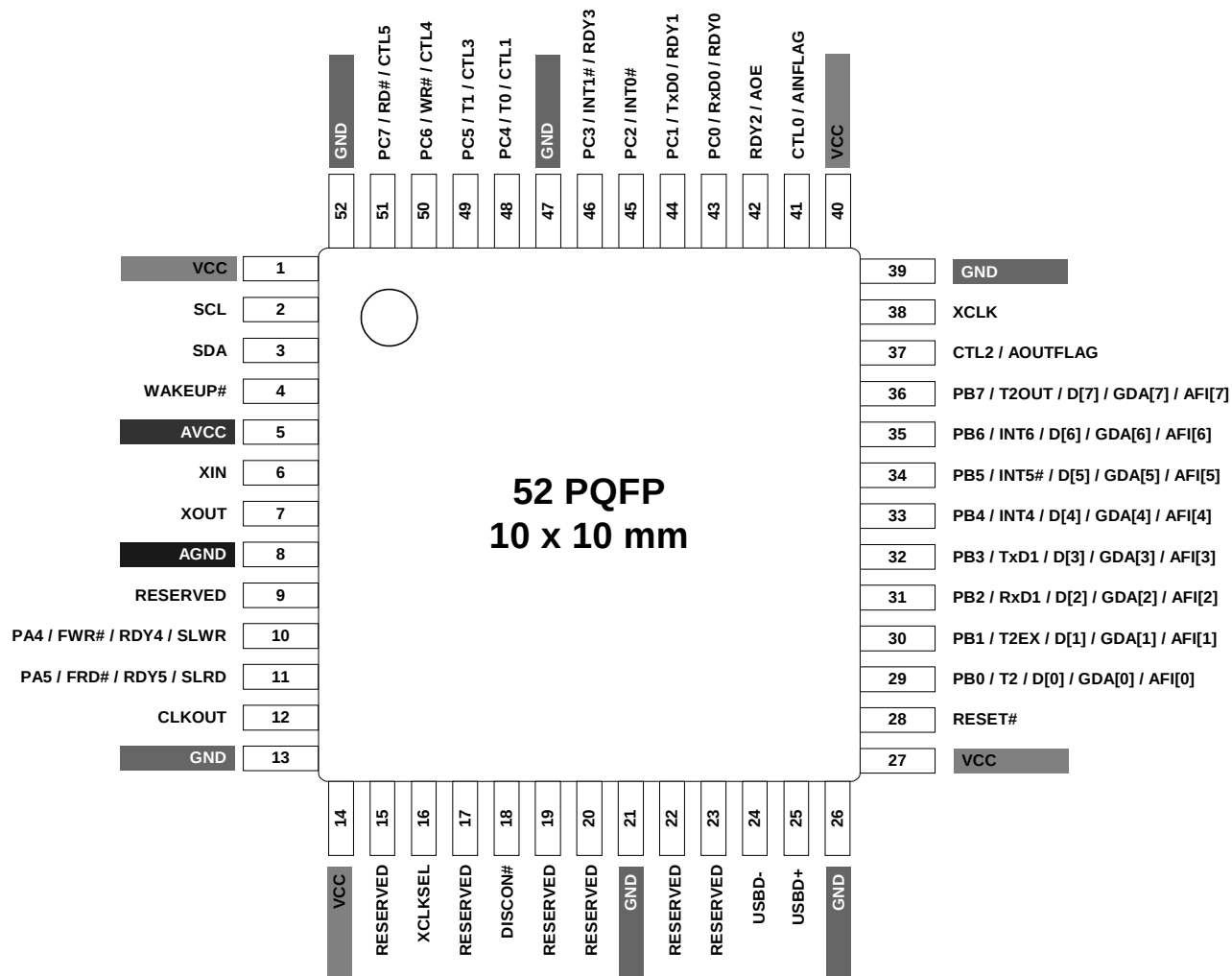
Endpoint	Type	Alternate Setting		
		0	1	2
		Max Packet Size (bytes)		
0	CTL	64	64	64
1 IN	INT	0	16	64
2 IN	BULK	0	64	64
2 OUT	BULK	0	64	64
4 IN	BULK	0	64	64
4 OUT	BULK	0	64	64
6 IN	BULK	0	64	64
6 OUT	BULK	0	64	64
8 IN	ISO	0	16	256
8 OUT	ISO	0	16	256
9 IN	ISO	0	16	16
9 OUT	ISO	0	16	16
10 IN	ISO	0	16	16
10 OUT	ISO	0	16	16

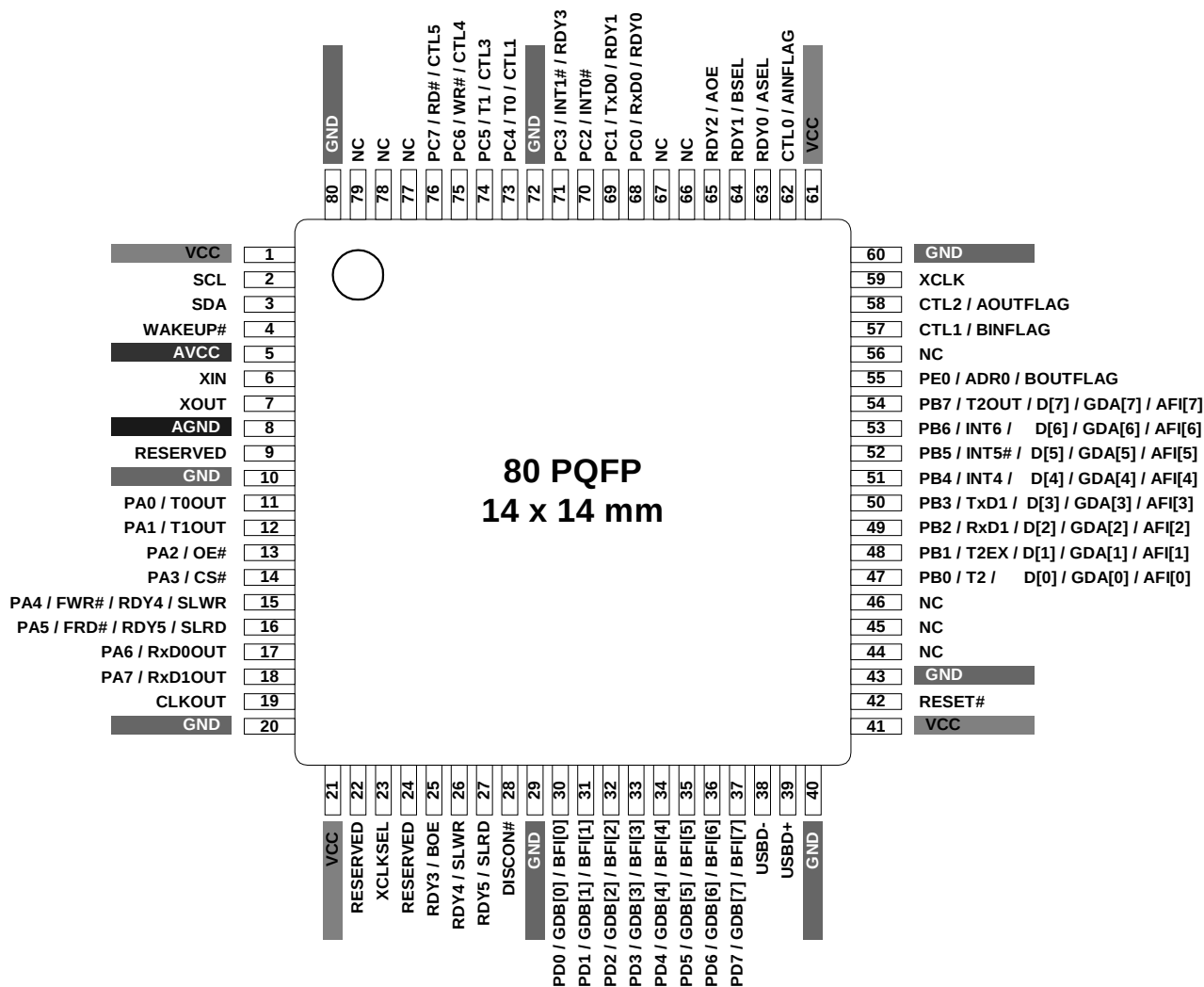
2.9 IBN (In-Bulk-NAK) Interrupts

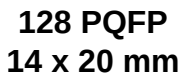
The EZ-USB FX has a special interrupt called In-Bulk-NAK. IBN is triggered when an IN token has been received by an endpoint (the host is attempting to read data), but the SIE NAKed the host (because there is no data in the endpoint) . The 8051 program can identify which endpoint triggered the interrupt by reading the IBNIRQ register, where a bit is set for the endpoint (EP1-IN to EP7-IN) that caused the NAK.

3.0 Pins

3.1 Pin Diagrams







3.2 General Notes About the Pin Description Table

1. **See the EZ-USB FX TRM:** For multiplexed pins, consult the EZ-USB FX TRM (primarily Chapter 4) for details of setting the configuration registers.
2. **Multiply Routed Signals:** In some cases, an internal signal can be routed to more than one pin. For example, in the 80 and 128-pin packages RDY4 can be routed to any combination of (neither, either or both) pins 15 and 26.
3. **Tie Up Unused Inputs:** It is important that the recommendations in the Pin Description Table be followed, especially for inputs. Unused CMOS inputs can oscillate if they are left open (floating), which can cause higher power usage and decreased reliability.
4. **Tie Up Certain Outputs That Are Initially Inputs:** Many alternate functions of the FX multiplexed pins are *similar* to the WR# alternate function (see the PC6 / WR# / CTL4 pin below) in the following respect:

If WR# is chosen as the function of PC6, it should be **pulled up to V_{CC} through a pull-up resistor**. This is to **ensure that WR# is inactive (pulled HIGH) at power-up**, since, before the 8051 can configure this pin to WR#, it defaults to 'PC6 an input' (not driven by the FX pin).

All multiplexed pins that you use should be carefully considered in your circuit design for the effects of the transition through their default configuration at power-up. These are typically (though not always) active LOW signals such as WR#.

The critical time interval to be considered is between:

RESET# deasserted and

the pin driven as an output (immediately after the 8051 code has initialized the port to be an alternate function that is an output).

3.3 Pin Description Table

128	80	52	Name	Type	Default	Description
18	5	5	AVCC	Power	N/A	Analog V_{CC} This signal provides power to the analog section of the chip.
21	8	8	AGND	Power	N/A	Analog Ground. Connect to ground with as short a path as possible.
48	28	18	DISCON#	O/Z	H	Disconnect. This pin can drive HIGH, LOW, or float. DISCON# pin floats when the register bit USBCS.2 is LOW, and drives when it is HIGH. The drive level of the DISCON# pin is the invert of register bit USBCS.3. The DISCON# pin is normally connected to the USB D+ line through a 1500Ω resistor. The EZ-USB FX signals a USB connection by setting USBCS.3=0 (drive 3.3V) and USBCS.2=1 (output enable). The EZ-USB FX signals a USB disconnect by setting USBCS.2=0 which floats the pin and disconnects the 1500Ω resistor from D+.
65	38	24	USBD-	I/O/Z	Z	USB D- Connect to the USB D- signal through a 22 ±5% ohm resistor.
66	39	25	USBD+	I/O/Z	Z	USB D+ Connect to the USB D+ signal through a 22 ±5% ohm resistor.

3.3 Pin Description Table (continued)

128	80	52	Name	Type	Default	Description
105			A0	Output	L	8051 Address Bus This bus is driven at all times, hence, when the 8051 is addressing internal RAM, it reflects the internal address. During DMA transfers that use the RD# and WR# strobes, the address bus contains the incrementing DMA source or destination address for data transferred over D[7..0].
106			A1	Output	L	
107			A2	Output	L	
108			A3	Output	L	
114			A4	Output	L	
115			A5	Output	L	
116			A6	Output	L	
117			A7	Output	L	
118			A8	Output	L	
120			A9	Output	L	
121			A10	Output	L	
122			A11	Output	L	
127			A12	Output	L	
128			A13	Output	L	
1			A14	Output	L	
2			A15	Output	L	8051 Data Bus This bidirectional bus is: - input for bus reads - output for bus writes - high-impedance when inactive. It is active only for external bus accesses, but driven LOW in suspend. The data bus is used for: - external 8051 program and data memory - DMA transfers that use the RD#, FRD#, WR# or FWR# pins as strobes.
8			D0	I/O/Z	Z	
9			D1	I/O/Z	Z	
10			D2	I/O/Z	Z	
11			D3	I/O/Z	Z	
13			D4	I/O/Z	Z	
14			D5	I/O/Z	Z	
15			D6	I/O/Z	Z	
16			D7	I/O/Z	Z	
33			PSEN#	Output	H	Program Store Enable PSEN# strobes LOW when the 8051 fetches a CODE byte from external memory. If EA=0, the 8051 fetches CODE from external memory from 0x1B40 to 0xFFFF. If EA=1, the 8051 fetches CODE from external memory from 0x0000 to 0xFFFF. See EA pin.
41			BKPT	Output	L	Breakpoint This pin goes active (HIGH) when the 8051 address bus matches the BPADDRH/L registers and breakpoints are enabled in the USBBAV register (BPEN=1). If the BPPULSE bit in the USBBAV register is HIGH, BKPT pulses HIGH for eight 24-/48-MHz clocks. If the BPPULSE bit is LOW, BKPT stays HIGH until the 8051 clears the BREAK bit (by writing a 1 to it) in the USBBAV register.
69	42	28	RESET#	Input	N/A	Active LOW Reset This pin resets the entire chip. It is normally tied to V _{CC} through a 10K resistor, and to GND through a 1-μF capacitor. Hysteresis input.

3.3 Pin Description Table (continued)

128	80	52	Name	Type	Default	Description
51			EA	Input	N/A	External Access This pin determines from which memory the 8051 fetches CODE when a CODE fetch is in the lower 8051 address space (CODE addresses 0x0000 to 0x1B3F): If EA=0 the 8051 fetches CODE from internal RAM. If EA=1 the 8051 fetches CODE from external memory (normally used to boot from external memory, for example, boot from Flash). See PSEN# pin. (EA is tied to GND internally in both the 80- and 52-pin packages.)
19	6	6	XIN	Input	N/A	Crystal Input. Connect this signal to a 12-MHz parallel-resonant, fundamental mode crystal and 22–33 pF capacitor to GND. Also connect a 1-MΩ resistor between XIN and XOUT. It is also correct to drive XIN with an external 12 MHz square wave derived from another clock source.
20	7	7	XOUT	Output	N/A	Crystal Output. Connect this signal to a 12-MHz parallel-resonant, fundamental mode crystal and 22–33 pF capacitor to GND. Also connect a 1-MΩ resistor between XIN and XOUT. If an external clock is used to drive XIN, leave this pin open.
34	19	12	CLKOUT	O/Z	24 MHz	Clock Output This is the 24- or 48-MHz clock, the master clock for the 8051, phase locked to the 12-MHz XIN/XOUT clock. (Note: the GPIF always uses a 48 MHz clock or XCLK, regardless of the 8051 clock. See XCLK and XCLKSEL.) The frequency of the 8051 clock is set via a boot EEPROM bit: If Config 0.2 = 0, CLKOUT is 24 MHz. If Config 0.2 = 1, CLKOUT is 48 MHz. CLKOUT may be inverted by setting a boot EEPROM bit CONFIG0.1=1. If no EEPROM is connected to the I²C compatible port (the required pull-up resistors must be present), the Config0 bits default to zero, hence - CLKOUT is 24-MHz - CLKOUT is non-inverted. The 8051 may three-state this output by setting CPUCS.1=1.

3.3 Pin Description Table (continued)

128	80	52	Name	Type	Default	Description
Port A						
25	11		PA0 or T0OUT	I/O/Z	I (PA0)	Multiplexed pin. Function selected by bits: PORTACFG.0 and IFCONFIG.3. PA0 is a bidirectional I/O port pin. T0OUT is an active-HIGH signal from 8051 Timer-counter0. T0OUT outputs a high level for one CLKOUT clock cycle when Timer0 overflows. If Timer0 is operated in mode 3 (two separate timer/counters), T0OUT is active when the low byte timer/counter overflows.
26	12		PA1 or T1OUT	I/O/Z	I (PA1)	Multiplexed pin. Function selected by bits: PORTACFG.1 and IFCONFIG.3. PA1 is a bidirectional I/O port pin. T1OUT is an active-HIGH signal from 8051 Timer-counter1. T1OUT outputs a high level for one CLKOUT clock cycle when Timer1 overflows. If Timer1 is operated in mode 3 (two separate timer/counters), T1OUT is active when the low byte timer/counter overflows.
27	13		PA2 or OE#	I/O/Z	I (PA2)	Multiplexed pin. Function selected by bits: PORTACFG.2 and IFCONFIG.3. PA2 is a bidirectional I/O port pin. OE# is an active-LOW output enable for external memory. If OE# is chosen as the function of this pin, it should be pulled up to V_{CC} through a pull-up resistor. This is to ensure that OE# is inactive (pulled HIGH) at power-up, since, before the 8051 can configure this pin to OE#, it defaults to 'PA2 an input'.
28	14		PA3 or CS#	I/O/Z	I (PA3)	Multiplexed pin. Function selected by: PORTACFG.3 bit only. PA3 is a bidirectional I/O port pin. CS# is an active-LOW chip select for external memory. If CS# is chosen as the function of this pin, it should be pulled up to V_{CC} through a pull-up resistor. This is to ensure that CS# is inactive (pulled HIGH) at power-up, since, before the 8051 can configure this pin to CS#, it defaults to 'PA3 an input'.
29	15	10	PA4 or FWR# or RDY4 or SLWR	I/O/Z	I (PA4)	Multiplexed pin. Function selected by bits: PORTACFG.4, PORTACF2.4 and IFCONFIG[1..0]. PA4 is a bidirectional I/O port pin. FWR# is the write strobe output for an external FIFO connected to the data bus D[7..0]. RDY4 is a GPIF input signal. SLWR is the write strobe input for the slave FIFOs connected to AFI[7..0] and/or BFI[7..0]. If FWR# is chosen as the function of this pin, it should be pulled up to V_{CC} through a pull-up resistor. This is to ensure that FWR# is inactive (pulled HIGH) at power-up, since, before the 8051 can configure this pin to FWR#, it defaults to 'PA4 an input'.

3.3 Pin Description Table (continued)

128	80	52	Name	Type	Default	Description
30	16	11	PA5 or FRD# or RDY5 or SLRD	I/O/Z	I (PA5)	Multiplexed pin. Function selected by bits: PORTACFG.5, PORTACF2.5 and IFCONFIG[1..0]. PA5 is a bidirectional I/O port pin. FRD# is the write strobe output for an external FIFO connected to the data bus D[7..0]. RDY5 is a GPIF input signal. SLRD is the read strobe input for the slave FIFOs connected to AFI[7..0] and/or BFI[7..0]. If FRD# is chosen as the function of this pin, it should be pulled up to V_{CC} through a pull-up resistor. This is to ensure that FRD# is inactive (pulled HIGH) at power-up, since, before the 8051 can configure this pin to FRD#, it defaults to 'PA5 an input'.
31	17		PA6 or RxD0OUT	I/O/Z	I (PA6)	Multiplexed pin. Function selected by bit: PORTACFG.6 only. PA6 is a bidirectional I/O port pin. RxD0OUT is an active-HIGH signal from 8051 UART0. If RxD0OUT is selected and UART0 is in mode 0, this pin provides the output data for UART0 only when it is in sync mode. Otherwise it is a 1.
32	18		PA7 or RxD1OUT	I/O/Z	I (PA7)	Multiplexed pin. Function selected by bit: PORTACFG.7 only. PA7 is a bidirectional I/O port pin. RxD1OUT is an active-HIGH output from 8051 UART1. When RxD1OUT is selected and UART1 is in mode 0, this pin provides the output data for UART1 only when it is in sync mode. In modes 1, 2, and 3, this pin is HIGH.

3.3 Pin Description Table (continued)

128	80	52	Name	Type	Default	Description
Port B						
						The following alternate functions are available on all PORT B pins: D[7..0] is the bidirectional 8051 data bus. GDA[7..0] is the bidirectional GPIF A data bus. AFI[7..0] is the bidirectional A-FIFO data bus.
79	47	29	PB0 or T2 or D[0] or GDA[0] or AFI [0]	I/O/Z	I (PB0)	Multiplexed pin. Function selected by bits: PORTBCFG.0 and IFCONFIG[1..0]. PB0 is a bidirectional I/O port pin. T2 is the active-HIGH T2 input signal to 8051 Timer2, which provides the input to Timer2 when C/T2=1. When C/T2=0, Timer2 does not use this pin.
80	48	30	PB1 or T2EX or D[1] or GDA[1] or AFI [1]	I/O/Z	I (PB1)	Multiplexed pin. Function selected by bits: PORTBCFG.1 and IFCONFIG[1..0]. PB1 is a bidirectional I/O port pin. T2EX is an active-HIGH input signal to the 8051 Timer2. T2EX reloads timer 2 on its falling edge. T2EX is active only if the EXEN2 bit is set in T2CON.
81	49	31	PB2 or RxD1 or D[2] or GDA[2] or AFI [2]	I/O/Z	I (PB2)	Multiplexed pin. Function selected by bits: PORTBCFG.2 and IFCONFIG[1..0]. PB2 is a bidirectional I/O port pin. RxD1 is an active-HIGH input signal for 8051 UART1, which provides data to the UART in all modes.
82	50	32	PB3 or TxD1 or D[3] or GDA[3] or AFI [3]	I/O/Z	I (PB3)	Multiplexed pin. Function selected by bits: PORTBCFG.3 and IFCONFIG[1..0]. PB3 is a bidirectional I/O port pin. TxD1 is an active-HIGH output pin from 8051 UART1, which provides the output clock in sync mode, and the output data in async mode.
83	51	33	PB4 or INT4 or D[4] or GDA[4] or AFI [4]	I/O/Z	I (PB4)	Multiplexed pin. Function selected by bits: PORTBCFG.4 and IFCONFIG[1..0]. PB4 is a bidirectional I/O port pin. INT4 is the 8051 INT4 interrupt request input signal. INT4 is triggered on the rising edge.
84	52	34	PB5 or INT5# or D[5] or GDA[5] or AFI [5]	I/O/Z	I (PB5)	Multiplexed pin. Function selected by bits: PORTBCFG.5 and IFCONFIG[1..0]. PB5 is a bidirectional I/O port pin. INT5# is the 8051 INT5 interrupt request input signal. The INT5 interrupt is triggered on the falling edge of the INT5# input.
85	53	35	PB6 or INT6 or D[6] or GDA[6] or AFI [6]	I/O/Z	I (PB6)	Multiplexed pin. Function selected by bits: PORTBCFG.6 and IFCONFIG[1..0]. PB6 is a bidirectional I/O port pin. INT6 is the 8051 INT6 interrupt request input signal. INT6 is triggered on the rising edge.
86	54	36	PB7 or T2OUT or D[7] or GDA[7] or AFI [7]	I/O/Z	I (PB7)	Multiplexed pin. Function selected by bits: PORTBCFG.7 and IFCONFIG[1..0]. PB7 is a bidirectional I/O port pin. T2OUT is the active-HIGH output signal from 8051 Timer2. T2OUT is active (HIGH) for one clock cycle when Timer/Counter 2 overflows.

3.3 Pin Description Table (continued)

128	80	52	Name	Type	Default	Description
Port C						
110	68	43	PC0 or RxD0 or RDY0	I/O/Z	I (PC0)	Multiplexed pin. Function selected by bits: PORTCCFG.0, PORTCCF2.0 and IFCONFIG[1..0]. PC0 is a bidirectional I/O port pin. RxD0 is the active-HIGH RxD0 input to 8051 UART0, which provides data to the UART in all modes. RDY0 is a GPIF input signal.
111	69	44	PC1 or TxD0 or RDY1	I/O/Z	I (PC1)	Multiplexed pin. Function selected by bits: PORTCCFG.1, PORTCCF2.1 and IFCONFIG[1..0]. PC1 is a bidirectional I/O port pin. TxD0 is the active-HIGH TxD0 output from 8051 UART0, which provides the output clock in sync mode, and the output data in async mode. RDY1 is a GPIF input signal.
112	70	45	PC2 or INT0#	I/O/Z	I (PC2)	Multiplexed pin. Function selected by bit: PORTCCFG.2 only. PC2 is a bidirectional I/O port pin. INT0# is the active-LOW 8051 INT0 interrupt input signal, which is either edge triggered (IT0 = 1) or level triggered (IT0 = 0).
113	71	46	PC3 or INT1# or RDY3	I/O/Z	I (PC3)	Multiplexed pin. Function selected by bits: PORTCCFG.3, PORTCCF2.3 and IFCONFIG[1..0]. PC3 is a bidirectional I/O port pin. INT1# is the active-LOW 8051 INT1 interrupt input signal, which is either edge triggered (IT1 = 1) or level triggered (IT1 = 0). RDY3 is a GPIF input signal.
123	73	48	PC4 or T0 or CTL1	I/O/Z	I (PC4)	Multiplexed pin. Function selected by bits: PORTCCFG.4, PORTCCF2.4 and IFCONFIG[1..0]. PC4 is a bidirectional I/O port pin. T0 is the active-HIGH T0 signal for 8051 Timer0, which provides the input to Timer0 when C/T0 is 1. When C/T0 is 0, Timer0 does not use this bit. CTL1 is a GPIF output signal.
124	74	49	PC5 or T1 or CTL3	I/O/Z	I (PC5)	Multiplexed pin. Function selected by bits: PORTCCFG.5, PORTCCF2.5 and IFCONFIG[1..0]. PC5 is a bidirectional I/O port pin. T1 is the active-HIGH T1 signal for 8051 Timer1, which provides the input to Timer1 when C/T1 is 1. When C/T1 is 0, Timer1 does not use this bit. CTL3 is a GPIF output signal.
125	75	50	PC6 or WR# or CTL4	I/O/Z	I (PC6)	Multiplexed pin. Function selected by bits: PORTCCFG.6, PORTCCF2.6 and IFCONFIG[1..0]. PC6 is a bidirectional I/O port pin. WR# is the active-LOW write strobe output for external memory. CTL4 is a GPIF output signal. If WR# is chosen as the function of this pin, it should be pulled up to V _{CC} through a pull-up resistor. This is to ensure that WR# is inactive (pulled HIGH) at power-up, since, before the 8051 can configure this pin to WR#, it defaults to 'PC6 an input'.

3.3 Pin Description Table (continued)

128	80	52	Name	Type	Default	Description
126	76	51	PC7 or RD# or CTL5	I/O/Z	I (PC7)	Multiplexed pin. Function selected by bits: PORTCCFG.7, PORTCCF2.7 and IFCONFIG[1..0]. PC7 is a bidirectional I/O port pin. RD# is the active-LOW read strobe output for external memory. CTL5 is a GPIF output signal. If RD# is chosen as the function of this pin, it should be pulled up to V_{CC} through a pull-up resistor. This is to ensure that RD# is inactive (pulled HIGH) at power-up, since, before the 8051 can configure this pin to RD#, it defaults to 'PC6 an input'.

3.3 Pin Description Table (continued)

128	80	52	Name	Type	Default	Description
Port D						
						Port D is multiplexed between three sources: PD0–PD7 are bidirectional I/O port pins. GDB[7..0] is the bidirectional GPIF B data bus. BFI[7..0] is the bidirectional B-FIFO data bus.
56	30		PD0 or GDB[0] or BFI [0]	I/O/Z	I (PD0)	Multiplexed pin. Function selected by bits: IFCONFIG[2..0].
57	31		PD1 or GDB[1] or BFI [1]	I/O/Z	I (PD1)	Multiplexed pin. Function selected by bits: IFCONFIG[2..0].
58	32		PD2 or GDB[2] or BFI [2]	I/O/Z	I (PD2)	Multiplexed pin. Function selected by bits: IFCONFIG[2..0].
59	33		PD3 or GDB[3] or BFI [3]	I/O/Z	I (PD3)	Multiplexed pin. Function selected by bits: IFCONFIG[2..0].
60	34		PD4 or GDB[4] or BFI [4]	I/O/Z	I (PD4)	Multiplexed pin. Function selected by bits: IFCONFIG[2..0].
61	35		PD5 or GDB[5] or BFI [5]	I/O/Z	I (PD5)	Multiplexed pin. Function selected by bits: IFCONFIG[2..0].
63	36		PD6 or GDB[6] or BFI [6]	I/O/Z	I (PD6)	Multiplexed pin. Function selected by bits: IFCONFIG[2..0].
64	37		PD7 or GDB[7] or BFI [7]	I/O/Z	I (PD7)	Multiplexed pin. Function selected by bits: IFCONFIG[2..0].

3.3 Pin Description Table (continued)

128	80	52	Name	Type	Default	Description
Port E						
88	55		PE0 or ADR0 or BOUTFLAG	I/O/Z	I (PE0)	Multiplexed pin. Function selected by bits: IFCONFIG[1..0]. PE0 is a bidirectional I/O port pin. ADR0 is a GPIF address output pin. BOUTFLAG is the B-OUT FIFO flag output, which indicates a programmable level of FIFO fullness.
89	Note 2		PE1 or ADR1 or AINFULL	I/O/Z	I (PE1)	Multiplexed pin. Function selected by bits: IFCONFIG[1..0]. PE1 is a bidirectional I/O port pin. ADR1 is a GPIF address output pin. AINFULL is the A-IN FIFO flag output, which indicates FIFO full.
90	Note 2		PE2 or ADR2 or BINFULL	I/O/Z	I (PE2)	Multiplexed pin. Function selected by bits: IFCONFIG[1..0]. PE2 is a bidirectional I/O port pin. ADR2 is a GPIF address output pin. BINFULL is the B-IN FIFO flag output, which indicates FIFO full.
91	Note 2		PE3 or ADR3 or AOUTEMPTY	I/O/Z	I (PE3)	Multiplexed pin. Function selected by bits: IFCONFIG[1..0]. PE3 is a bidirectional I/O port pin. ADR3 is a GPIF address output pin. AOUTEMPTY is the A-OUT FIFO flag output, which indicates FIFO empty.
92	Note 2		PE4 or ADR4 or BOUTEMPTY	I/O/Z	I (PE4)	Multiplexed pin. Function selected by bits: IFCONFIG[1..0]. PE4 is a bidirectional I/O port pin. ADR4 is a GPIF address output pin. BOUTEMPTY is the B-OUT FIFO flag output, which indicates FIFO empty.
93	Note 2		PE5 or CTL3	I/O/Z	I (PE5)	Multiplexed pin. Function selected by bits: IFCONFIG[1..0]. PE5 is a bidirectional I/O port pin. CTL3 is a GPIF output signal.
94	Note 2		PE6 or CTL4	I/O/Z	I (PE6)	Multiplexed pin. Function selected by bits: IFCONFIG[1..0]. PE6 is a bidirectional I/O port pin. CTL4 is a GPIF output signal.
95	Note 2		PE7 or CTL5	I/O/Z	I (PE7)	Multiplexed pin. Function selected by bits: IFCONFIG[1..0]. PE7 is a bidirectional I/O port pin. CTL5 is a GPIF output signal.

3.3 Pin Description Table (continued)

128	80	52	Name	Type	Default	Description
24			ADR5	Output	L	ADR5 is a GPIF address output pin.
102	63		RDY0 or ASEL	Input	X	Multiplexed pin whose function is selected by IFCONFIG[1..0]. RDY0 is a GPIF input signal. ASEL is the select input for the A-IN and A-OUT FIFOs.
103	64		RDY1 or BSEL	Input	X	Multiplexed pin whose function is selected by IFCONFIG[1..0]. RDY1 is a GPIF input signal. BSEL is the select input for the B-IN and B-OUT FIFOs.
104	65	42	RDY2 or AOE	Input	X	Multiplexed pin whose function is selected by IFCONFIG[1..0]. RDY2 is a GPIF input signal. AOE is the output enable input for the A-OUT FIFO.
44	25		RDY3 or BOE	Input	X	Multiplexed pin whose function is selected by IFCONFIG[1..0]. RDY3 is a GPIF input signal. BOE is the output enable input for the B-OUT FIFO.
45	26		RDY4 or SLWR	Input	X	Multiplexed pin whose function is selected by IFCONFIG[1..0]. RDY4 is a GPIF input signal. SLWR is the input-only write strobe for the slave FIFOs connected to AFI[7..0] and/or BFI[7..0].
46	27		RDY5 or SLRD	Input	X	Multiplexed pin whose function is selected by IFCONFIG[1..0]. RDY5 is a GPIF input signal. SLRD is the input-only read strobe for the slave FIFOs connected to AFI[7..0] and/or BFI[7..0].
101	62	41	CTL0 or AINFLAG	Output	X	Multiplexed pin whose function is selected by IFCONFIG[1..0]. CTL0 is a GPIF control output. AINFLAG is the A-IN FIFO flag output which indicates a programmable level of FIFO fullness.
96	57		CTL1 or BINFLAG	Output	X	Multiplexed pin whose function is selected by IFCONFIG[1..0]. CTL1 is a GPIF control output. BINFLAG is the B-IN FIFO flag output which indicates a programmable level of FIFO fullness.
97	58	37	CTL2 or AOUTFLAG	Output	X	Multiplexed pin whose function is selected by IFCONFIG[1..0]. CTL2 is a GPIF control output. AOUTFLAG is the A-OUT FIFO flag output which indicates a programmable level of FIFO fullness.
98	59	38	XCLK	Input	N/A	When the XCLKSEL input is strapped HIGH, XCLK is used for: - synchronously clocking data into the slave FIFOs - a timing reference for all slave FIFO control signals and GPIF.
53		22	Reserved	Input	N/A	Reserved. Connect to Ground.
54		23	Reserved	Input	N/A	Reserved. Connect to Ground.
70			Reserved	Input	N/A	Reserved. Connect to Ground.
71			Reserved	Input	N/A	Reserved. Connect to Ground.
73			Reserved	Input	N/A	Reserved. Connect to Ground.
74			Reserved	Input	N/A	Reserved. Connect to Ground.
76			Reserved	Input	N/A	Reserved. Connect to Ground.
77			Reserved	Input	N/A	Reserved. Connect to Ground.
50		20	Reserved	Power	N/A	Reserved. Must be left open.
49			Reserved	Input	N/A	Reserved. Connect to Ground.
		19	Reserved	Input	N/A	Reserved. Connect to 3.3 V power source.

3.3 Pin Description Table (continued)

128	80	52	Name	Type	Default	Description
7	4	4	WAKEUP#	Input	N/A	USB Wakeup. If the 8051 is in the Suspend state, a LOW LEVEL on this pin starts up the oscillator and interrupts the 8051. Then the 8051 program can (or not) cause an exit from the Suspend state. Holding WAKEUP# LOW inhibits the EZ-USB chip from suspending.
5	2	2	SCL	Open Drain	Z	I ² C compatible Clock. Connect to Vcc with a 1K resistor, even if no I ² C compatible peripheral is attached.
6	3	3	SDA	Open Drain	Z	I ² C compatible Data. Connect to Vcc with a 1K resistor, even if no I ² C compatible peripheral is attached.
38	23	16	XCLKSEL	Input	N/A	HIGH: Use XCLK pin to clock GPIF and slave FIFOs. LOW: Use internal 48-MHz to clock GPIF and slave FIFOs.
39	24	17	Reserved	Input	N/A	Reserved. Connect to Ground.
37	22	15	Reserved	Input	N/A	Reserved. Connect to Ground.
22	9	9	Reserved	Input	N/A	Reserved. Connect to Ground.
4	1	1	V _{CC}	Power	N/A	V _{CC} . Connect to 3.3 V power source.
17			V _{CC}	Power	N/A	V _{CC} . Connect to 3.3 V power source.
36	21	14	V _{CC}	Power	N/A	V _{CC} . Connect to 3.3 V power source.
55			V _{CC}	Power	N/A	V _{CC} . Connect to 3.3 V power source.
68	41	27	V _{CC}	Power	N/A	V _{CC} . Connect to 3.3 V power source.
75			V _{CC}	Power	N/A	V _{CC} . Connect to 3.3 V power source.
100	61	40	V _{CC}	Power	N/A	V _{CC} . Connect to 3.3 V power source.
109			V _{CC}	Power	N/A	V _{CC} . Connect to 3.3 V power source.
3	80	52	GND	Ground	N/A	Ground.
12			GND	Ground	N/A	Ground.
23	10		GND	Ground	N/A	Ground.
35	20	13	GND	Ground	N/A	Ground.
40			GND	Ground	N/A	Ground.
47			GND	Ground	N/A	Ground.
52	29	21	GND	Ground	N/A	Ground.
62			GND	Ground	N/A	Ground.
67	40	26	GND	Ground	N/A	Ground.
72	43		GND	Ground	N/A	Ground.
78			GND	Ground	N/A	Ground.
87			GND	Ground	N/A	Ground.
99	60	39	GND	Ground	N/A	Ground.
119	72	47	GND	Ground	N/A	Ground.

3.3 Pin Description Table (continued)

128	80	52	Name	Type	Default	Description
42	79		N/A	NC	N/A	No-connect. This pin must be left open.
43	44		N/A	NC	N/A	No-connect. This pin must be left open.
	45		N/A	NC	N/A	No-connect. This pin must be left open.
	46		N/A	NC	N/A	No-connect. This pin must be left open.
	56		N/A	NC	N/A	No-connect. This pin must be left open.
	66		N/A	NC	N/A	No-connect. This pin must be left open.
	67		N/A	NC	N/A	No-connect. This pin must be left open.
	77		N/A	NC	N/A	No-connect. This pin must be left open.
	78		N/A	NC	N/A	No-connect. This pin must be left open.

Notes:

- For the 80-pin package, it is recommended practice to add 8051 code that selects the PE[7..0] alternate function, and makes PE[7..0] outputs.

4.0 Register Summary

This table is a summary only. See the EZ-USB FX TRM for details about the meaning and usage of all FX registers.

Addr	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0
FIFO A-IN										
7800	AINDATA	Read Data from FIFO A	D7	D6	D5	D4	D3	D2	D1	D0
7801	AINBC	Input FIFO A Byte Count	0	D6	D5	D4	D3	D2	D1	D0
7802	AINPF	FIFO A-IN Prog. Flag (internal bit)	LTGT	D6	D5	D4	D3	D2	D1	D0
7803	AINPFPIN	FIFO A-IN Prog. Flag (external pin)	LTGT	D6	D5	D4	D3	D2	D1	D0
7804 (reserved)										
FIFO B-IN										
7805	BINDATA	Read Data from FIFO B	D7	D6	D5	D4	D3	D2	D1	D0
7806	BINBC	Input FIFO B Byte Count	0	D6	D5	D4	D3	D2	D1	D0
7807	BINPF	FIFO B-IN Prog. Flag (internal bit)	LTGT	D6	D5	D4	D3	D2	D1	D0
7808	BINPFPIN	FIFO B-IN Prog. Flag (external pin)	LTGT	D6	D5	D4	D3	D2	D1	D0
7809 (reserved)										
FIFO A/B-IN Control										
780A	ABINTF	Input FIFOs Toggle control and flags	INTOG	INSEL	AINPF	AINEF	AINFF	BINPF	BINEF	BINFF
780B	ABINIE	Input FIFO Interrupt Enables	0	0	AINPFIE	AINEFIE	AINFFIE	BINPFIE	BINEFIE	BINFFIE
780C	ABINIRQ	Input FIFO Interrupt Requests	0	0	AINPFIR	AINEFIR	AINFFIR	BINPFIR	BINEFIR	BINFFIR
780D (reserved)										
FIFO A-OUT										
780E	AOUTDATA	Load Output FIFO A	D7	D6	D5	D4	D3	D2	D1	D0
780F	AOUTBC	Output FIFO A Byte Count	0	D6	D5	D4	D3	D2	D1	D0
7810	AOUTPF	FIFO A-OUT Prog. Flag (internal bit)	LTGT	D6	D5	D4	D3	D2	D1	D0
7811	AOUTPFPIN	FIFO A-OUT Programmable Flag (external pin)	LTGT	D6	D5	D4	D3	D2	D1	D0
7812 (reserved)										
FIFO B-OUT										
7813	BOOUTDATA	Load Output FIFO B	D7	D6	D5	D4	D3	D2	D1	D0
7814	BOOUTBC	Output FIFO B Byte Count	0	D6	D5	D4	D3	D2	D1	D0
7815	BOOUTPF	FIFO B-OUT Prog. (internal bit)	LTGT	D6	D5	D4	D3	D2	D1	D0
7816	BOOUTPFPIN	FIFO B-OUT Prog. Flag (external pin)	LTGT	D6	D5	D4	D3	D2	D1	D0
7817 (reserved)										
FIFO A/B OUT Control										
7818	ABOUTF	Output FIFOs Toggle control and flags	OUTTOG	OUTSEL	AOUTPF	AOUTEF	AOUTFF	BOOUTPF	BOOUTEF	BOOUTFF
7819	ABOUTIE	Output FIFO Interrupt Enables	0	0	AOUTPFIE	AOUTEFIE	AOUTFFIE	BOOUTPFIE	BOOUTEFIE	BOOUTFFIE
781A	ABOUTIRQ	Output FIFO Interrupt Requests	0	0	AOUTPFIR	AOUTEFIR	AOUTFFIR	BOOUTPFIR	BOOUTEFIR	BOOUTFFIR

Addr	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0
781B	(reserved)									
	FIFO A/B Global Control									
781C	ABSETUP	FIFO Setup	0	0	ASYNC	DBLIN	0	OUTDLY	0	DBLOUT
781D	ABPOLAR	FIFO Control Signals Polarity	0	0	BOE	AOE	SLRD	SLWR	ASEL	BSEL
781E	ABFLUSH	Write (data=x) to reset all flags	*	*	*	*	*	*	*	*
781F-7823	(reserved)									
7824	WFSELECT	Waveform Selector	SINGLEWR		SINGLERD		FIFOWR		FIFORD	
7825	IDLE_CS	GPIF IDLE State control	DONE	0	0	0	0	0	0	IDLEDRV
7826	IDLECTLOUT	GPIF IDLE CTL states	IOE3	IOE2	IOE1/CTL5	IOE0/CTL4	CTL3	CTL2	CTL1	CTL0
7827	CTLOUTCFG	GPIF CTL Drive mode	TRICTL	0	CTL5	CTL4	CTL3	CTL2	CTL1	CTL0
7828-7829	(reserved)									
782A	GPIFADRL	GPIF Address	*	*	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0
782B	(reserved)									
782C	AINTC	FIFO A In Transfer Count	FITC	Transfer Count						
782D	AOUTTC	FIFO A Out Transfer Count	FITC	Transfer Count						
782E	ATRIG	Trigger a FIFO A RD/WR	*	*	*	*	*	*	*	*
782F	(reserved)									
7830	BINTC	FIFO B In Transfer Count	FITC	Transfer Count						
7831	BOUTTC	FIFO B Out Transfer Count	FITC	Transfer Count						
7832	BTRIG	Trigger a FIFO B RD/WR	*	*	*	*	*	*	*	*
7833	(reserved)									
7834	SGLDATH	GPIF Data High	D15	D14	D13	D12	D11	D10	D9	D8
7835	SGLDATLTRIG	GPIF Data Low and Trigger	D7	D6	D5	D4	D3	D2	D1	D0
7836	SGLDATLN-TRIG	GPIF Data Low and No Trigger	D7	D6	D5	D4	D3	D2	D1	D0
7837	(reserved)									
7838	READY	GPIF Ready flags	INTRDY	SAS	RDY5	RDY4	RDY3	RDY2	RDY1	RDY0
7839	ABORT	Abort current GPIF cycle	*	*	*	*	*	*	*	*
783A	(reserved)									
783B	GENIE	GPIF/DMA Interrupt Enable	0	0	0	0	0	DMADN	GPWR	GPDONE
783C	GENIRQ	GPIF/DMA Interrupt Request	0	0	0	0	0	DMADN	GPWR	GPDONE
783D-7840	(reserved)									
	I/O Ports D, E									
7841	OUTD	Output Port D	OUTD7	OUTD6	OUTD5	OUTD4	OUTD3	OUTD2	OUTD1	OUTD0
7842	PINSD	Input Port D pins	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0
7843	OED	Port D Output Enable	0ED7	0ED6	0ED5	0ED4	0ED3	0ED2	0ED1	0ED0
7844	(reserved)									
7845	OUTE	Output Port E	OUTE7	OUTE6	OUTE5	OUTE4	OUTE3	OUTE2	OUTE1	OUTE0
7846	PINSE	Input Port E pins	PINE7	PINE6	PINE5	PINE4	PINE3	PINE2	PINE1	PINE0
7847	OEE	Port E Output Enable	OEE7	OEE6	OEE5	OEE4	OEE3	OEE2	OEE1	OEE0
7848	(reserved)									
7849	PORTSETUP	Timer0 Clock source, Port-to-SFR mapping	0	0	0	0	0	0	T0CLK	SFRPORT

Addr	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0
784A	IFCONFIG	Select 8/16 bit data bus, configure buses (IF)	52ONE	0	0	0	GSTATE	BUS16	IF1	IF0
784B	PORTACF2	Port A Configuration #2	0	0	SLRD	SLWR	0	0	0	0
784C	PORTCCF2	Port C Configuration #2	CTL5	CTL4	CTL3	CTL1	RDY3	0	RDY1	RDY0
784D-784E (reserved)										
	DMA Control									
784F	DMASRCH	DMA Source H	A15	A14	A13	A12	A11	A10	A9	A8
7850	DMASRCL	DMA Source L	A7	A6	A5	A4	A3	A2	A1	A0
7851	DMADESTH	DMA Destination H	A15	A14	A13	A12	A11	A10	A9	A8
7852	DMADESTL	DMA Destination L	A7	A6	A5	A4	A3	A2	A1	A0
7853 (reserved)										
7854	DMALEN	DMA Transfer Length	D7	D6	D5	D4	D3	D2	D1	D0
7855	DMAGO	Start DMA Transfer	DONE	*	*	*	*	*	*	*
7856 (reserved)										
7857	DMABURST	DMA Burst control	*	*	*	DSTR2	DSTR1	DSTR0	RB	WB
7858	DMAEXTFIFO	Dummy data reg for using RAM as external FIFO	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
7859 - 785C (reserved)										
785D	INT4IVEC	Interrupt 4 Vector	0	1	I4V3	I4V2	I4V1	I4V0	0	0
785E	INT4SETUP	Interrupt 4 Setup	0	0	0	0	0	INT4SFC	INTERNAL	AV4EN
785F-78FF (reserved)										
7900-797F	WFDESC	GPIF Waveform Descriptors								
7980-7B3F (reserved)										
	Endpoint 0-7 Data Buffers									
7B40	OUT7BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7B80	IN7BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7BC0	OUT6BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7C00	IN6BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7C40	OUT5BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7C80	IN5BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7CC0	OUT4BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7D00	IN4BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7D40	OUT3BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7D80	IN3BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7DC0	OUT2BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7E00	IN2BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7E40	OUT1BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7E80	IN1BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7EC0	OUT0BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7F00	IN0BUF	(64 bytes)	d7	d6	d5	d4	d3	d2	d1	d0
7F40-7F5F (reserved)										
	Isochronous Data									
7F60	OUT8DATA	Endpoint 8 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0
7F61	OUT9DATA	Endpoint 9 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0

Addr	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0
7F62	OUT10DATA	Endpoint 10 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0
7F63	OUT11DATA	Endpoint 11 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0
7F64	OUT12DATA	Endpoint 12 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0
7F65	OUT13DATA	Endpoint 13 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0
7F66	OUT14DATA	Endpoint 14 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0
7F67	OUT15DATA	Endpoint 15 OUT Data	d7	d6	d5	d4	d3	d2	d1	d0
7F68	IN8DATA	Endpoint 8 IN Data	d7	d6	d5	d4	d3	d2	d1	d0
7F69	IN9DATA	Endpoint 9 IN Data	d7	d6	d5	d4	d3	d2	d1	d0
7F6A	IN10DATA	Endpoint 10 IN Data	d7	d6	d5	d4	d3	d2	d1	d0
7F6B	IN11DATA	Endpoint 11 IN Data	d7	d6	d5	d4	d3	d2	d1	d0
7F6C	IN12DATA	Endpoint 12 IN Data	d7	d6	d5	d4	d3	d2	d1	d0
7F6D	IN13DATA	Endpoint 13 IN Data	d7	d6	d5	d4	d3	d2	d1	d0
7F6E	IN14DATA	Endpoint 14 IN Data	d7	d6	d5	d4	d3	d2	d1	d0
7F6F	IN15DATA	Endpoint 15 IN Data	d7	d6	d5	d4	d3	d2	d1	d0
Isochronous Byte Counts										
7F70	OUT8BCH	EP8 Out Byte Count H	0	0	0	0	0	0	d9	d8
7F71	OUT8BCL	EP8 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0
7F72	OUT9BCH	EP9 Out Byte Count H	0	0	0	0	0	0	d9	d8
7F73	OUT9BCL	EP9 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0
7F74	OUT10BCH	EP10 Out Byte Count H	0	0	0	0	0	0	d9	d8
7F75	OUT10BCL	EP10 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0
7F76	OUT11BCH	EP11 Out Byte Count H	0	0	0	0	0	0	d9	d8
7F77	OUT11BCL	EP11 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0
7F78	OUT12BCH	EP12 Out Byte Count H	0	0	0	0	0	0	d9	d8
7F79	OUT12BCL	EP12 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0
7F7A	OUT13BCH	EP13 Out Byte Count H	0	0	0	0	0	0	d9	d8
7F7B	OUT13BCL	EP13 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0
7F7C	OUT14BCH	EP14 Out Byte Count H	0	0	0	0	0	0	d9	d8
7F7D	OUT14BCL	EP14 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0
7F7E	OUT15BCH	EP15 Out Byte Count H	0	0	0	0	0	0	d9	d8
7F7F	OUT15BCL	EP15 Out Byte Count L	d7	d6	d5	d4	d3	d2	d1	d0
7F80-7F91 (reserved)										
CPU Registers										
7F92	CPUCS	Control & Status	rv3	rv2	rv1	rv0	24/48	CLKINV	CLKOUT OE	8051RES
7F93	PORTACFG	Port A Configuration	RxD1out	RxD0out	FRD	FWR	CS	OE	T1out	T0out
7F94	PORTBCFG	Port B Configuration	T2OUT	INT6	INT5	INT4	TxD1	RxD1	T2EX	T2
7F95	PORTCCFG	Port C Configuration	RD	WR	T1	T0	INT1	INT0	TxD0	RxD0
Input-Output Port Registers										
7F96	OUTA	Output Register A	OUTA7	OUTA6	OUTA5	OUTA4	OUTA3	OUTA2	OUTA1	OUTA0
7F97	OUTB	Output Register B	OUTB7	OUTB6	OUTB5	OUTB4	OUTB3	OUTB2	OUTB1	OUTB0
7F98	OUTC	Output Register C	OUTC7	OUTC6	OUTC5	OUTC4	OUTC3	OUTC2	OUTC1	OUTC0
7F99	PINSA	Port Pins A	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0
7F9A	PINSB	Port Pins B	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0
7F9B	PINSC	Port Pins C	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0

Addr	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0
7F9C	OEA	Output Enable A	OEA7	OEA6	OEA5	OEA4	OEA3	OEA2	OEA1	OEA0
7F9D	OEB	Output Enable B	OEB7	OEB6	OEB5	OEB4	OEB3	OEB2	OEB1	OEB0
7F9E	OEC	Output Enable C	OEC7	OEC6	OEC5	OEC4	OEC3	OEC2	OEC1	OEC0
	Isochronous Control/Status Registers									
7FA0	ISOERR	ISO OUT Endpoint Error	ISO15 ERR	ISO14 ERR	ISO13 ERR	ISO12 ERR	ISO11 ERR	ISO10 ERR	ISO9 ERR	ISO8 ERR
7FA1	ISOCTL	Isochronous Control	*	*	*	*	PPSTAT	0	0	ISODISAB
7FA2	ZBCOUT	Zero Byte Count bits	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8
7FA3 (reserved)										
7FA4 (reserved)										
	I²C compatible Registers									
7FA5	I2CS	Control & Status	START	STOP	LASTRD	ID1	ID0	BERR	ACK	DONE
7FA6	I2DAT	Data	d7	d6	d5	d4	d3	d2	d1	d0
7FA7	I2CMODE	STOP Int Enable, I ² C compatible bus speed	0	0	0	0	0	0	STOPIE	400KHZ
	Interrupts									
7FA8	IVC	Interrupt Vector	0	IV4	IV3	IV2	IV1	IV0	0	0
7FA9	IN07IRQ	EPIN Interrupt Request	IN7IR	IN6IR	IN5IR	IN4IR	IN3IR	IN2IR	IN1IR	IN0IR
7FAA	OUT07IRQ	EPOUT Interrupt Request	OUT7IR	OUT6IR	OUT5IR	OUT4IR	OUT3IR	OUT2IR	OUT1IR	OUT0IR
7FAB	USBIRQ	USB Interrupt Request	0	0	IBNIR	URESIR	SUSPIR	SUTOKIR	SOFIR	SUDAVIR
7FAC	IN07IEN	EP0–7IN Int Enables	IN7IEN	IN6IEN	IN5IEN	IN4IEN	IN3IEN	IN2IEN	IN1IEN	IN0IEN
7FAD	OUT07IEN	EP0–7OUT Int Enables	OUT7IEN	OUT6IEN	OUT5IEN	OUT4IEN	OUT3IEN	OUT2IEN	OUT1IEN	OUT0IEN
7FAE	USBIEN	USB Int Enables	0	0	IBNIE	URESIE	SUSPIE	SUTOKIE	SOFIE	SUDAVIE
7FAF	USBBV	Breakpoint & Autovector	*	*	*	INT2SFC	BREAK	BPPULSE	BPEN	AVEN
7FB0	IBNID	IN-Bulk-NAK ID	EP7IN	EP6IN	EP5IN	EP4IN	EP3IN	EP2IN	EP1IN	EP0IN
7FB1	IBNMASK	IN-Bulk-NAK Intr. mask	EP7IN	EP6IN	EP5IN	EP4IN	EP3IN	EP2IN	EP1IN	EP0IN
7FB2	BPADDRH	Breakpoint Address H	A15	A14	A13	A12	A11	A10	A9	A8
7FB3	BPADDRL	Breakpoint Address L	A7	A6	A5	A4	A3	A2	A1	A0
	Bulk Endpoints 0–7									
7FB4	EP0CS	Control & Status	*	*	*	*	OUTBSY	INBSY	HSNAK	EP0STALL
7FB5	IN0BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FB6	IN1CS	Control & Status	*	*	*	*	*	*	in1bsy	in1stl
7FB7	IN1BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FB8	IN2CS	Control & Status	*	*	*	*	*	*	in2bsy	in2stl
7FB9	IN2BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FBA	IN3CS	Control & Status	*	*	*	*	*	*	in3bsy	in3stl
7FBB	IN3BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FBC	IN4CS	Control & Status	*	*	*	*	*	*	in4bsy	in4stl
7FBD	IN4BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FBE	IN5CS	Control & Status	*	*	*	*	*	*	in5bsy	in5stl
7FBF	IN5BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FC0	IN6CS	Control & Status	*	*	*	*	*	*	in6bsy	in6stl
7FC1	IN6BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FC2	IN7CS	Control & Status	*	*	*	*	*	*	in7bsy	in7stl
7FC3	IN7BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0

Addr	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0
7FC4	(reserved)									
7FC5	OUT0BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FC6	OUT1CS	Control & Status	*	*	*	*	*	*	out1bsy	out1stl
7FC7	OUT1BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FC8	OUT2CS	Control & Status	*	*	*	*	*	*	out2bsy	out2stl
7FC9	OUT2BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FCA	OUT3CS	Control & Status	*	*	*	*	*	*	out3bsy	out3stl
7FCB	OUT3BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FCC	OUT4CS	Control & Status	*	*	*	*	*	*	out4bsy	out4stl
7FCD	OUT4BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FCE	OUT5CS	Control & Status	*	*	*	*	*	*	out5bsy	out5stl
7FCF	OUT5BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FD0	OUT6CS	Control & Status	*	*	*	*	*	*	out6bsy	out6stl
7FD1	OUT6BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FD2	OUT7CS	Control & Status	*	*	*	*	*	*	out7bsy	out7stl
7FD3	OUT7BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FC5	OUT0BC	Byte Count	*	d6	d5	d4	d3	d2	d1	d0
7FC6	OUT1CS	Control & Status	*	*	*	*	*	*	out1bsy	out1stl
	Global USB Registers									
7FD4	SUDPTRH	Setup Data Ptr H	A15	A14	A13	A12	A11	A10	A9	A8
7FD5	SUDPTL	Setup Data Ptr L	A7	A6	A5	A4	A3	A2	A1	A0
7FD6	USBCS	USB Control & Status	WakeSRC	*	*	*	DisCon	DiscOE	ReNum	SIGR-SUME
7FD7	TOGCTL	Toggle Control	Q	S	R	IO	0	EP2	EP1	EP0
7FD8	USBFRAMEL	Frame Number L	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0
7FD9	USBFRAMEH	Frame Number H	0	0	0	0	0	FC10	FC9	FC8
7FDA	(reserved)									
7FDB	FNADDR	Function Address	0	FA6	FA5	FA4	FA3	FA2	FA1	FA0
7FDC	(reserved)									
7FDD	USBPAIR	Endpoint Control	ISOsend0	*	PR6OUT	PR4OUT	PR2OUT	PR6IN	PR4IN	PR2IN
7FDE	IN07VAL	Input Endpoint 0–7 valid	IN7VAL	IN6VAL	IN5VAL	IN4VAL	IN3VAL	IN2VAL	IN1VAL	1
7FDF	OUT07VAL	Output Endpoint 0–7 valid	OUT7VAL	OUT6VAL	OUT5VAL	OUT4VAL	OUT3VAL	OUT2VAL	OUT1VAL	1
7FE0	INISOVAL	Input EP 8–15 valid	IN15VAL	IN14VAL	IN13VAL	IN12VAL	IN11VAL	IN10VAL	IN9VAL	IN8VAL
7FE1	OUTISOVAL	Output EP 8–15 valid	OUT15VAL	OUT14VAL	OUT13VAL	OUT12VAL	OUT11VAL	OUT10VAL	OUT9VAL	OUT8VAL
7FE2	FASTXFR	Fast Transfer Mode	FISO	FBLK	RPOL	RMOD1	RMOD0	WPOL	WMOD1	WMOD0
7FE3	AUTOPTRH	Auto-Pointer H	A15	A14	A13	A12	A11	A10	A9	A8
7FE4	AUTOPTL	Auto-Pointer L	A7	A6	A5	A4	A3	A2	A1	A0
7FE5	AUTODATA	Auto Pointer Data	D7	D6	D5	D4	D3	D2	D1	D0
7FE6-7FE7	(reserved)									
	Setup Data									
7FE8	SETUPDAT	8 bytes of SETUP data	d7	d6	d5	d4	d3	d2	d1	d0
	Isochronous FIFO Sizes									
7FF0	OUT8ADDR	Endpt 8 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0
7FF1	OUT9ADDR	Endpt 9 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0

Addr	Name	Description	D7	D6	D5	D4	D3	D2	D1	D0
7FF2	OUT10ADDR	Endpt 10 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0
7FF3	OUT11ADDR	Endpt 11 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0
7FF4	OUT12ADDR	Endpt 12 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0
7FF5	OUT13ADDR	Endpt 13 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0
7FF6	OUT14ADDR	Endpt 14 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0
7FF7	OUT15ADDR	Endpt 15 OUT Start Addr	A9	A8	A7	A6	A5	A4	0	0
7FF8	IN8ADDR	Endpt 8 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0
7FF9	IN9ADDR	Endpt 9 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0
7FFA	IN10ADDR	Endpt 10 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0
7FFB	IN11ADDR	Endpt 11 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0
7FFC	IN12ADDR	Endpt 12 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0
7FFD	IN13ADDR	Endpt 13 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0
7FFE	IN14ADDR	Endpt 14 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0
7FFF	IN15ADDR	Endpt 15 IN Start Addr	A9	A8	A7	A6	A5	A4	0	0

* - register bit is not used and undefined if read.

5.0 Absolute Maximum Ratings

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Supplied	0°C to +70°C
Supply Voltage on V_{CC} relative to GND	–0.5V to +4.0V
DC Input Voltage	–0.5V to 5.25V
DC Voltage Applied to Outputs in High Z State	–0.5V to $V_{CC}+0.5V$
Power Dissipation	500 mW
Static Discharge Voltage	>2 KV
Latch-up Current	>200 mA
Max Output Sink Current	10 mA

6.0 Operating Conditions

T_A (Ambient Temperature Under Bias)	0°C to +70°C
Supply Voltage	+3.0V to +3.6V
Ground Voltage	0V
F_{OSC} (Oscillator or Crystal Frequency)	12 MHz $\pm$ 0.20% ^[3]

7.0 DC Characteristics

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		3.0		3.6	V
V_{IH}	Input High Voltage		2		5.25	V
V_{IL}	Input Low Voltage		–0.5		0.8	V
I_I	Input Leakage Current	$0 < V_{IN} < V_{CC}$			± 10	μA
V_{OH}	Output Voltage High	$I_{OUT} = 1.6$ mA	2.4			V
V_{OL}	Output Low Voltage	$I_{OUT} = -1.6$ mA			0.4	V
C_{IN}	Input Pin Capacitance				10	pF
I_{SUSP}	Suspend Current			120		μA
I_{CC}	Supply Current	8051 running, connected to USB		35		mA
USB Transceiver						
V_{OH}	Output Voltage High	$I_{OUT} = 1.6$ mA	2.8		3.6	V
V_{OL}	Output Low Voltage	$I_{OUT} = -1.6$ mA	0.0		0.3	V
R_{pH}	Output Impedance (HIGH state)	Includes external 22 Ω $\pm 5\%$ resistor	28		44	Ω
R_{pL}	Output Impedance (LOW state)	Includes external 22 Ω $\pm 5\%$ resistor	28		44	Ω
I_i	Input Leakage Current	$V_{CC} = 3.6V$; $V_I = 5.5V$ or GND; not for I/O pins		± 0.1	± 5	μA
I_{oz}	Three-State Output OFF-State Current	$V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND			± 10	μA

Note:

- The USB Specification requires that the full-speed data rate when transmitting is 12.000 Mb/s $\pm 0.25\%$ (2,500 ppm). Circuitry between the oscillator and the USB (the PLL, etc.) can introduce frequency error in addition to the oscillator or crystal error. Hence, the tolerance of F_{OSC} must be tighter than $\pm 0.25\%$ to guarantee $\pm 0.25\%$ when transmitting on the USB.

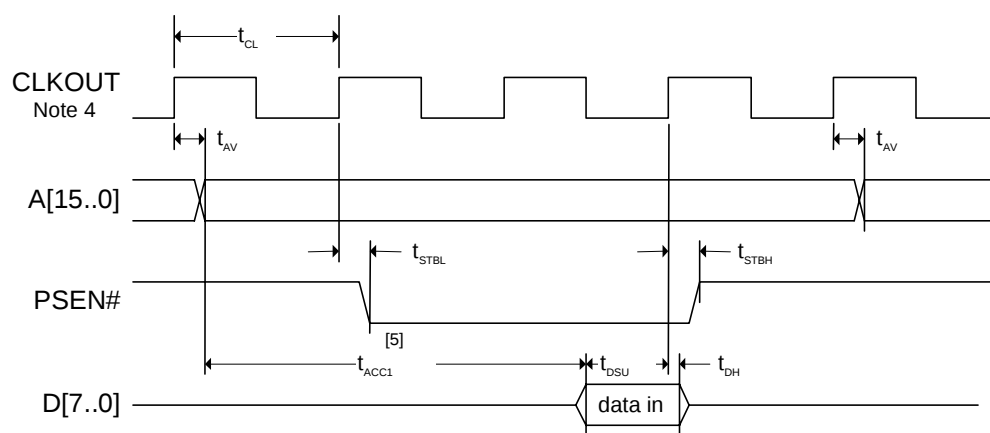
8.0 AC Electrical Characteristics

8.1 USB Transceiver

Specified Conditions: Per Table 7-9 *Full-speed Source Electrical Characteristics* Revision 2.0 of the USB specification.

Parameter	Description	Min.	Max.	Unit
T_{rise}	Rise and Fall Times Full Speed	4	20	ns
T_{fall}		4	20	ns
t_{RFM}	Rise/Fall Time Matching	90	110	%
V_{cr}	Crossover Point	1.3	2.0	V

8.2 Program Memory Read



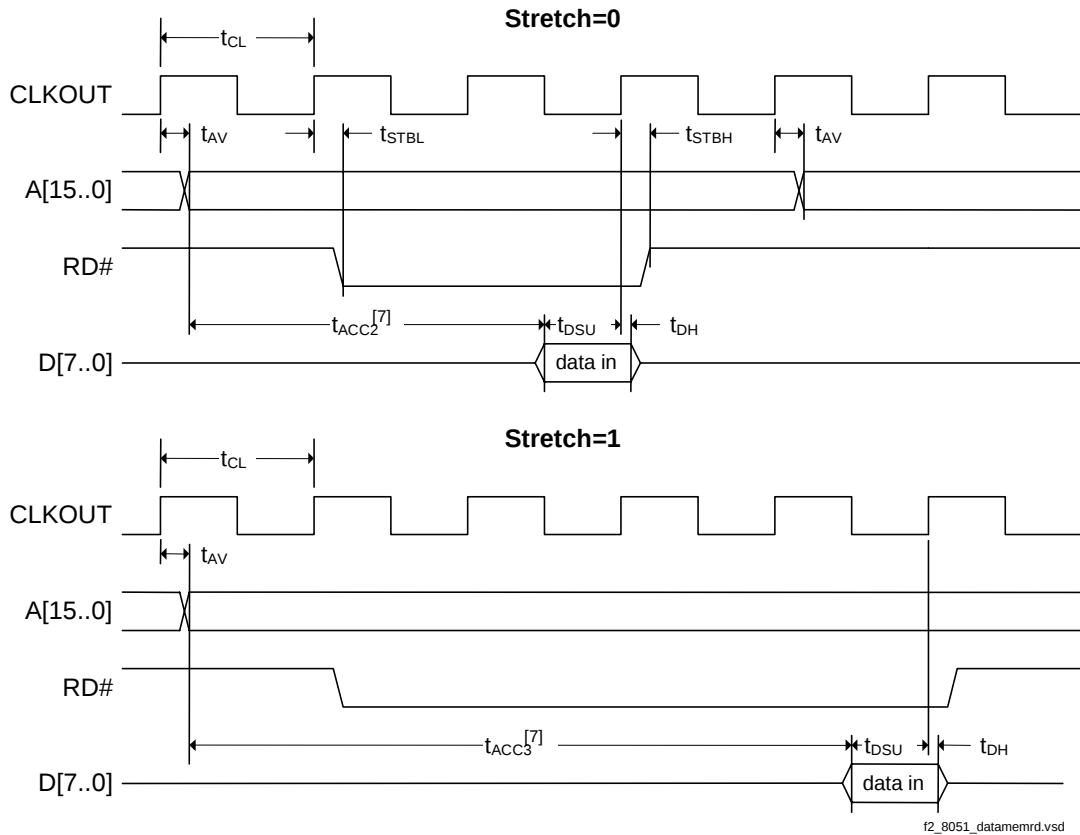
f1_8051_pgmemrd.vsd

Parameter	Description	Min.	Typ.	Max.	Unit	Notes
t_{CL}	1/CLKOUT Frequency		41.66		ns	24 MHz
			20.83		ns	48 MHz
t_{AV}	Delay from Clock to Valid Address	0		10	ns	
t_{STBL}	Clock to PSEN# Low	0		8	ns	
t_{STBH}	Clock to PSEN# High	0		8	ns	
t_{DSU}	Data Set-up to Clock	10			ns	
t_{DH}	Data Hold Time	0			ns	

Notes:

- CLKOUT is shown with positive polarity.
- t_{ACC1} is computed from the above parameters as follows:
 $t_{ACC1}(24\text{ MHz}) = 3 \cdot t_{CL} - t_{AV} - t_{DSU} = 106\text{ ns}$
 $t_{ACC1}(48\text{ MHz}) = 3 \cdot t_{CL} - t_{AV} - t_{DSU} = 44\text{ ns}$
- During Program Memory Read, WR#, RD#, FWR#, and FRD# are driven HIGH (deasserted).

8.3 Data Memory Read



Parameter	Description	Min.	Typ.	Max.	Unit	Notes
t_{CL}	1/CLKOUT Frequency		41.66		ns	24 MHz
			20.83		ns	48 MHz
t_{AV}	Delay from Clock to Valid Address	0		10	ns	
t_{STBL}	Clock to RD Low	0		8	ns	
t_{STBH}	Clock to RD High	0		8	ns	
t_{DSU}	Data Set-up to Clock	10			ns	
t_{DH}	Data Hold Time	0			ns	

Notes:

7. t_{ACC2} and t_{ACC3} are computed from the above parameters as follows:

$$t_{ACC2}(24 \text{ MHz}) = 3 \cdot t_{CL} - t_{AV} - t_{DSU} = 106 \text{ ns}$$

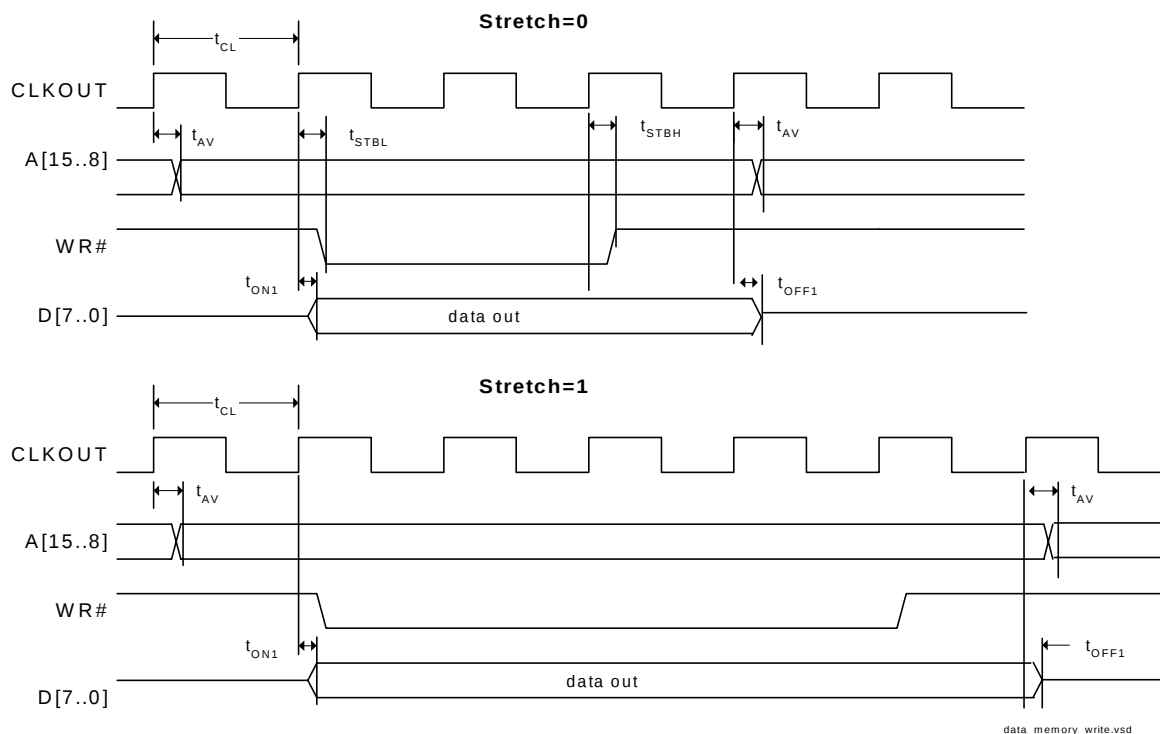
$$t_{ACC2}(48 \text{ MHz}) = 3 \cdot t_{CL} - t_{AV} - t_{DSU} = 44 \text{ ns}$$

$$t_{ACC3}(24 \text{ MHz}) = 5 \cdot t_{CL} - t_{AV} - t_{DSU} = 188 \text{ ns}$$

$$t_{ACC3}(48 \text{ MHz}) = 5 \cdot t_{CL} - t_{AV} - t_{DSU} = 85 \text{ ns}$$

8. During Data Memory Read, WR#, PSEN#, FWR#, and FRD# are driven HIGH (deasserted).

8.4 Data Memory Write

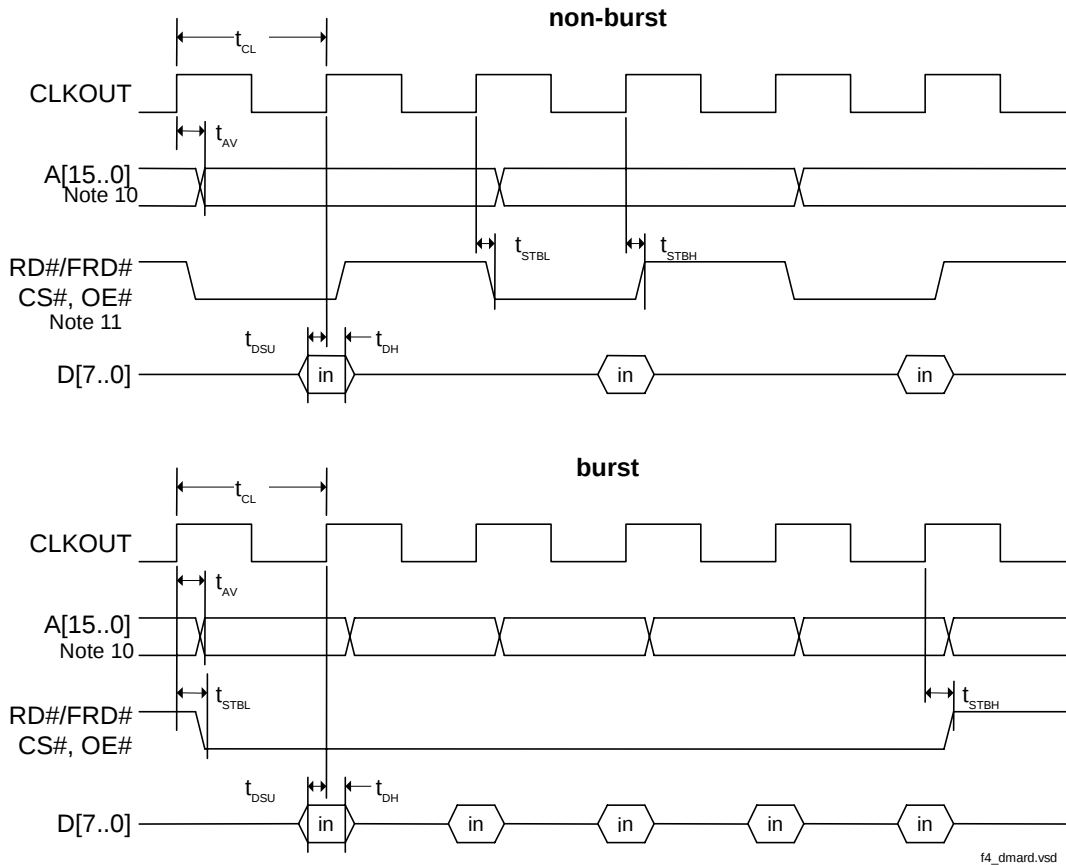


Parameter	Description	Min.	Max.	Unit	Notes
t_{AV}	Delay from Clock to Valid Address	0	10	ns	
t_{STBL}	Clock to WR Pulse Low	0	8	ns	
t_{STBH}	Clock to WR Pulse High	0	8	ns	
t_{ON1}	Clock to Data Turn-on	0	7	ns	
t_{OFF1}	Clock to Data Hold Time	-2	7	ns	

Note:

9. During Data Memory Write, RD#, PSEN#, OE#, FWR#, and FRD# are driven HIGH (deasserted).

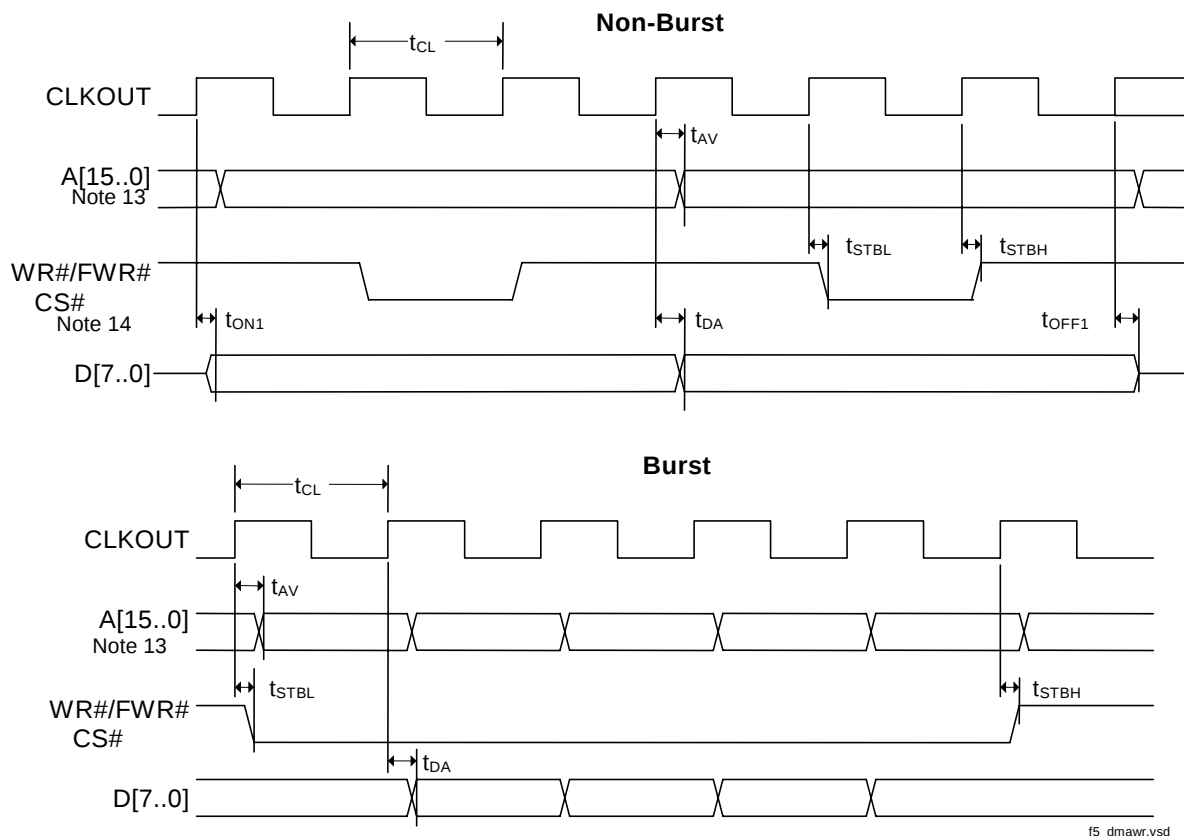
8.5 DMA Read



Parameter	Description	Min.	Max.	Unit	Notes
t_{AV}	Delay from Clock to Valid Address	0	10	ns	
t_{STBL}	Clock to Strobe Low	0	8	ns	Non-burst
t_{STBH}	Clock to Strobe High	0	8	ns	Non-burst
t_{DSU}	Data to Clock Set-up	10		ns	
t_{DH}	Clock to Data Hold	0		ns	

Notes:

10. The address bus is not used in external FIFO transfers that use FRD#.
11. This is the maximum data rate. The strobes are programmable for longer access times.
12. During DMA Read, WR#, PSEN#, FWR#, and FRD# are driven HIGH (deasserted).

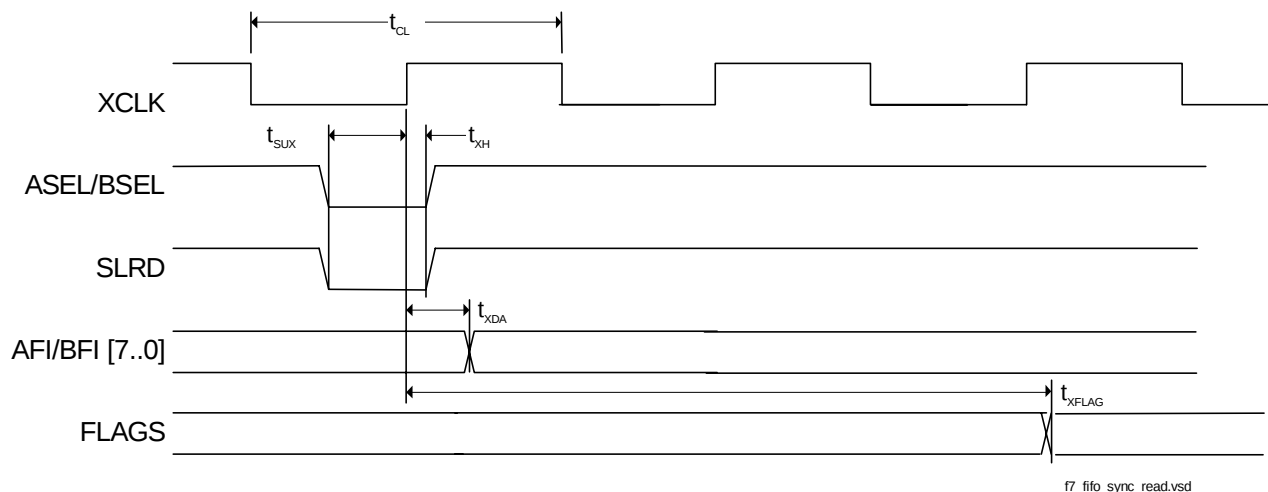
8.6 DMA Write


Parameter	Description	Min.	Max.	Unit	Notes
t_{AV}	Clock to Address Valid	0	10	ns	
t_{STBL}	Clock to Strobe Low	0	8	ns	Non-burst
t_{STBH}	Clock to Strobe High	0	8	ns	Non-burst
t_{DA}	Clock to Valid Data	0	12	ns	
t_{ON1}	Clock to Data Turn-on	0	7	ns	
t_{OFF1}	Clock to Data Hold Time	-2	7	ns	

Notes:

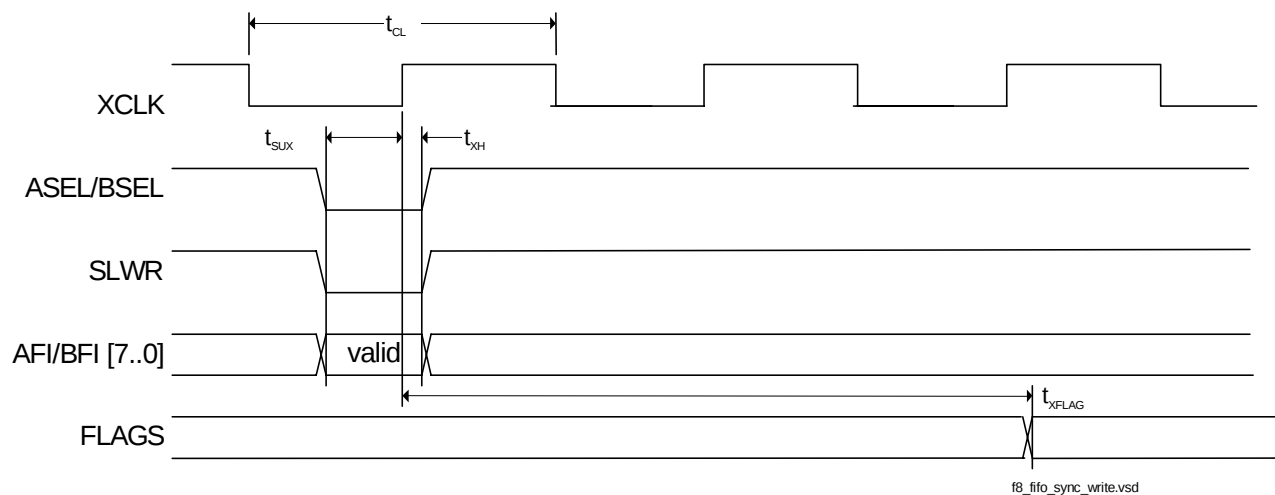
13. The address bus is not used in external FIFO transfers (FWR# strobe).
14. This is the maximum data rate. The WR/FWR pulses are programmable for longer access times.
15. During DMA Write, RD#, PSEN#, OE#, FWR#, and FRD# are driven HIGH (deasserted).

8.7 Slave FIFOs—Synchronous Read



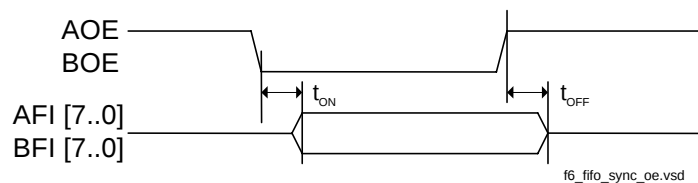
Parameter	Description	Min.	Max.	Unit
t_{SUX}	Strobe & Sel to External Clock Setup Time	9		ns
t_{XH}	External Clock to Strobe & Sel Hold Time	6		ns
t_{XDA}	Clock to A/B FIFO data		13	ns
t_{XFLAG}	Clock to FIFO flag		$2t_{CL}+11$	ns

8.8 Slave FIFOs—Synchronous Write



Parameter	Description	Min.	Typ.	Max.	Unit
t_{CL}	CLKOUT Period		41.66		ns
			20.83		ns
t_{SUX}	Sel, Strobe & Data Setup to External Clock	9			ns
t_{XH}	External Clock to Sel, Strobe & Data Hold Time	2			ns
t_{XFLAG}	External Clock to FIFO Flag			$2t_{CL}+11$	ns

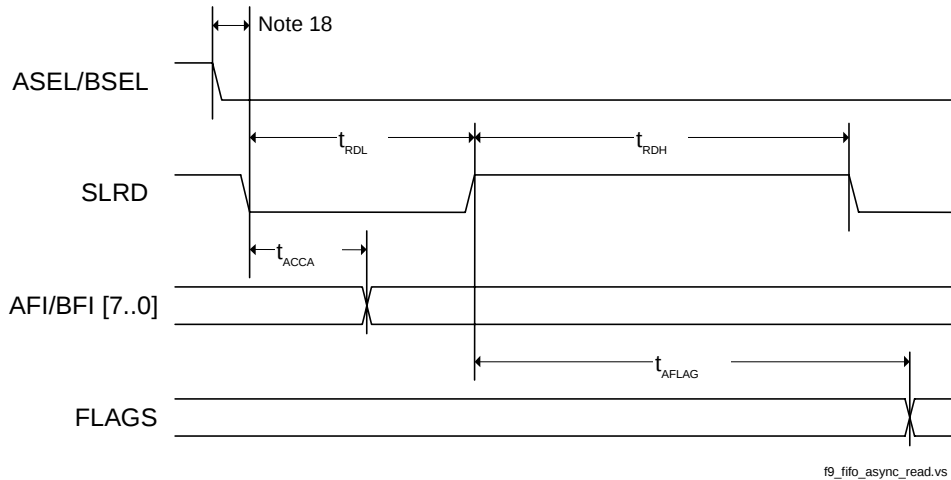
8.9 Slave FIFOs—Output Enables



Parameter	Description	Min.	Max.	Unit
t_{ON}	FIFO Data Bus Turn-on Time	0	10	ns
t_{OFF}	FIFO Data Bus Turn-off Time	0	10	ns

8.10 Slave FIFOs—Asynchronous Read

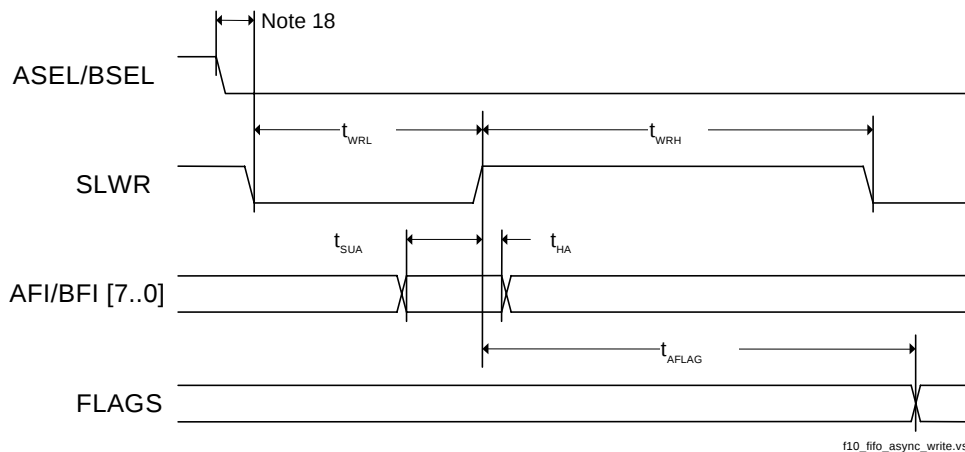
See notes 16 and 17 below, which apply to this entire timing diagram.



Parameter	Description	Min.	Max.	Unit	Notes
t_{RDL}	SLRD Strobe Active	30		ns	
t_{RDH}	SLRD Strobe Inactive	70		ns	
		90		ns	double byte mode
t_{ACCA}	Read Active to FIFO Data Valid		40	ns	
t_{AFLAG}	SLRD Inactive to FIFO Flag		95	ns	

8.11 Slave FIFOs—Asynchronous Write

See notes 16 and 17 below, which apply to this entire timing diagram.



Parameter	Description	Min.	Max.	Unit
t_{WRL}	Slave Write Strobe Active	30		ns
t_{WRH}	Slave Write Strobe Inactive	70		ns
t_{SUA}	Async Data Set-up Time to Write Strobe Inactive	10		ns
t_{HA}	Async Data Hold Time to Write Strobe Inactive	5		ns
t_{AFLAG}	Async Write Strobe Inactive to FIFO Flag Valid		95	ns

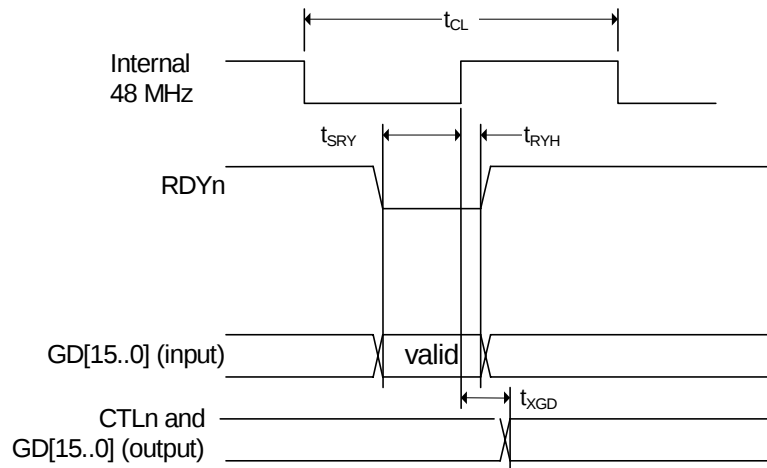
Notes:

16. The timing diagram assumes OEA/OEB is active.

17. The read operation begins when both A/BSEL and SLRD are active, and ends when either is inactive.

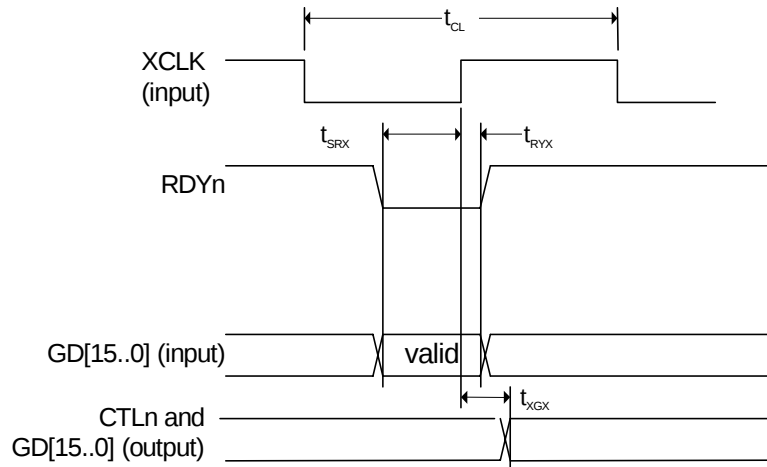
18. The polarities of ASEL/BSEL and SLRD are programmable. Active-LOW is shown.

8.12 GPIF - Clocked with Fixed 48 MHz Internal Clock



Parameter	Description	Min.	Typ.	Max.	Unit
t_{SRY}	Set-up Time: RDYn and GPIF Data to External Clock	9			ns
t_{RYH}	Hold Time: External Clock to RDYn and GPIF Data	2			ns
t_{XGD}	Clock to GPIF Data and CTLn Output			13	ns
t_{cl}	Clock Period		20.83		ns

8.13 GPIF- Clocked with XCLK



Parameter	Description	Min.	Max.	Unit
t_{SRX}	Set-up Time: RDYn and GPIF Data to External Clock	9		ns
t_{RYX}	Hold Time: External Clock to RDYn and GPIF Data	2		ns
t_{XGX}	Clock to GPIF Data and CTLn Output		13	ns
t_{cl}	XCLK Period	21 ^[19]	200 ^[19]	ns

Note:

19. XCLK must be greater than or equal to 5 MHz, and *less than (but not equal to)* 48 MHz

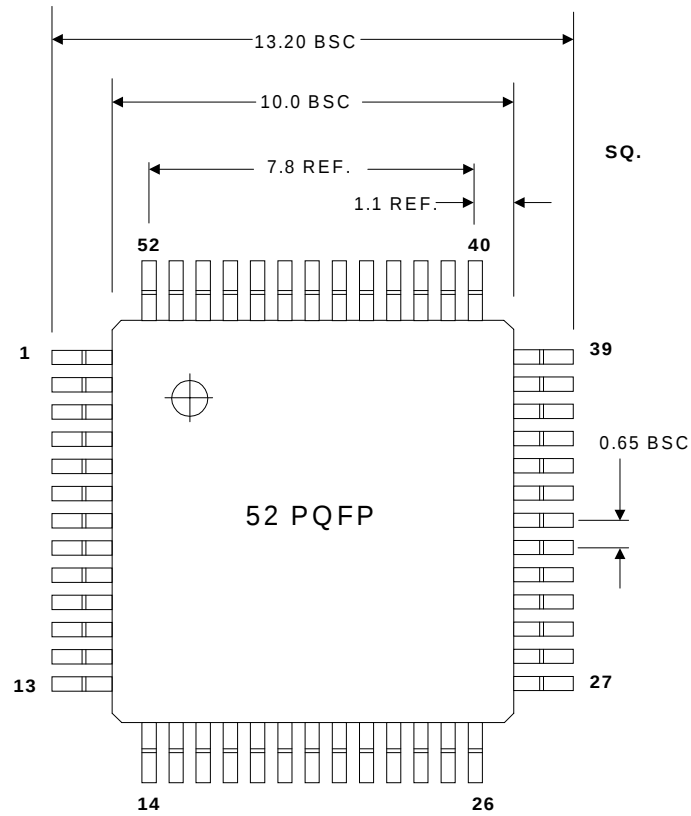
9.0 Package Diagrams

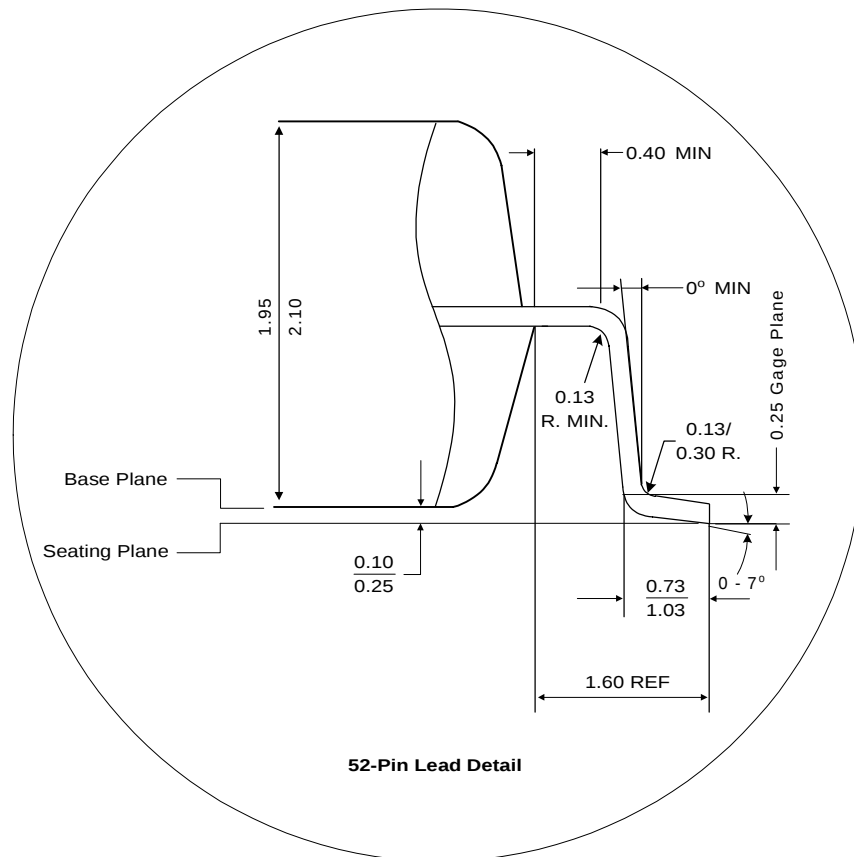
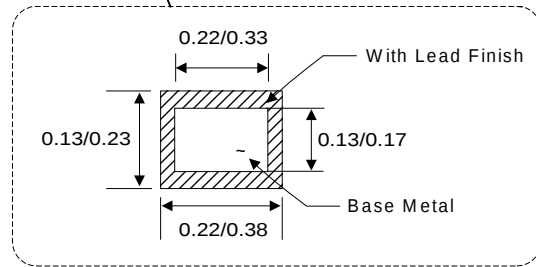
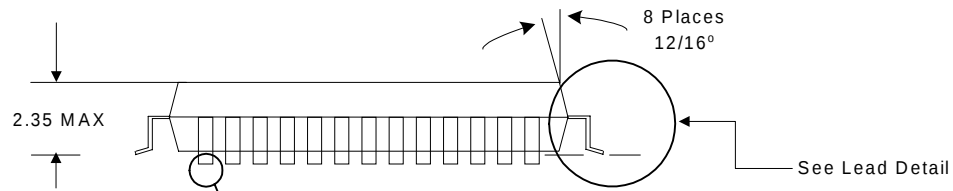
Key (for all Package Diagrams):

BSC = Basic Standard Configuration

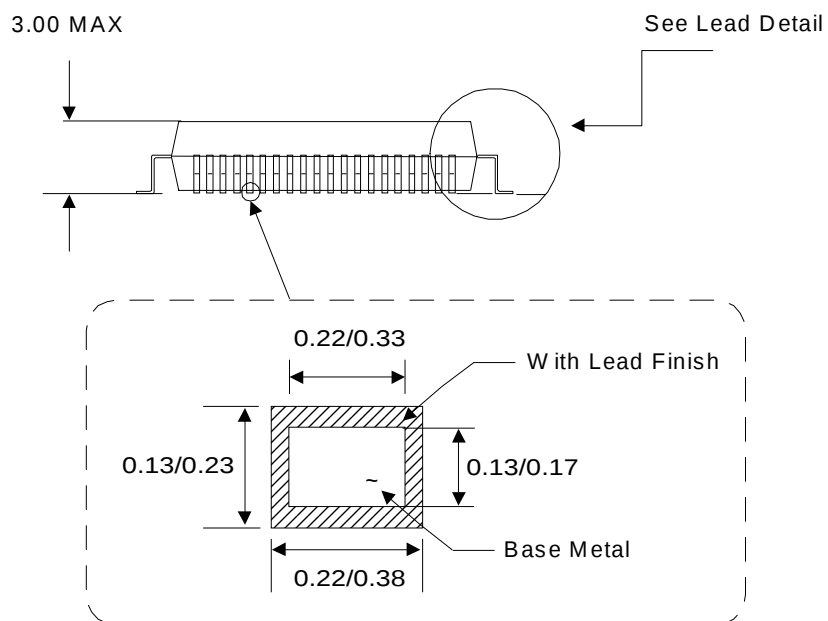
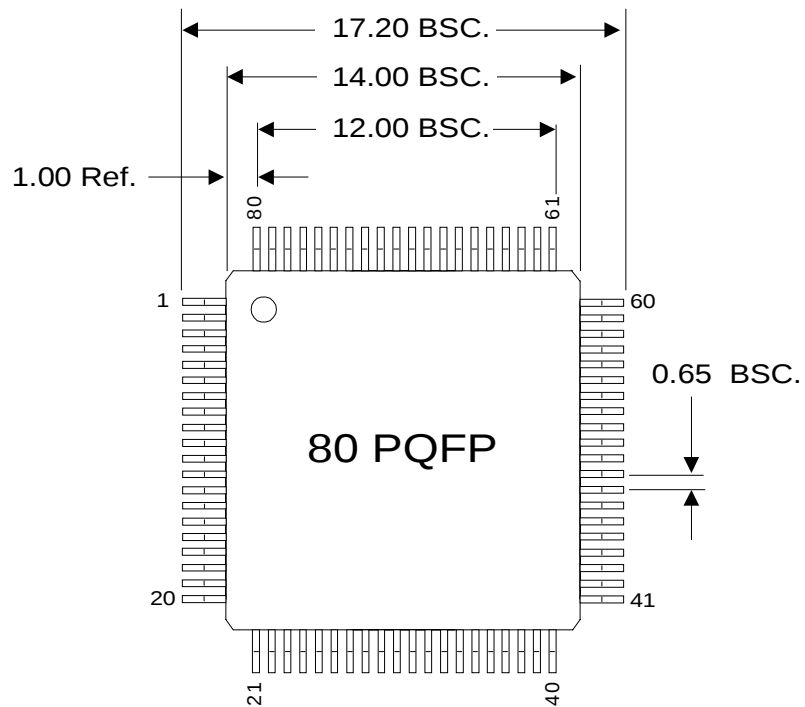
All dimensions are in millimeters (mm).

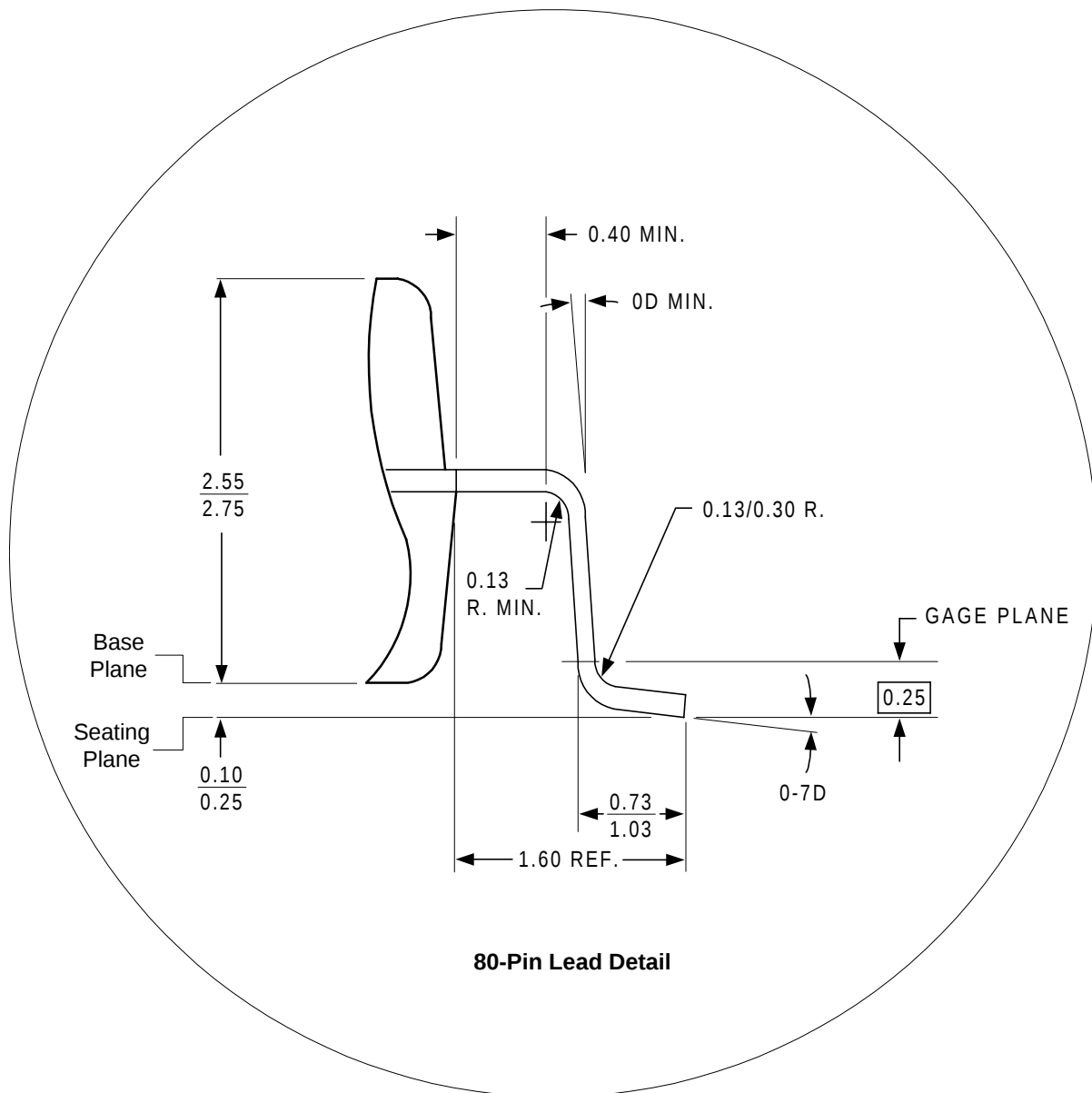
9.1 52 PQFP



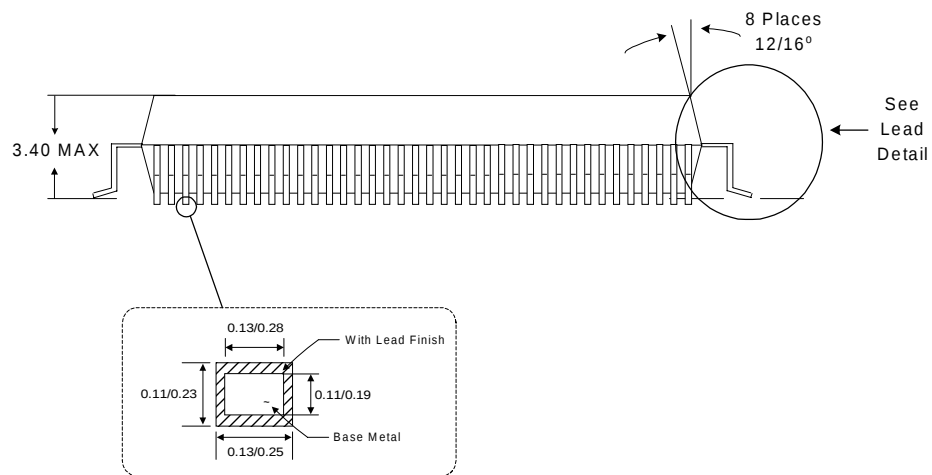
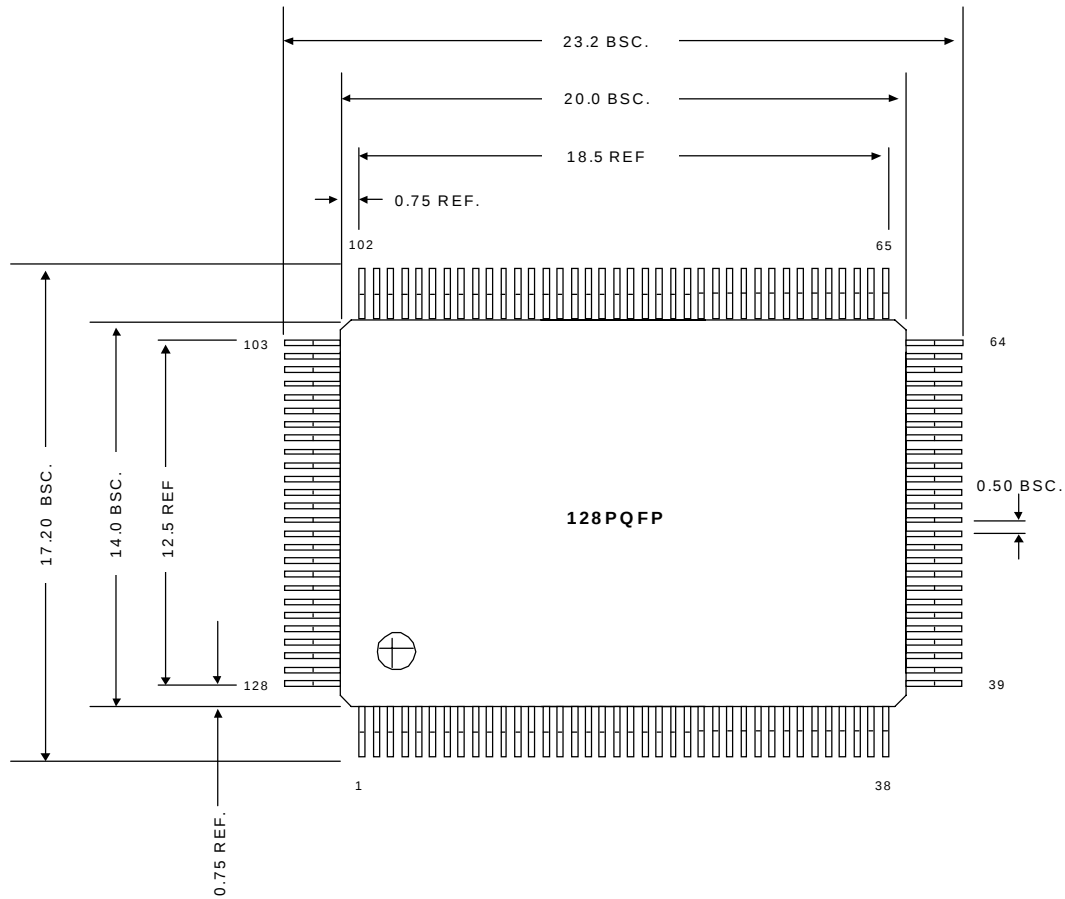


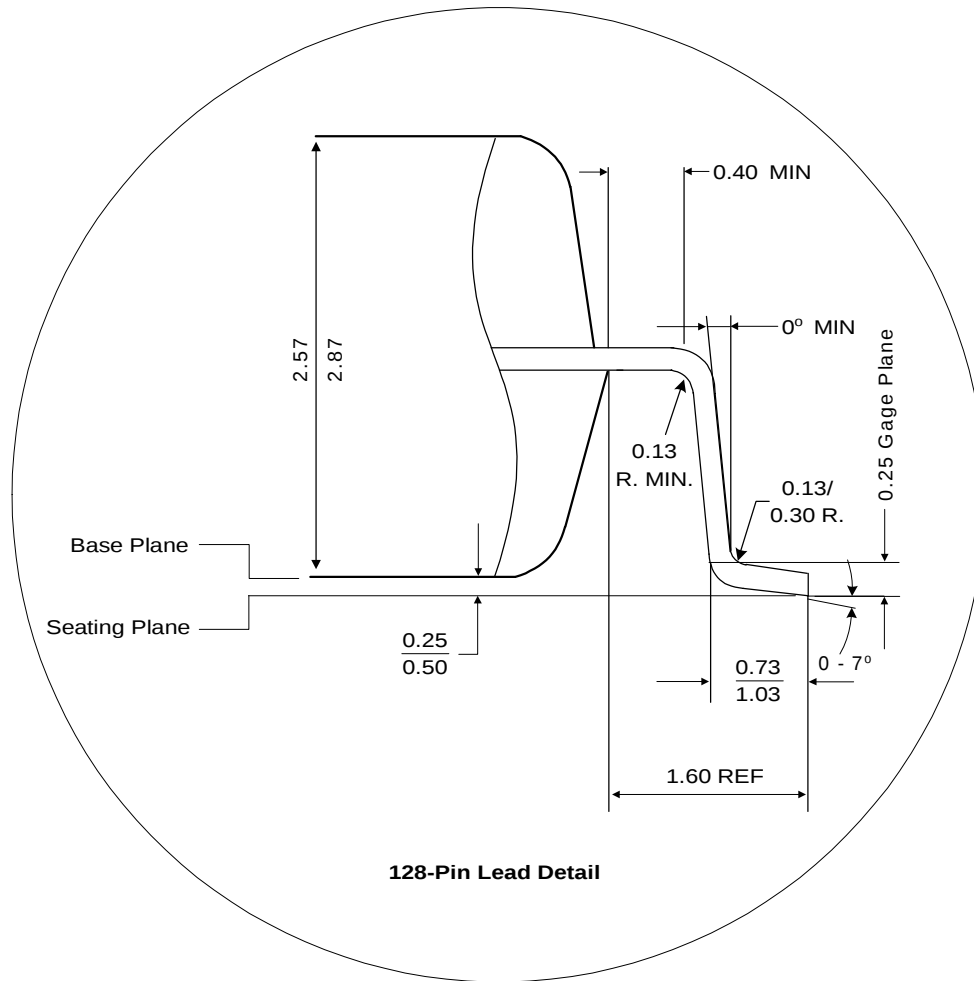
9.2 80 PQFP





9.3 128 PQFP





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