

# DMOS

## 100mA Low-Dropout Regulator

### FEATURES

- **NEW DMOS TOPOLOGY:**  
Ultra Low Dropout Voltage:  
60mV typ at 100mA  
Output capacitor NOT required for stability
- **FAST TRANSIENT RESPONSE**
- **VERY LOW NOISE:** 23 $\mu$ Vrms
- **HIGH ACCURACY:**  $\pm 1.5\%$  max
- **HIGH EFFICIENCY:**  
 $I_{GND} = 500\mu A$  at  $I_{OUT} = 100mA$   
Not Enabled:  $I_{GND} = 10nA$
- **2.5V, 2.8V, 2.85V, 3.0V, 3.3V, 5.0V, AND ADJUSTABLE OUTPUT VERSIONS**
- **OTHER OUTPUT VOLTAGES AVAILABLE UPON REQUEST**
- **FOLDBACK CURRENT LIMIT**
- **THERMAL PROTECTION**
- **SMALL SURFACE-MOUNT PACKAGES:**  
SOT23-5 and SO-8

### APPLICATIONS

- **PORTABLE COMMUNICATION DEVICES**
- **BATTERY-POWERED EQUIPMENT**
- **PERSONAL DIGITAL ASSISTANTS**
- **MODEMS**
- **BAR-CODE SCANNERS**
- **BACKUP POWER SUPPLIES**

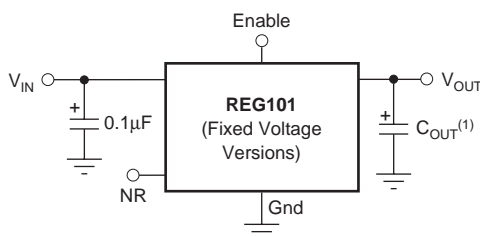
### DESCRIPTION

The REG101 is a family of low-noise, low-dropout linear regulators with low ground pin current. Its new DMOS topology provides significant improvement over previous designs, including low dropout voltage (only 60mV typ at full load), and better transient performance. In addition, no output capacitor is required for stability, unlike conventional low-dropout regulators that are difficult to compensate and require expensive low ESR capacitors greater than 1 $\mu$ F.

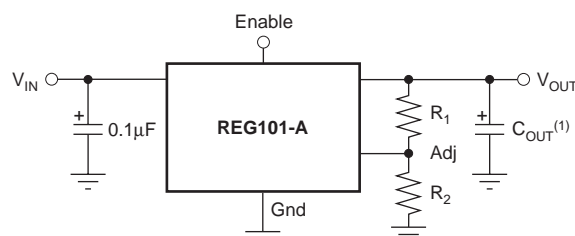
Typical ground pin current is only 500 $\mu$ A (at  $I_{OUT} = 100mA$ ) and drops to 10nA when not in enabled mode. Unlike regulators with PNP pass devices, quiescent current remains relatively constant over load variation and under dropout conditions.

The REG101 has very low output noise (typically 23 $\mu$ Vrms for  $V_{OUT} = 3.3V$  with  $C_{NR} = 0.01\mu F$ ), making it ideal for use in portable communications equipment. Accuracy is maintained over temperature, line, and load variations. Key parameters are tested over the specified temperature range ( $-40^{\circ}C$  to  $+85^{\circ}C$ ).

The REG101 is well protected—internal circuitry provides a current limit that protects the load from damage. Thermal protection circuitry keeps the chip from being damaged by excessive temperature. The REG101 is available in the SOT23-5 and the SO-8 packages.



NR = Noise Reduction



NOTE: (1) Optional.



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## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Supply Input Voltage, $V_{IN}$	–0.3V to 12V
Enable Input Voltage, $V_{EN}$	–0.3V to $V_{IN}$
Feedback Voltage, $V_{FB}$	–0.3V to 6.0V
NR Pin Voltage, $V_{NR}$	–0.3V to 6.0V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range ( $T_J$ )	–55°C to +125°C
Storage Temperature Range ( $T_A$ )	–65°C to +150°C
Lead Temperature (soldering, 3s, SOT23-5, and SO-8)	+240°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION<sup>(1)</sup>

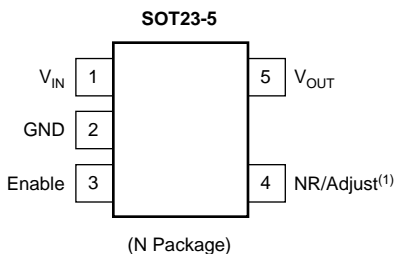
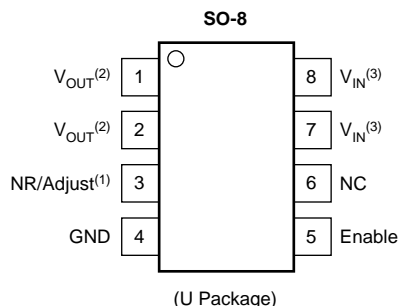
PRODUCT	$V_{OUT}^{(2)}$
REG101xx-yyy/zzz	<p><b>XX</b> is package designator.</p> <p><b>YYYY</b> is typical output voltage (5 = 5.0V, 2.85 = 2.85V, A = Adjustable).</p> <p><b>ZZZ</b> is package quantity.</p>

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

(2) Output voltages from 2.5V to 5.1V in 50mV increments are available; minimum order quantities apply. Contact factory for details and availability.

## PIN CONFIGURATIONS

Top View



NOTE: (1) For REG101A-A: voltage setting resistor pin. All other models: noise reduction capacitor pin.  
 (2) Both pin 1 and pin 2 must be connected.  
 (3) Both pin 7 and pin 8 must be connected.

# ELECTRICAL CHARACTERISTICS

**Boldface** limits apply over the specified temperature range,  $T_J = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

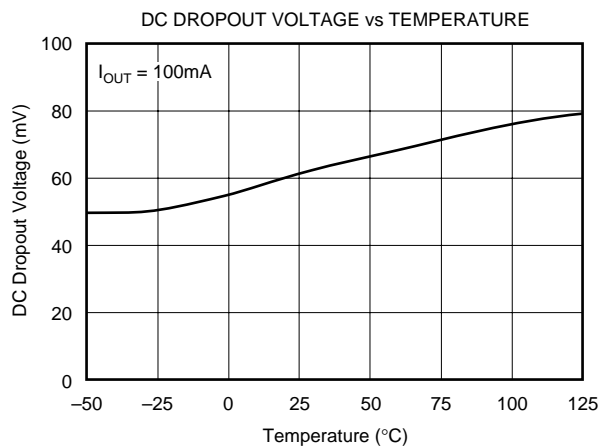
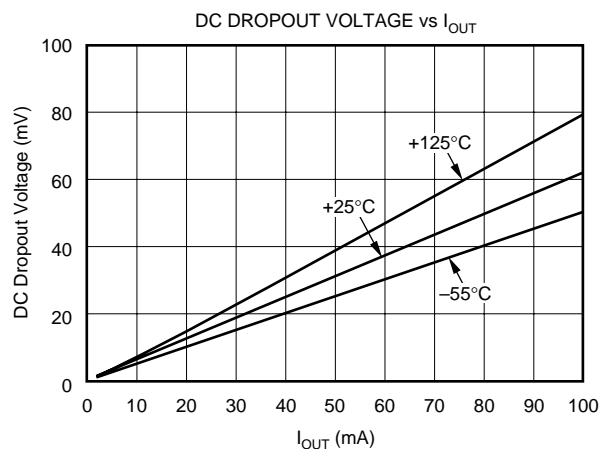
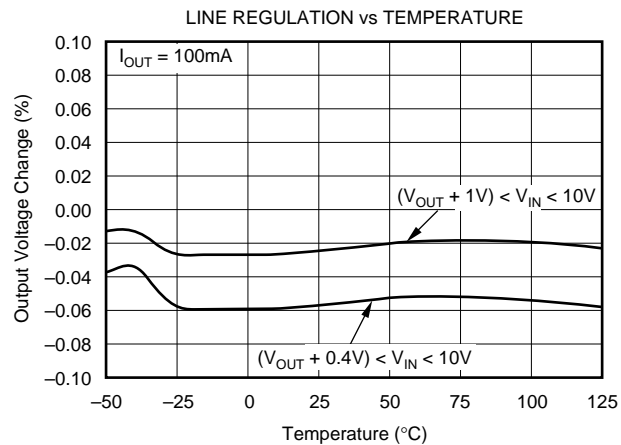
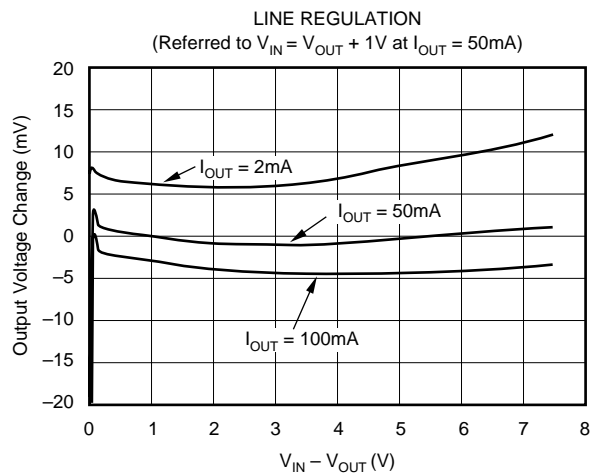
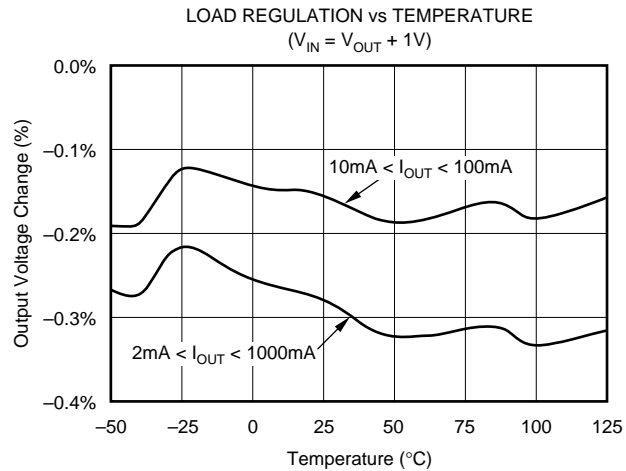
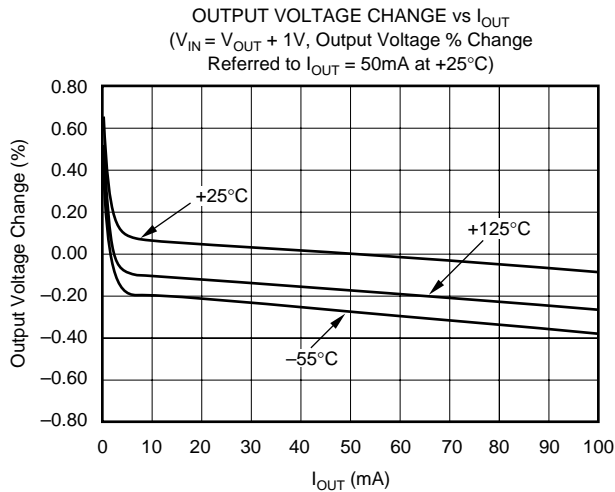
At  $T_J = +25^{\circ}\text{C}$ ,  $V_{IN} = V_{OUT} + 1\text{V}$  ( $V_{OUT} = 2.5\text{V}$  for REG101-A),  $V_{ENABLE} = 1.8\text{V}$ ,  $I_{OUT} = 2\text{mA}$ ,  $C_{NR} = 0.01\mu\text{F}$ , and  $C_{OUT} = 0.1\mu\text{F}^{(1)}$ , unless otherwise noted.

PARAMETER	CONDITION	REG101NA REG101UA			UNITS
		MIN	TYP	MAX	
<b>OUTPUT VOLTAGE</b>					
Output Voltage $V_{OUT}$			2.5		V
REG101-2.5			2.8		V
REG101-2.8			2.85		V
REG101-2.85			3.0		V
REG101-3.0			3.3		V
REG101-3.3			5		V
REG101-5		2.5		5.5	V
REG101-A			1.267		V
Reference Voltage $V_{REF}$			0.2	1	$\mu\text{A}$
Adjust Pin Current $I_{ADJ}$			$\pm 0.5$	$\pm 1.5$	%
Accuracy				<b><math>\pm 2.2</math></b>	%
<b>Over Temperature vs Temperature</b>	$dV_{OUT}/dT$		<b>50</b>		ppm/ $^{\circ}\text{C}$
Includes Line and Load			$\pm 0.8$	$\pm 2.0$	%
<b>Over Temperature</b>				<b><math>\pm 2.7</math></b>	%
<b>DC DROPOUT VOLTAGE<sup>(2)</sup></b>	$V_{DROP}$		4	10	mV
For all models			60	100	mV
<b>Over Temperature</b>				<b>130</b>	mV
<b>VOLTAGE NOISE</b>	$V_n$				
Without $C_{NR}$			$23\mu\text{Vrms/V} \cdot V_{OUT}$		$\mu\text{Vrms}$
With $C_{NR}$ (all fixed voltage models)			$7\mu\text{Vrms/V} \cdot V_{OUT}$		$\mu\text{Vrms}$
<b>OUTPUT CURRENT</b>					
Current Limit <sup>(3)</sup>	$I_{CL}$	130	170	220	mA
<b>Over Temperature</b>		<b>110</b>		<b>240</b>	mA
Short-Circuit Current	$I_{SC}$		60		mA
<b>RIPPLE REJECTION</b>					
$f = 120\text{Hz}$			65		dB
<b>ENABLE CONTROL</b>					
$V_{ENABLE}$ High (output enabled)	$V_{ENABLE}$	1.8		$V_{IN}$	V
$V_{ENABLE}$ Low (output disabled)		-0.2		0.5	V
$I_{ENABLE}$ High (output enabled)	$I_{ENABLE}$		1	100	nA
$I_{ENABLE}$ Low (output disabled)			2	100	nA
Output Disable Time			200		$\mu\text{s}$
Output Enable Time			1.5		ms
<b>THERMAL SHUTDOWN</b>					
Junction Temperature					
Shutdown			160		$^{\circ}\text{C}$
Reset from Shutdown			140		$^{\circ}\text{C}$
<b>GROUND PIN CURRENT</b>					
Ground Pin Current	$I_{GND}$		400	500	$\mu\text{A}$
			500	650	$\mu\text{A}$
Enable Pin Low			0.01	0.2	$\mu\text{A}$
<b>INPUT VOLTAGE</b>	$V_{IN}$				
Operating Input Voltage Range <sup>(5)</sup>		1.8		10	V
Specified Input Voltage Range		$V_{OUT} + 0.4$		10	V
<b>Over Temperature</b>		<b><math>V_{OUT} + 0.6</math></b>		<b>10</b>	V
<b>TEMPERATURE RANGE</b>					
Specified Range	$T_J$	-40		+85	$^{\circ}\text{C}$
Operating Range	$T_J$	-55		+125	$^{\circ}\text{C}$
Storage Range	$T_A$	-65		+150	$^{\circ}\text{C}$
Thermal Resistance					
SOT23-5 Surface Mount	$\theta_{JA}$		200		$^{\circ}\text{C/W}$
SO-8 Surface Mount	$\theta_{JA}$		150		$^{\circ}\text{C/W}$

- NOTES: (1) The REG101 does not require a minimum output capacitor for stability. However, transient response can be improved with proper capacitor selection.  
(2) Dropout voltage is defined as the input voltage minus the output voltage that produces a 2% change in the output voltage from the value at  $V_{IN} = V_{OUT} + 1\text{V}$  at fixed load.  
(3) Current limit is the output current that produces a 10% change in output voltage from  $V_{IN} = V_{OUT} + 1\text{V}$  and  $I_{OUT} = 2\text{mA}$ .  
(4) For  $V_{ENABLE} > 6.5\text{V}$ , see typical characteristic " $I_{ENABLE}$  vs  $V_{ENABLE}$ ".  
(5) The REG101 no longer regulates when  $V_{IN} < V_{OUT} + V_{DROP (MAX)}$ . In drop-out, the impedance from  $V_{IN}$  to  $V_{OUT}$  is typically less than  $1\Omega$  at  $T_J = +25^{\circ}\text{C}$ .

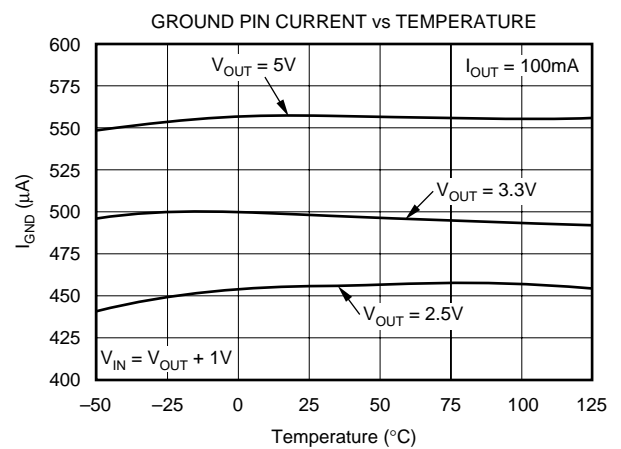
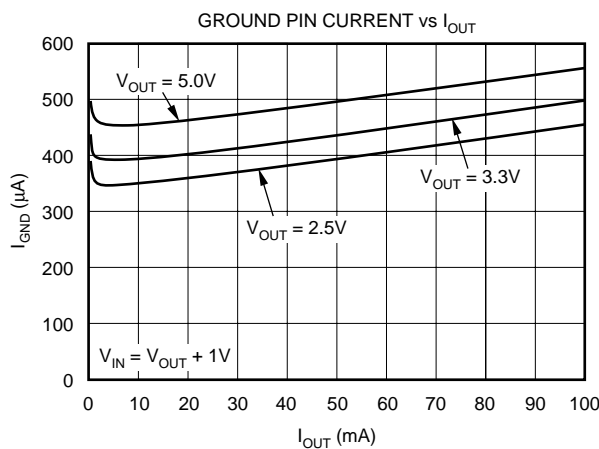
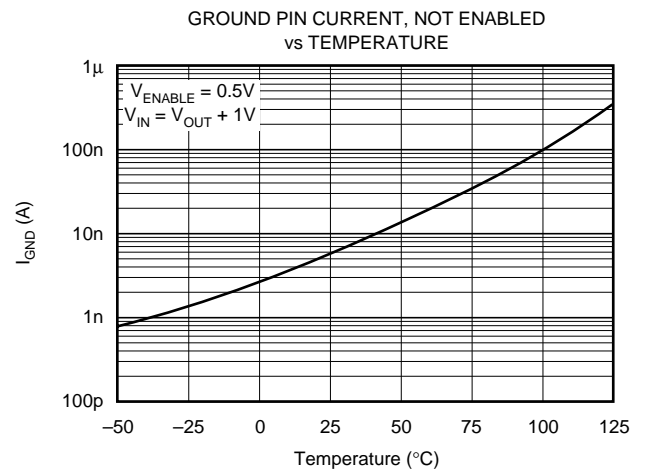
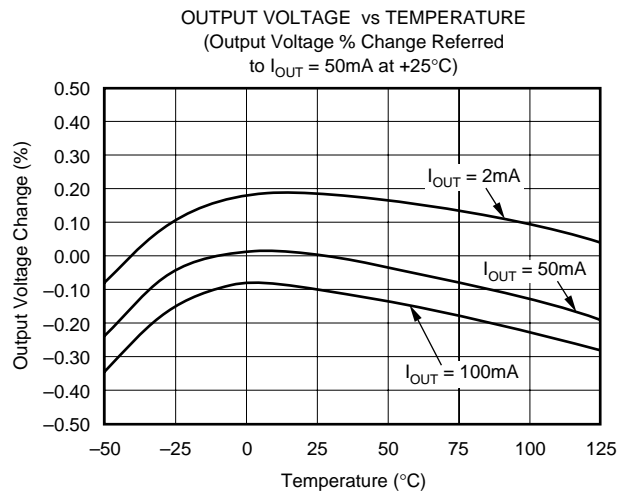
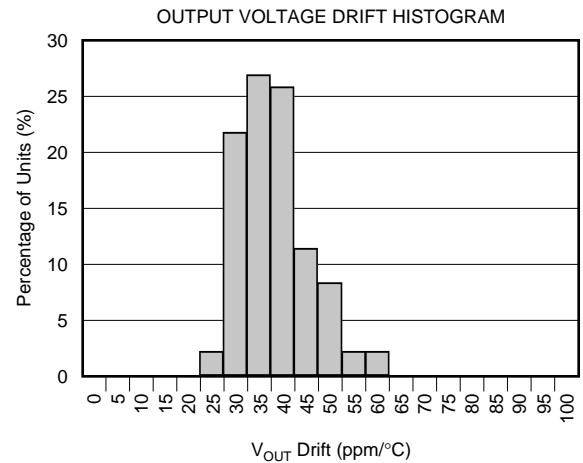
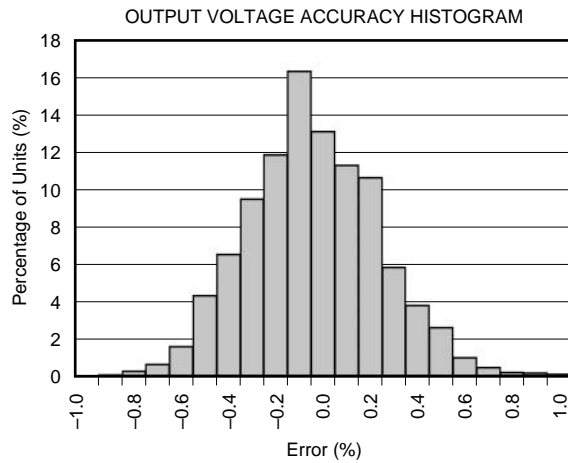
# TYPICAL CHARACTERISTICS

For all models, at  $T_J = +25^\circ\text{C}$  and  $V_{\text{ENABLE}} = 1.8\text{V}$ , unless otherwise noted.



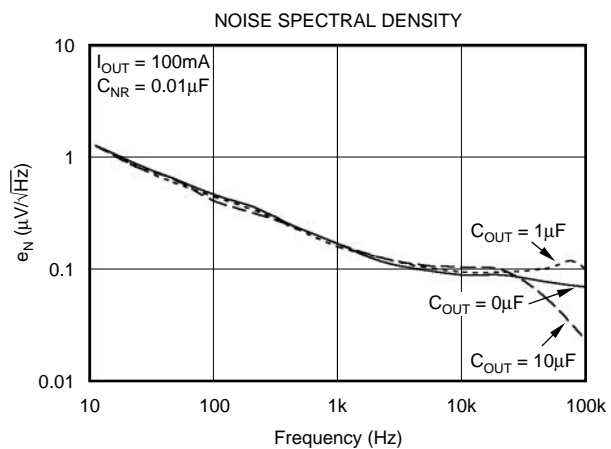
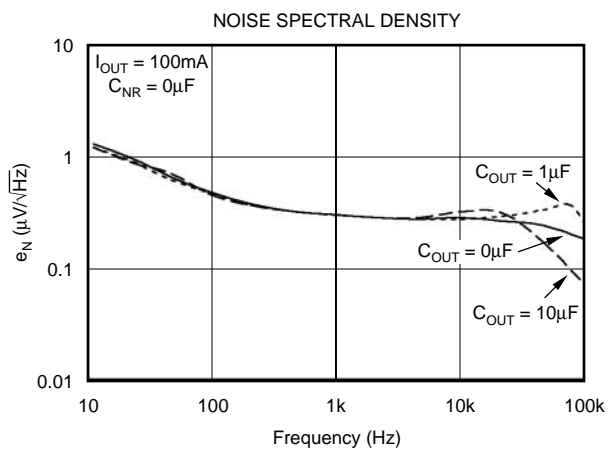
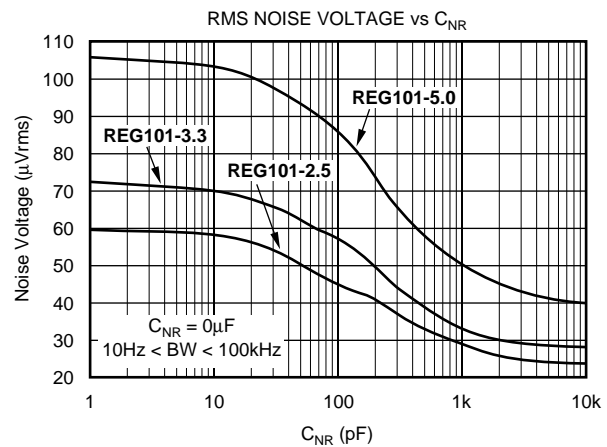
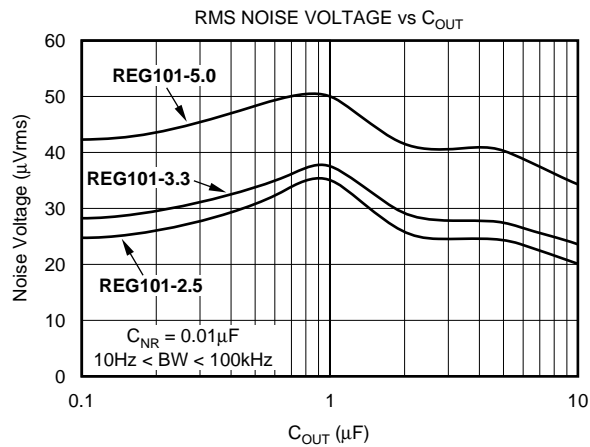
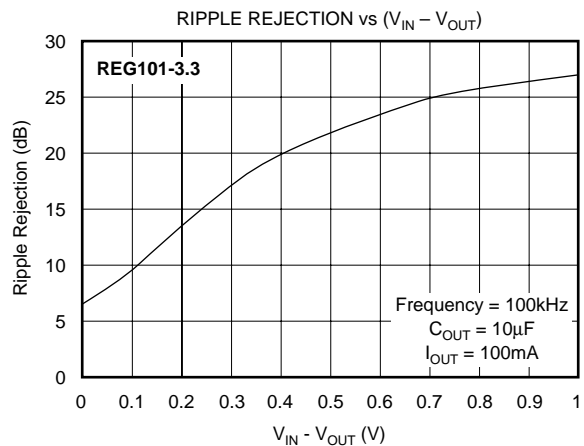
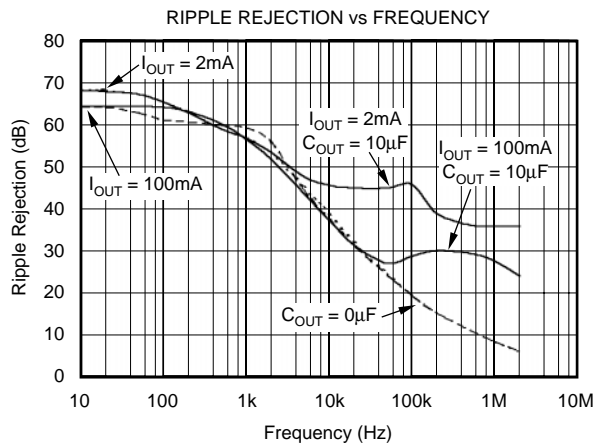
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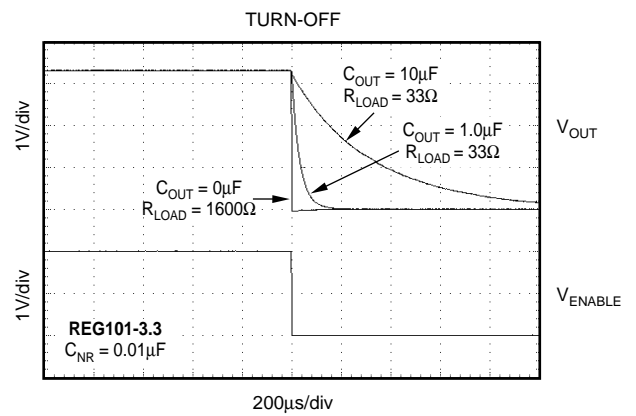
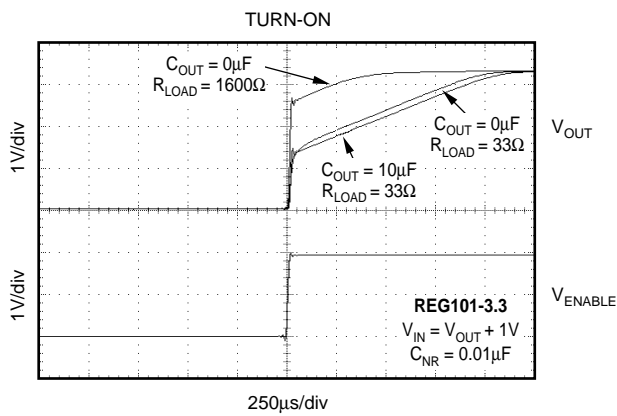
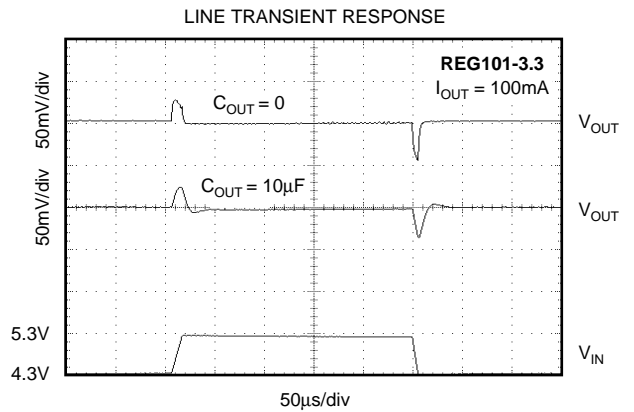
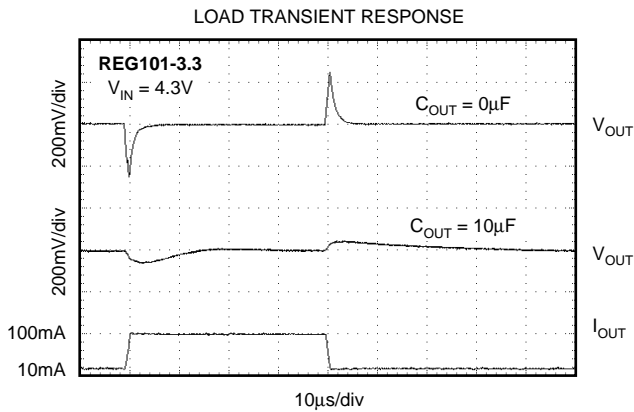
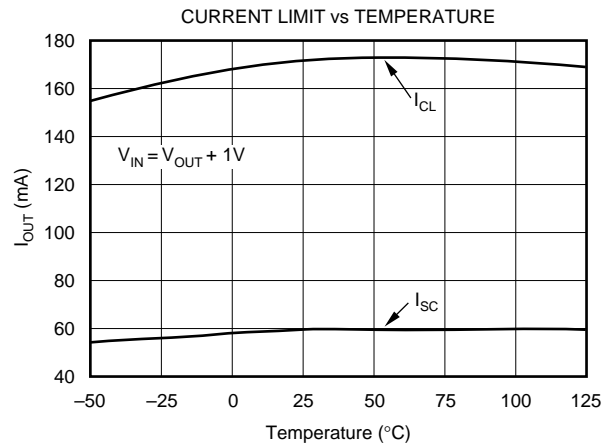
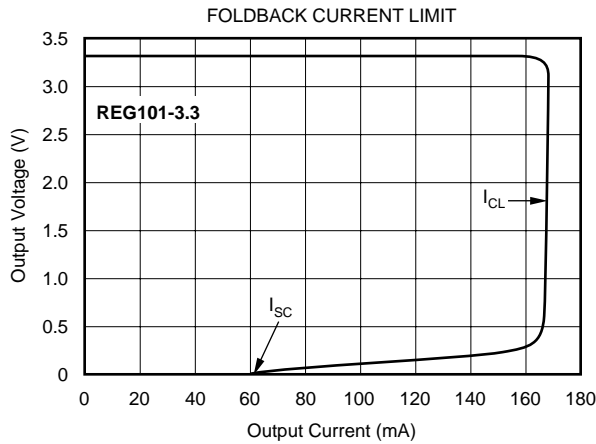
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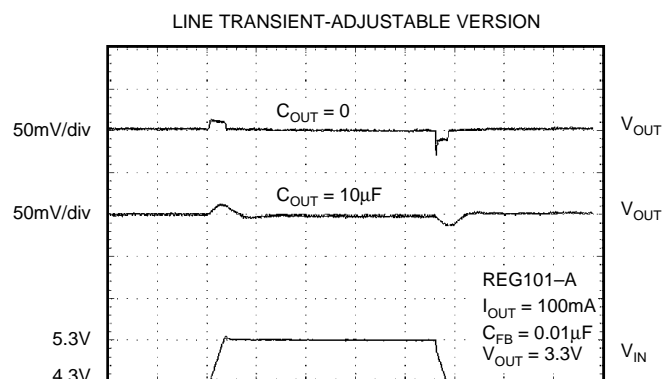
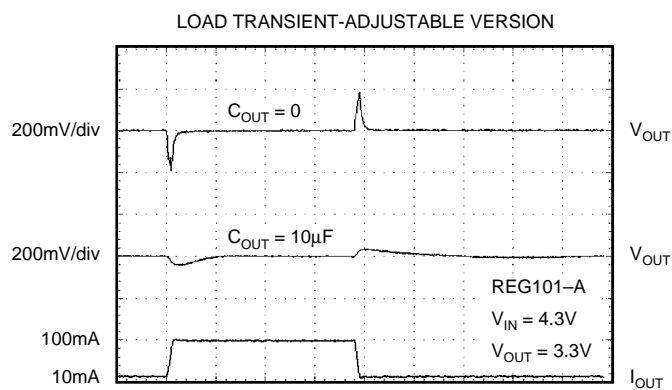
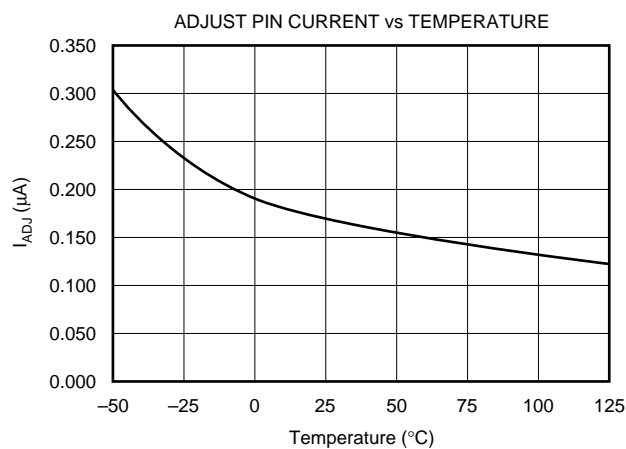
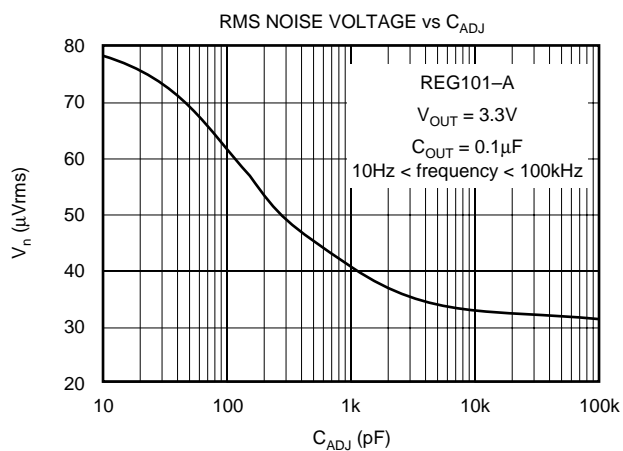
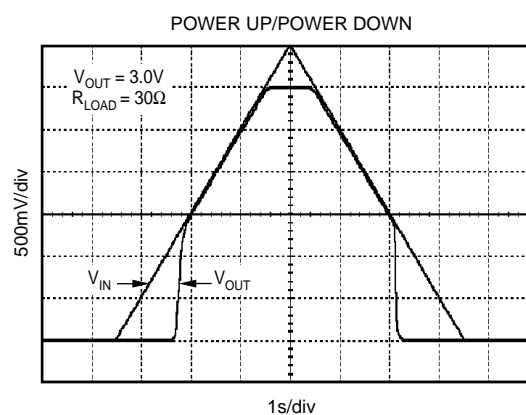
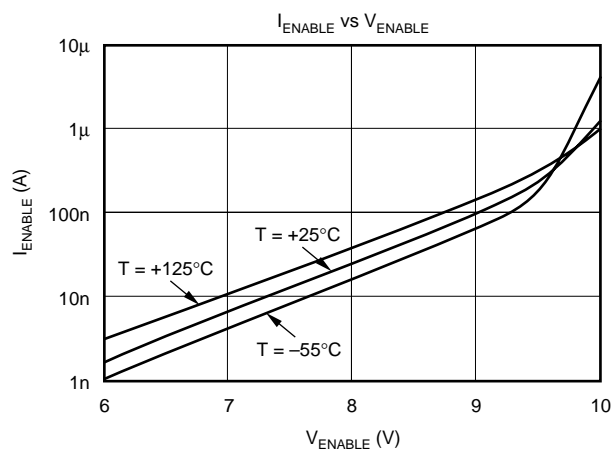
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# TYPICAL CHARACTERISTICS (Cont.)

For all models, at  $T_J = +25^\circ\text{C}$  and  $V_{\text{ENABLE}} = 1.8\text{V}$ , unless otherwise noted.





# BASIC OPERATION

The REG101 series of LDO (Low Drop-Out) linear regulators offers a wide selection of fixed output voltage versions and an adjustable output version. The REG101 belongs to a family of new generation LDO regulators that utilize a DMOS pass transistor to achieve ultra-low dropout performance and freedom from output capacitor constraints. Ground pin current remains under 650μA over all line, load, and temperature conditions. All versions have thermal and over-current protection, including foldback current limit.

The REG101 does not require an output capacitor for regulator stability and is stable over most output currents and with almost any value and type of output capacitor up to 10μF or more. For applications where the regulator output current drops below several milliamps, stability can be enhanced by: adding a 1kΩ to 2kΩ load resistor; using capacitance values less than 10μF; or keeping the effective series resistance greater than 0.05Ω including the capacitor's ESR and parasitic resistance in printed circuit board traces, solder joints, and sockets.

Although an input capacitor is not required, it is good analog design practice to connect a 0.1μF low ESR capacitor across

the input supply voltage. This is recommended to improve ripple rejection by reducing input voltage ripple.

Figure 1 shows the basic circuit connections for the fixed voltage models. Figure 2 gives the connections for the adjustable output version (REG101A) and example resistor values for some commonly used output voltages. Values for other voltages can be calculated from the equation shown in Figure 2.

## INTERNAL CURRENT LIMIT

The REG101 internal current limit has a typical value of 170mA. A foldback feature limits the short-circuit current to a typical short-circuit value of 60mA. This helps to protect the regulator from damage under all load conditions. A characteristic of  $V_{OUT}$  versus  $I_{OUT}$  is given in Figure 3 and in the Typical Characteristics section.

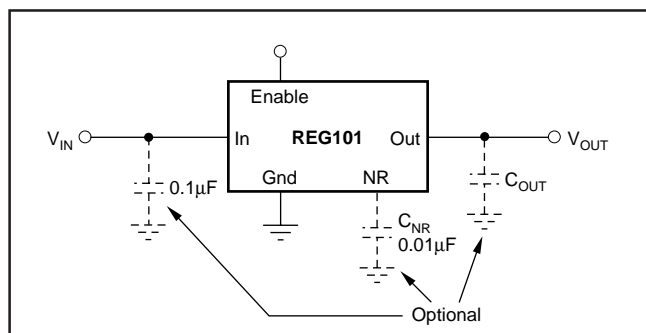


FIGURE 1. Fixed Voltage Nominal Circuit for REG101.

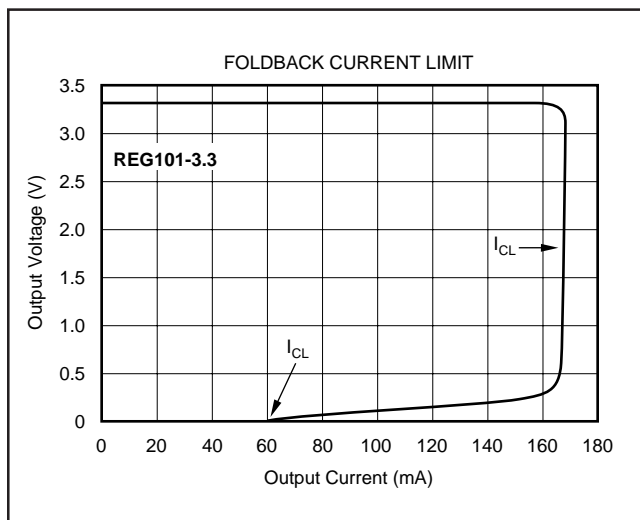


FIGURE 3. Foldback Current Limit of the REG101-3.3 at 25°C.

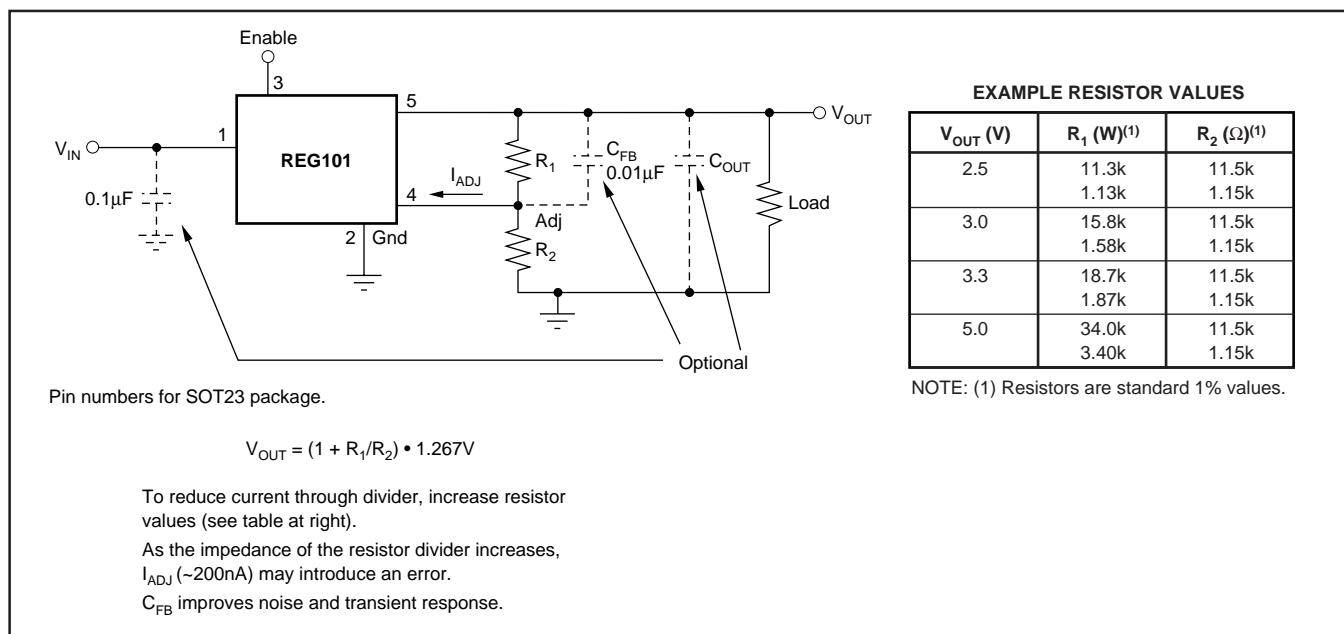


FIGURE 2. Adjustable Voltage Circuit for REG101A.

## ENABLE

The Enable pin is active HIGH and compatible with standard TTL-CMOS levels. Inputs below 0.5V (max) turn the regulator off and all circuitry is disabled. Under this condition, ground pin current drops to approximately 10nA. When a pull-up resistor is used, and operation down to  $V_{IN} = 1.8V$  is required, use values  $< 50k\Omega$ .

## OUTPUT NOISE

A precision band-gap reference is used for the internal reference voltage,  $V_{REF}$ . This reference is the dominant noise source within the REG101 and it generates approximately 29 $\mu V_{rms}$  in the 10Hz to 100kHz bandwidth at the reference output. The regulator control loop gains up the reference noise, so that the noise voltage of the regulator is approximately given by:

$$V_N = 29\mu V_{rms} \frac{R_1 + R_2}{R_2} = 29\mu V_{rms} \cdot \frac{V_{OUT}}{V_{REF}}$$

Since the value of  $V_{REF}$  is 1.267V, this relationship reduces to:

$$V_N = 23 \frac{\mu V_{rms}}{V} \cdot V_{OUT}$$

Connecting a capacitor,  $C_{NR}$ , from the Noise Reduction (NR) pin to ground, as shown in Figure 4, forms a low-pass filter for the voltage reference. For  $C_{NR} = 10nF$ , the total noise in the 10Hz to 100kHz bandwidth is reduced by approximately a factor of 2.8 for  $V_O = 3.3V$ . This noise reduction effect is shown in Figure 5 and as “RMS Noise Voltage vs  $C_{NR}$ ” in the Typical Characteristics section.

Noise can be further reduced by carefully choosing an output capacitor,  $C_{OUT}$ . Best overall noise performance is

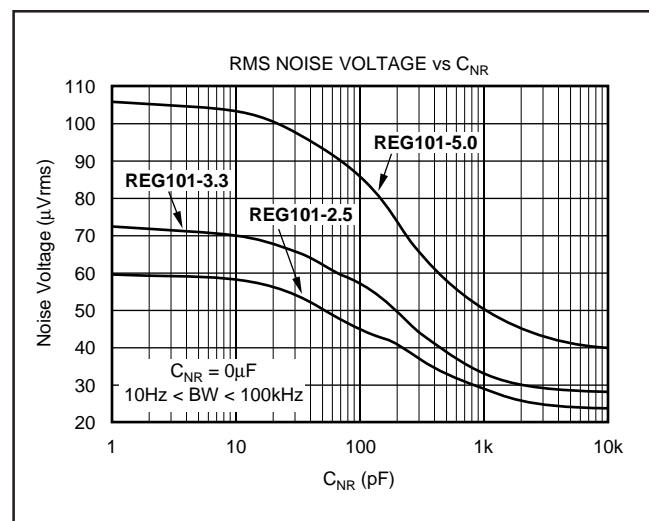


FIGURE 5. Output Noise versus Noise Reduction Capacitor.

achieved with very low ( $< 0.22\mu F$ ) or very high ( $> 2.2\mu F$ ) values of  $C_{OUT}$ . See “RMS Noise Voltage vs  $C_{OUT}$ ” in the Typical Characteristics section.

The REG101 utilizes an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the DMOS pass element above  $V_{IN}$ . The charge-pump switching noise (nominal switching frequency = 2MHz) is not measurable at the output of the regulator over most values of  $C_{OUT}$  and  $I_{OUT}$ .

The REG101 adjustable version does not have the noise-reduction pin available, however, the adjust pin is the summing junction of the error amplifier. A capacitor,  $C_{FB}$ , connected from the output to the adjust pin will reduce both the output noise and the peak error from a load transient. See the typical characteristics for output noise performance.

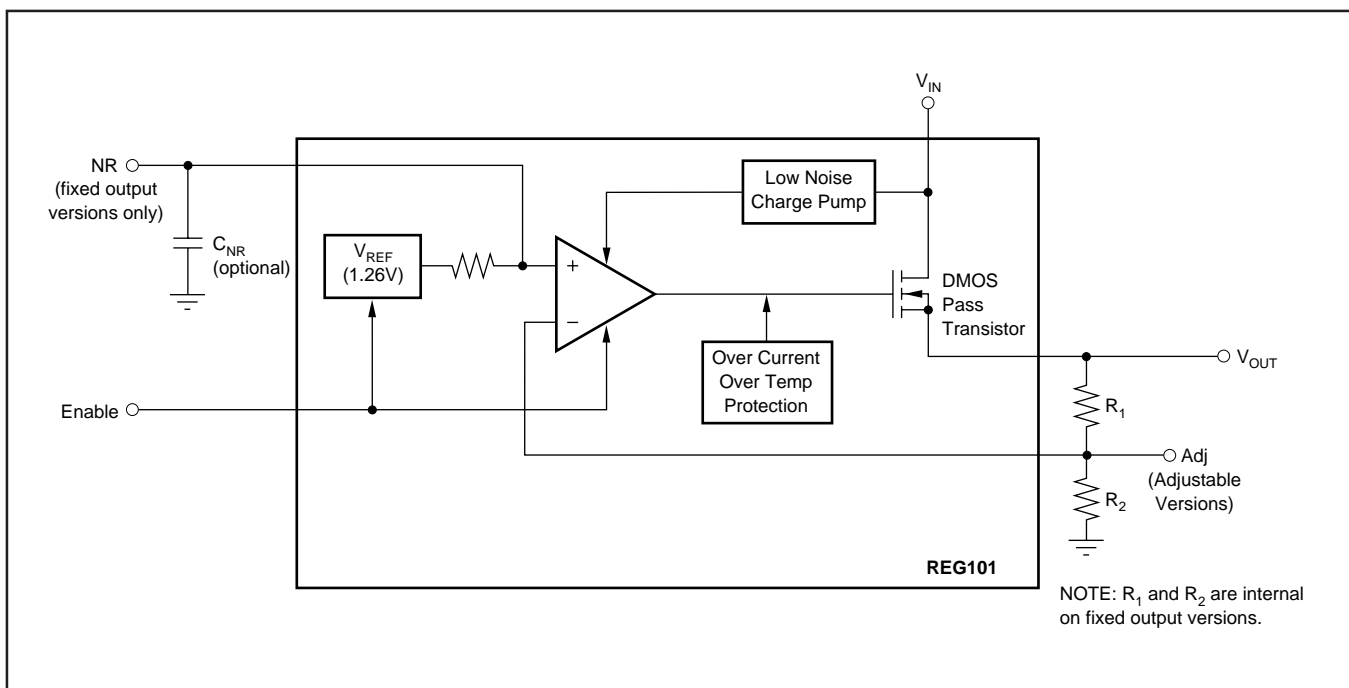


FIGURE 4. Block Diagram.

## DROP-OUT VOLTAGE

The REG101 uses an N-channel DMOS as the “pass” element. When the input voltage is within a few tens of millivolts of the output voltage, the DMOS device behaves like a resistor. Therefore, for low values of  $V_{IN}$  to  $V_{OUT}$ , the regulator’s input-to-output resistance is the  $R_{DS(ON)}$  of the DMOS pass element (typically 600m $\Omega$ ). For static (DC) loads, the REG101 will typically maintain regulation down to  $V_{IN}$  to  $V_{OUT}$  voltage drop of 60mV at full rated output current. In Figure 6, the bottom line (DC dropout) shows the minimum  $V_{IN}$  to  $V_{OUT}$  voltage drop required to prevent drop-out under DC load conditions.

For large step changes in load current, the REG101 requires a larger voltage drop across it to avoid degraded transient response. The boundary of this “transient drop-out” region is shown as the top line in Figure 6. Values of  $V_{IN}$  to  $V_{OUT}$  voltage drop above this line insure normal transient response.

In the transient dropout region between “DC” and “Transient”, transient response recovery time increases. The time required to recover from a load transient is a function of both the magnitude and rate of the step change in load current and the available “headroom”  $V_{IN}$  to  $V_{OUT}$  voltage drop. Under worst-case conditions (full-scale load change with  $V_{IN}$  to  $V_{OUT}$  voltage drop close to DC dropout levels), the REG101 can take several hundred microseconds to re-enter the specified window of regulation.

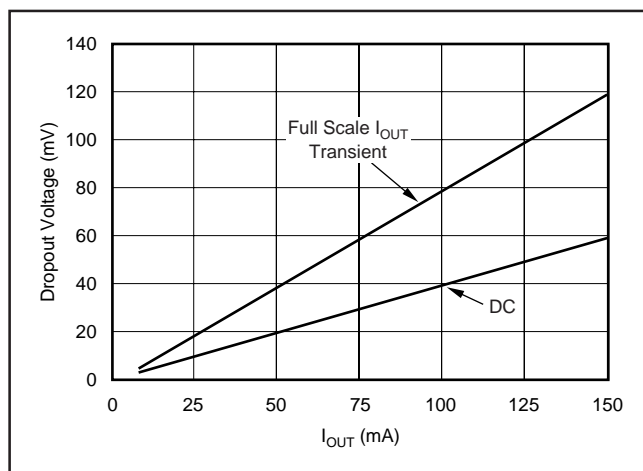


FIGURE 6. Transient and DC Dropout.

## TRANSIENT RESPONSE

The REG101 response to transient line and load conditions improves at lower output voltages. The addition of a capacitor (nominal value 0.47 $\mu$ F) from the output pin to ground may improve the transient response. In the adjustable version, the addition of a capacitor,  $C_{FB}$  (nominal value 10nF), from the output to the adjust pin will also improve the transient response.

## THERMAL PROTECTION

The REG101 has thermal shutdown circuitry that protects the regulator from damage. The thermal protection circuitry disables the output when the junction temperature reaches approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on various conditions, the thermal protection circuit may cycle on and off. This limits the dissipation of the regulator, but may have an undesirable effect on the load.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to 125°C, maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered. Use worst-case loads and signal conditions. For good reliability, thermal protection should trigger more than 35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the REG101 has been designed to protect against overload conditions. It was not intended to replace proper heat sinking. Continuously running the REG101 into thermal shutdown will degrade reliability.

## POWER DISSIPATION

The REG101 is available in two different package configurations. The ability to remove heat from the die is different for each package type and, therefore, presents different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. While it is difficult to impossible to quantify all of the variables in a thermal design of this type, performance data for several configurations are shown in Figure 7.

Power dissipation depends on input voltage, load condition, and duty cycle. Power dissipation is equal to the product of the average output current times the voltage across the output element,  $V_{IN}$  to  $V_{OUT}$  voltage drop.

$$P_D = (V_{IN} - V_{OUT}) \cdot I_{OUT(AVG)}$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage.

## REGULATOR MOUNTING

Solder pad footprint recommendations for the various REG101 devices are presented in the Application Bulletin AB-132, "Solder Pad Recommendations for Surface-Mount Devices" (SBFA015), available from the Texas Instruments web site ([www.ti.com](http://www.ti.com)).

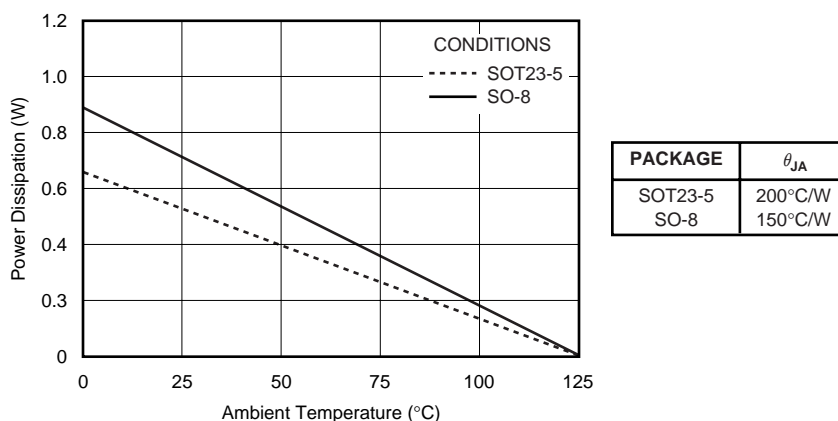


FIGURE 7. Maximum Power Dissipation versus Ambient Temperature for the Various Packages.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REG101NA-2.5/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1G	<a href="#">Samples</a>
REG101NA-2.5/250G4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1G	<a href="#">Samples</a>
REG101NA-2.5/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1G	<a href="#">Samples</a>
REG101NA-2.8/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1E	<a href="#">Samples</a>
REG101NA-2.85/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1N	<a href="#">Samples</a>
REG101NA-2.85/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1N	<a href="#">Samples</a>
REG101NA-3.3/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1C	<a href="#">Samples</a>
REG101NA-3.3/250G4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1C	<a href="#">Samples</a>
REG101NA-3.3/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1C	<a href="#">Samples</a>
REG101NA-3.3/3KG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1C	<a href="#">Samples</a>
REG101NA-3/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R01D	<a href="#">Samples</a>
REG101NA-3/250G4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R01D	<a href="#">Samples</a>
REG101NA-3/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R01D	<a href="#">Samples</a>
REG101NA-3/3KG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	R01D	<a href="#">Samples</a>
REG101NA-5/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1B	<a href="#">Samples</a>
REG101NA-5/250G4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1B	<a href="#">Samples</a>
REG101NA-5/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1B	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REG101NA-5/3KG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1B	<a href="#">Samples</a>
REG101NA-A/250	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1A	<a href="#">Samples</a>
REG101NA-A/250G4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1A	<a href="#">Samples</a>
REG101NA-A/3K	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1A	<a href="#">Samples</a>
REG101NA-A/3KG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RO1A	<a href="#">Samples</a>
REG101UA-2.5	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 101U25	<a href="#">Samples</a>
REG101UA-2.5G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 101U25	<a href="#">Samples</a>
REG101UA-2.85	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 101285	<a href="#">Samples</a>
REG101UA-3	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 101U30	<a href="#">Samples</a>
REG101UA-3.3	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 101U33	<a href="#">Samples</a>
REG101UA-3.3/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 101U33	<a href="#">Samples</a>
REG101UA-3.3G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 101U33	<a href="#">Samples</a>
REG101UA-3G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 101U30	<a href="#">Samples</a>
REG101UA-5	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 101U50	<a href="#">Samples</a>
REG101UA-5/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 101U50	<a href="#">Samples</a>
REG101UA-5/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 101U50	<a href="#">Samples</a>
REG101UA-5G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 101U50	<a href="#">Samples</a>
REG101UA-A	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 101UA	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REG101UA-AG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	REG 101UA	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REG101NA-2.5/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG101NA-2.5/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG101NA-2.8/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG101NA-2.85/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG101NA-2.85/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG101NA-3.3/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG101NA-3.3/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG101NA-3/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG101NA-3/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG101NA-5/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG101NA-5/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG101NA-A/250	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG101NA-A/3K	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REG101UA-3.3/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REG101UA-5/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

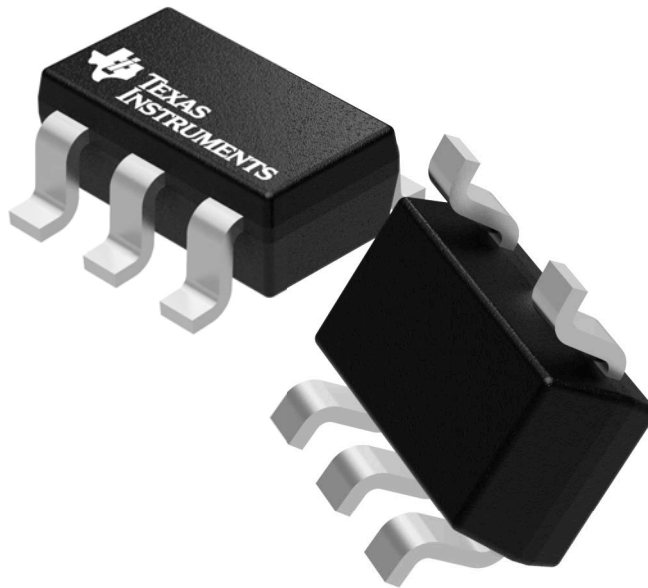
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REG101NA-2.5/250	SOT-23	DBV	5	250	203.0	203.0	35.0
REG101NA-2.5/3K	SOT-23	DBV	5	3000	203.0	203.0	35.0
REG101NA-2.8/250	SOT-23	DBV	5	250	203.0	203.0	35.0
REG101NA-2.85/250	SOT-23	DBV	5	250	203.0	203.0	35.0
REG101NA-2.85/3K	SOT-23	DBV	5	3000	203.0	203.0	35.0
REG101NA-3.3/250	SOT-23	DBV	5	250	203.0	203.0	35.0
REG101NA-3.3/3K	SOT-23	DBV	5	3000	203.0	203.0	35.0
REG101NA-3/250	SOT-23	DBV	5	250	203.0	203.0	35.0
REG101NA-3/3K	SOT-23	DBV	5	3000	203.0	203.0	35.0
REG101NA-5/250	SOT-23	DBV	5	250	203.0	203.0	35.0
REG101NA-5/3K	SOT-23	DBV	5	3000	203.0	203.0	35.0
REG101NA-A/250	SOT-23	DBV	5	250	203.0	203.0	35.0
REG101NA-A/3K	SOT-23	DBV	5	3000	203.0	203.0	35.0
REG101UA-3.3/2K5	SOIC	D	8	2500	367.0	367.0	35.0
REG101UA-5/2K5	SOIC	D	8	2500	367.0	367.0	35.0

## GENERIC PACKAGE VIEW

**DBV 5**

**SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4073253/P

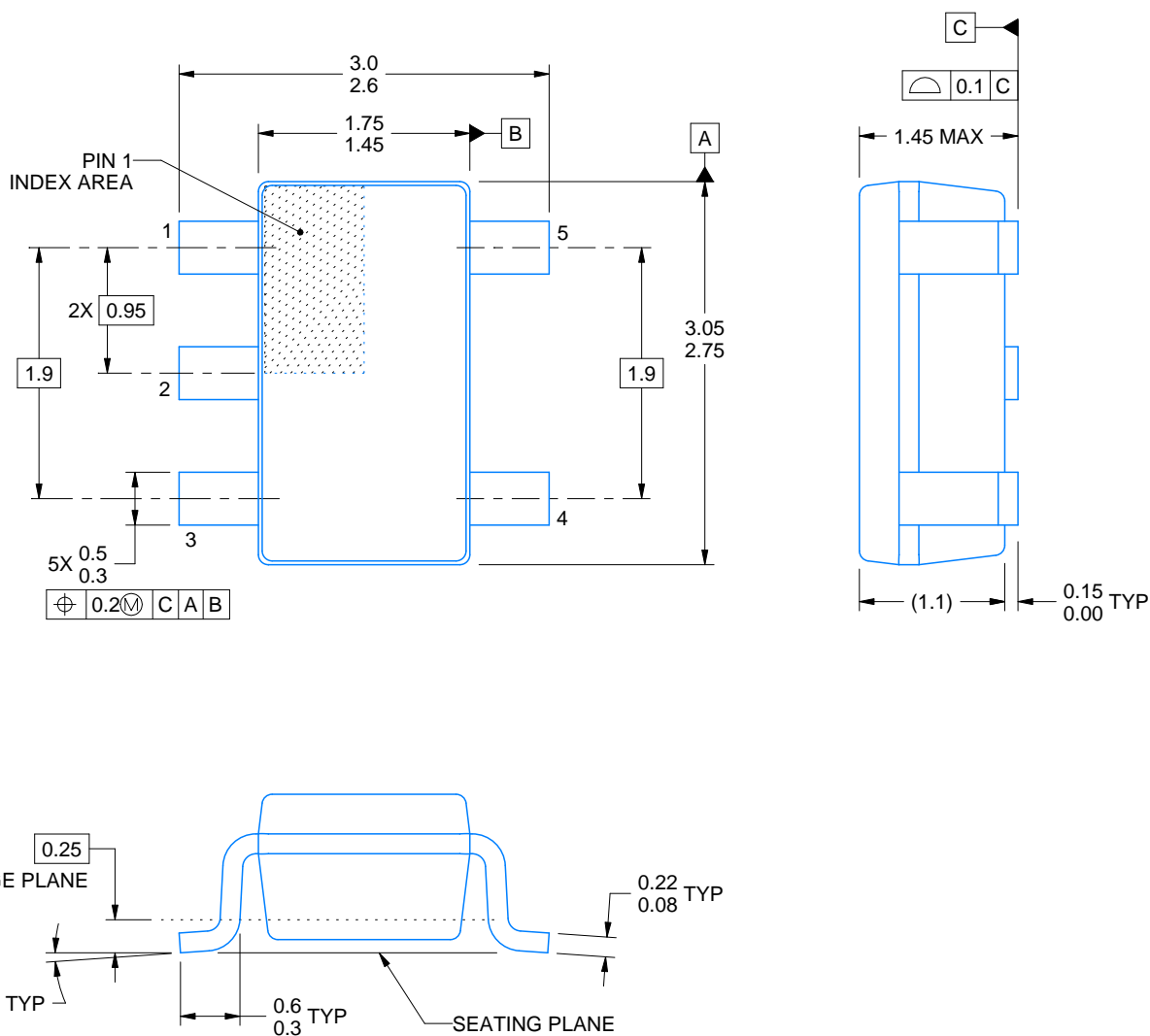


**DBV0005A**

# PACKAGE OUTLINE

**SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



4214839/C 04/2017

## NOTES:

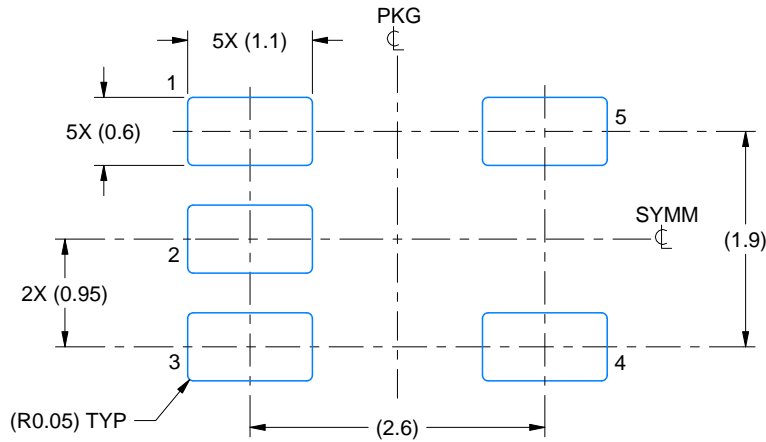
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.

# EXAMPLE BOARD LAYOUT

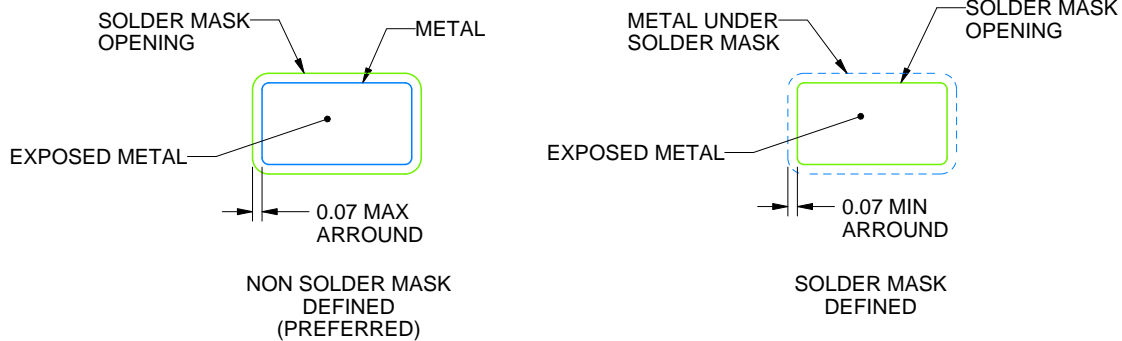
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

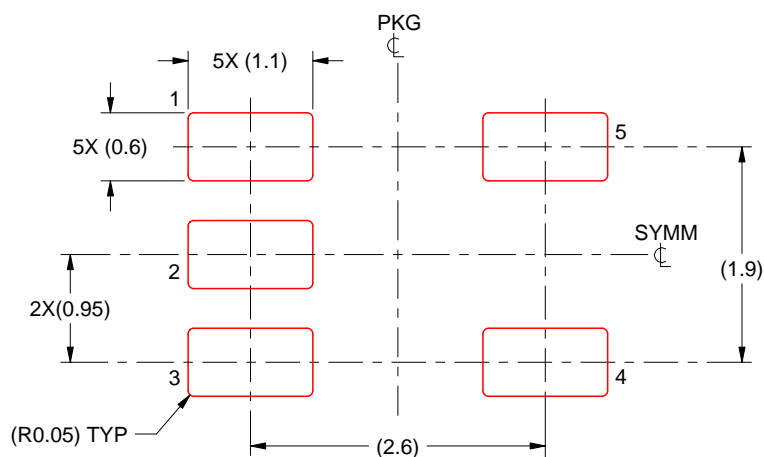
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



## NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.