PI2EQXDP101-A

1 to 1 DisplayPort™ ReDriver™

Features

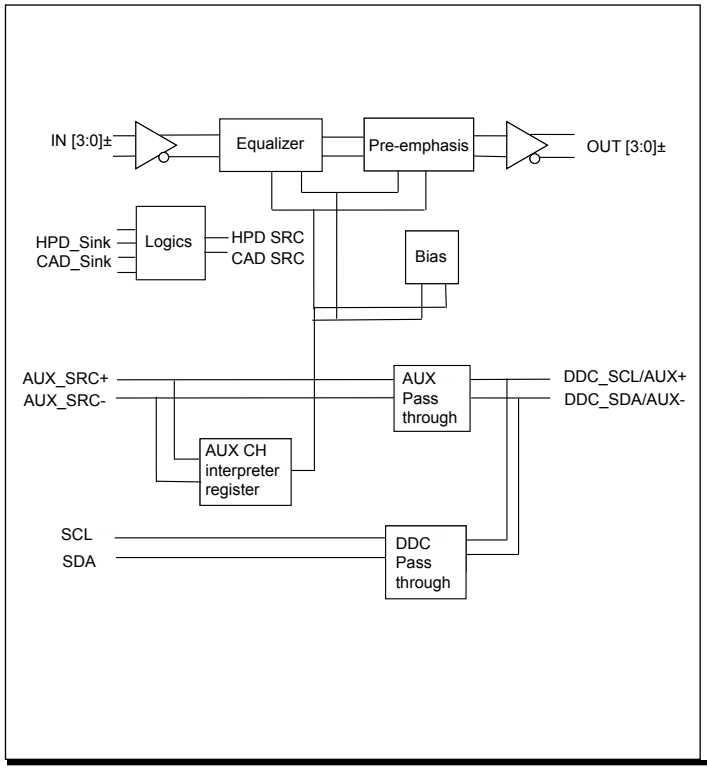
- DisplayPort™ 1.1a operation at reduced bit rate (1.62Gbps) and high bit rate (2.7Gbps)
- Jitter elimination circuits automatically adjust link via training path
  - Pre-Emphasis, and output swing
- Can support all 4 levels of output swing and 4 levels output pre-emphasis, as specified in the DisplayPort 1.1a spec.
- AUX interception circuit only listens to the link training, but does not affect link training
- Low insertion loss across the AUX signal path (0.35dB @1Mbps)
- Output can support dual mode DP by providing DDC signals across the AUX_sink pins
  - Using Cable Detect pin from DP connector (pin 13), the switch can toggle between DP and TMDS mode.
- Automatic power down state when HPD signal is LOW
- Enters low power mode when no data signal is present
- Dual power supply (1.5V and 3.3V)
- 2KV HBM ESD protection
- 50 ohm output termination can be turned off when port is off
  - Port is turned off automatically when not needed
- Package (Pb-Free & Green available)
  - 36-pin TQFN (ZF)

Description

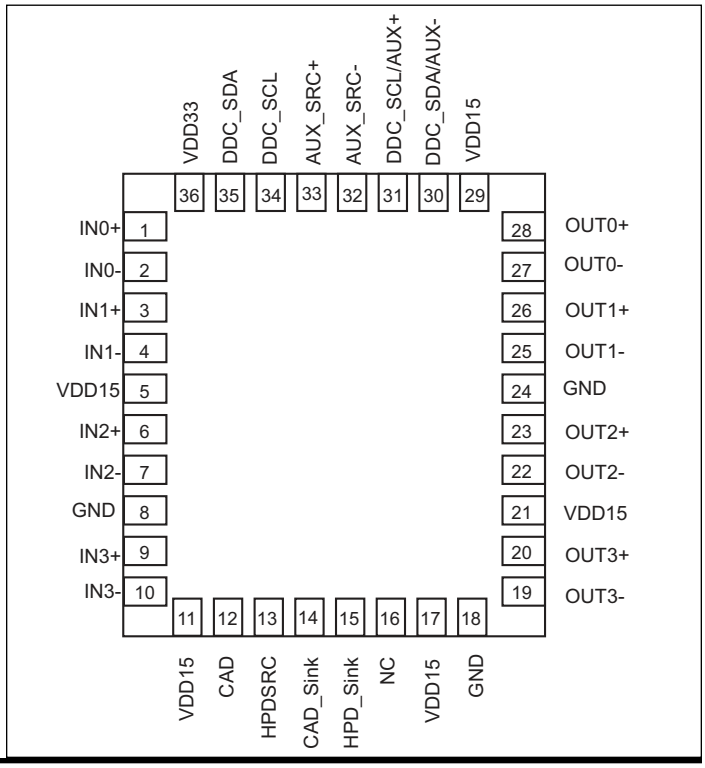
The PI2EQXDP101-A is a one Input and one Output DisplayPort™ ReDriver™ that support a maximum data rate of 2.7 Gbps through each channel, which results in a total of 10.8Gbps through-put.

Output Level Swing and Output Pre-emphasis and number of active lanes are controlled by decoding the AUX command during link initialization. Also, utilizing the HPD signals from each DisplayPort port, the PI2EQXDP101-A can automatically enter power down state. Or, if the graphics driver is off and has no output signal, Pericom's PI2EQXDP101-A can automatically enter low power mode, even if an active monitor is attached.

Block Diagram



Pin Diagram (Top-side View)



Pin Description

Pin #	Name	I/O	Description
33	AUX_SRC+	I/O	Aux positive channel on source side
32	AUX_SRC-	I/O	Aux negative channel on source side
12	CAD	Output	Cable Detect to source
14	CAD_Sink	Input	Cable Detect from DP connector, with 200K-Ohm pull-down.
34	DDC_SCL	I/O	I^2C SCL clock on source side
31	DDC_SCL/AUX+	I/O	Aux channel positive when configured as DP mode, I^2C SCL clock when configured as TMDS mode
35	DDC_SDA	I/O	I^2C SDA data on source side
30	DDC_SDA/AUX-	I/O	Aux channel negative when configured as DP mode, I^2C SDA data when configured as TMDS mode
8, 18, 24, Center Pad	GND	Power	Ground
15	HPD_Sink	Input	Hot Plug detect from sink side, with 200K-Ohm pull-down.
13	HPDSRC	Output	Hot Plug detect to source
1	IN0+	Input	Lane 0 data input, differential pair
2	IN0-		
3	IN1+	Input	Lane 1 data input, differential pair
4	IN1-		
6	IN2+	Input	Lane 2 data input, differential pair
7	IN2-		
9	IN3+	Input	Lane 3 data input, differential pair
10	IN3-		
16	NC	-	No Connect
28	OUT0+	Output	Lane 0 data output, differential pair
27	OUT0-		
26	OUT1+	Output	Lane 1 data output, differential pair
25	OUT1-		
23	OUT2+	Output	Lane 2 data output, differential pair
22	OUT2-		
20	OUT3+	Output	Lane 3 data output, differential pair
19	OUT3-		
5, 11, 17, 21, 29	VDD15	Power	Power Supply, 1.5V ± 5%
36	VDD33	Power	Power Supply, 3.3V ± 5%

AUX listener Register Assignment

AUX command are stored interpreted and stored in the registers, ReDriver will then be re-configured by default. Registers do not have a power-on default state.

Address	Name	Description	Access
00100h	Link initialization field AUX	LINK_BW_SET: Main Link Bandwidth Setting = Value x 0.27 Gbps per lane Bits 7:0 = LINK_BW_SET For DisplayPort version 1, revision 1a, only two values are supported. All other values are reserved. 06h = 1.62 Gbps per lane 0Ah = 2.7 Gbps per lane Source may choose either of the two link bandwidth as long as it does not exceed the capability of DisplayPort receiver as indicated in the receiver capability field.	R/W
00101h	Link initialization field	LANE_COUNT_SET Bits3:0 = LANE_COUNT_SET 1h = One lane 2h = Two lanes 4h = Four lanes For one-lane configuration, Lane0 is used. For 2-lane configuration, Lane0 and Lane1 are used. Bits7:4 = RESERVED. Read all 0's.	R/W
00103h	DPCD Lane 0 status	TRAINING_LANE0_SET Link Training Control_Lane0 Bits1:0 = DRIVE_CURRENT_SET 00 – Training Pattern 1 w/ level 0 01 – Training Pattern 1 w/ level 1 10 – Training Pattern 1 w/ level 2 11 – Training Pattern 1 w/ level 3 Bit2 = MAX_CURRENT_REACHED Set to 1 when the maximum driven current setting is reached. Note: Support of programmable drive current is optional. For example if there is only 1 level, then program Bits2:0 to 100 to indicate to the receiver that Level 1 is the maximum drive current. Support of independent drive current controlfor each lane is also optional. Bit4:3 = PRE-EMPHASIS_SET 00 = Training Pattern 2 w/o pre-emphasis 01 = Training Pattern 2 w/ pre-emphasis level 1 10 = Training Pattern 2 w/ pre-emphasis level 2 11 = Training Pattern 2 w/ pre-emphasis level 3 Bit5 = MAX_PRE-EMPHASIS_REACHED	R/W
00104h	DPCD Lane 1 status	Lane setting for lane 1. The definition is the same as lane 0	R/W
00105h	DPCD Lane 2 status	Lane setting for lane 2. The definition is the same as lane 0	R/W
00106h	DPCD Lane 3 status	Lane setting for lane 3. The definition is the same as lane 0	R/W

AUX listener specification

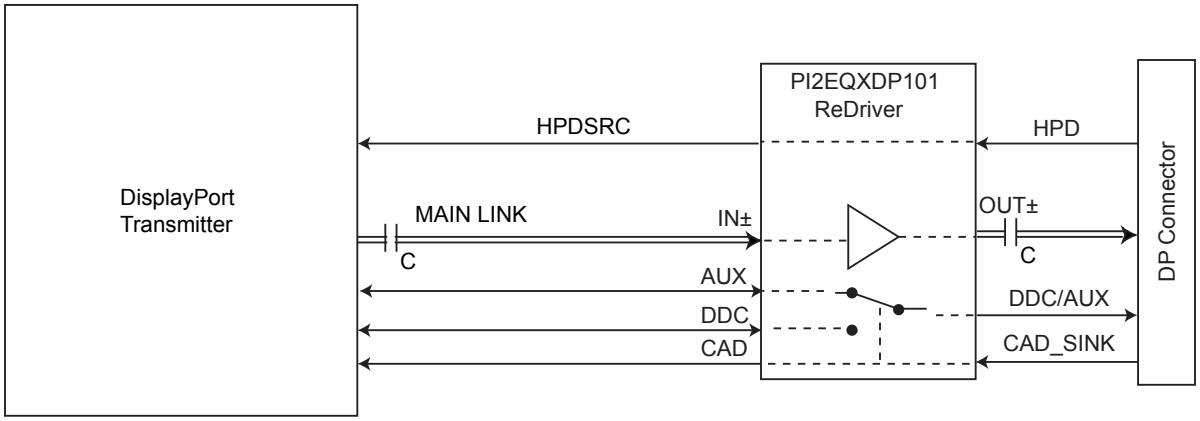
DP AUX command interpreter will support Native AUX CH Syntax. Mapping of I^2C onto AUX CH Syntax is not supported.

AUX command interpreter monitor AUX channel from requester and replier for transactions and stored AUX command from requester and reply command from replier that are related to the link settings.

The data from the following addresses will be extracted and stored into internal registers for controlling the ReDriver signal level, lane count and pre-emphasis setting.

00101h LANE_COUNT_SET
00103h TRAINING_LANE0_SET
00104h TRAINING_LANE1_SET
00105h TRAINING_LANE2_SET
00106h TRAINING_LANE3_SET

Application Diagram



Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C
Supply Voltage to Ground Potential ..... –0.5V to +4.6V
DC SIG Voltage ..... –0.5V to V_{DD} +0.5V
Current Output ..... -25mA to +25mA
Power Dissipation Continuous 500mW
Operating Temperature ..... 0 to +85°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics ($V_{DD}33$ = 3.3V ±5%, $V_{DD}15$ = 1.5V ±5%, T_A=0°C to 85°C)

Power Supply Characteristics

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
I_{ACTIVE_VDD15}	Current into $V_{DD}15$ when active	4-lanes operating at 2.7Gbps		150	250	mA
$I_{STANDBY\_VDD15}$	Current into $V_{DD}15$ when standby				10	mA
I_{ACTIVE_VDD33}	Current into $V_{DD}33$ when active	4-lanes operating at 2.7Gbps		0.1	1.0	mA
$I_{STANDBY\_VDD33}$	Current into $V_{DD}33$ when standby				0.1	mA
P_{ACTIVE}	Total active power	4-lane, operating 2.7Gbps			400	mW
$P_{standby}$	Total standby power				20	mW

HPD_SRC, HPD_Sink , CAD, CAD_Sink, Pin Charaxteristics

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
VIH	LVTTL input high voltage		2			V
VIL	LVTTL input low voltage				0.8	V
IIH	Input High-level current			43	80	uA
IIL	Input Low-level current			6	20	uA
VOH	LVTTL high level output voltage	IOH=-8mA	2.4			V
VOL	LVTTL low level output voltage	IOL= 8mA			0.4	V

AUX_SRC±, DDC_SCL/AUX+, DDC_SDA/AUX– pins (When configured as SCL and SDA pins)

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
IIH	Input High-level current			43	80	uA
IIL	Input Low-level current			6	20	uA

AUX_SRC±, DDC_SCL/AUX+, DDC_SDA/AUX– pins (When configured as AUX± pins)

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
IIH	Input High-level current			43	80	uA
IIL	Input Low-level current			6	20	uA

AUX Channel Electrical Specifications						
Symbol	**Parameter**	**Conditions**	**Min**	**Nom**	**Max**	**Units**
V_I	AUX Unit Interval	1Mbps including overhead of Mancester II coding	0.4	0.5	0.6	µS
Pre-charge pulses	Number of pre-charge pulses	Each pulse is a '0' in Manchester II code.	10		16	
Sync Pulses	Number of sync pulses			16		
$V_{AUX-DIFFp-p}$	AUX Peak-to-peak Voltage at a receiving Device	$V_{AUX-DIFFp-p}$ = 2*|V_{AUX+} – V_{AUX-}|	0.32		1.36	V
AUX_{ATTEN}	AUX attenuation	with 100-Ohm termination		1.5	2.0	dB
$V_{AUXP-DC}$	AUX+ DC Voltage Range		0		2.0	V
$V_{AUXN-DC}$	AUX– DC Voltage Range		1.3		3.3	
I_{AUX_SHORT}	AUX Short Circuit Current				90	mA
C_{AUX}	AUX AC Coupling Capacitor	The AUX CH AC coupling capacitor placed on the DisplayPort Source	75		200	nF

Main Link Receiver (Main RX) Specifications						
Symbol	**Parameters**	**Comments**	**Min.**	**Typ.**	**Max.**	**Units**
UI_High_Rate	Unit Interval for high bit rate (2.7 Gbps / lane)	Range is nominal +/-350ppm DisplayPort link RX does not require local crystal for link clock generation.		370		ps
UI_Low_Rate	Unit Interval for low bit rate (1.62 Gbps / lane)			617		ps
$V_{RX-DIFFp-p-HR}$	Differential Peak-to-peak Input Voltage at RX package pins	For High Bit Rate. Informative.	120		1500	mV
$T_{RX-EYE-MEDIAN-to-MAX-JITTER\_CHIP}$	Maximum time between the jitter median and maximum deviation from the median at Rx package pins				0.265	UI
T_{RX-EYE_CONN}	Minimum Receiver Eye Width at R_X-side connector pins	Note 1	0.25			UI
T_{RX-EYE_CHIP}	Minimum Receiver Eye Width at R_X package pins	Note 1	0.22			UI
$T_{RX-EYE-MEDIAN-to-MAX-JITTER\_CHIP}$	Maximum time between the jitter median and maximum deviation from the median at R_X package pins	Note 1			0.39	UI
$V_{RX-DC-CM}$	R_X DC Common Mode Voltage	Common mode voltage is equal to Vbias_Rx voltage	0		2.0	V
Z_{RX-DC}	DC Input Resistance		45	50	55	
$RL_{RX-DIFF}$	Differential Return Loss at 0.675GHz at R_X package pins	Straight loss line between 0.675 GHz and 1.35 GHz	12			dB
	Differential Return Loss at 1.35GHz at R_X package pins	Straight loss line between 0.675 GHz and 1.35 GHz	9			dB
$L_{RX-SKEW-INTER\_PAIR}$	Lane-to-Lane Output Skew at R_X package pins	Maximum skew limit between different RX lanes of a DisplayPort link.			5200	ps
$L_{RX-SKEW-INTRA\_PAIR\ High-Bit-Rate}$	Lane Intra-pair Output Skew at R_X package pins	For High Bit Rate Maximum skew limit between D+ and D- of the same lane.			100	ps
$L_{RX-SKEW-INTRA\_PAIR\_Reduced-Bit-Rate}$	Lane Intra-pair Output Skew at R_X package pins	For Reduced Bit Rate Maximum skew limit between D+ and D- of the same lane.			300	ps

Note:
1. For Reduced Bit Rate (1- TRX-EYE_CONN) specifies the allowable TJ. TRX-EYE-MEDIAN-to-MAX-JITTER specifies the total allowable DJ

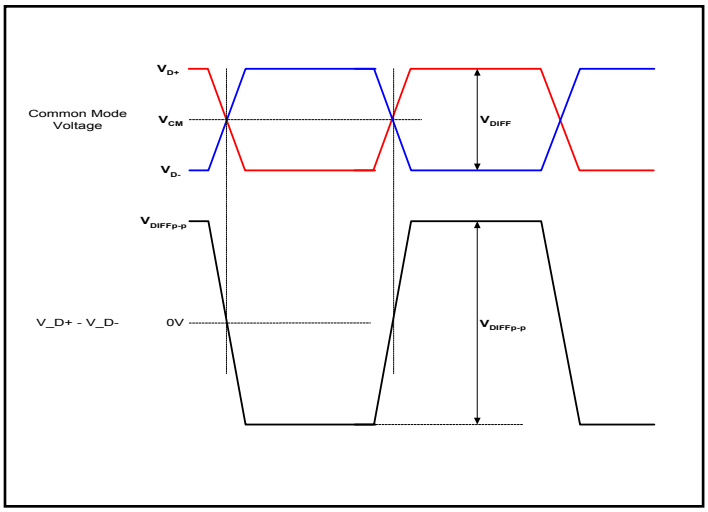
Main Link Transmitter (Main TX) Specifications

Symbol	Parameters	Comments	Min.	Typ.	Max.	Units
UI_High_Rate	Unit Interval for high bit rate (2.7 Gbps / lane)	High limit = +300ppm Low limit = -5300ppm		370		ps
UI_Low_Rate	Unit Interval for low bit rate (1.62 Gbps / lane)			617		ps
$V_{TX-DIFFp-p}$	Differential Peak-to-peak Output Voltage	HBR, VDD15 = 1.5V Voltage level 1 Voltage level 2 Voltage level 3 Voltage level 4	340 340 510 690 1020	 400 600 800 1200	1380 460 680 920 1380	mV
$V_{TX-PREEMP-RATIO}$	Output Pre-emphasis ratio	HBR, VDD15 = 1.5V No pre-emphasis 3.5 dB pre-emphasis 6.0 dB pre-emphasis 9.5 dB pre-emphasis	0.0 0.0 2.8 4.8 7.6	 0.0 3.5 6.0 9.5	11.4 0.0 4.2 7.2 11.4	dB
$T_{TX-EYE\_CHIP\_High\_Rate}$	Minimum TX Eye Width at Tx package pins	For High Bit Rate	0.726			UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER\_CHIP\_\_High\_Rate}$	Maximum time between the jitter median and maximum deviation from the median at Tx package pins	For High Bit Rate			0.137	UI
$T_{TX-EYE\_CHIP\_Low\_Rate}$	Minimum TX Eye Width at Tx package pins	For Reduced Bit Rate	0.82			UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER\_CHIP\_\_Low\_Rate}$	Minimum TX Eye Width at Tx package pins	For Reduced Bit Rate			0.09	UI
$T_{TX-RISE\_CHIP}$, $T_{TX-FALL\_CHIP}$	D+/D- TX Output Rise/Fall Time at Tx package pins	At 20%-to-80%	50		130	ps
$V_{TX-DC-CM}$	TX DC Common Mode Voltage	Common mode voltage is equal to Vbias_Tx voltage shown in Differential Waveform	0		1.5	V
$V_{TX-AC-CM}$	TX AC Common Mode Voltage	Measured at 1.62 GHz and 2.7 GHz (if supported), within the frequency tolerance range. Time-domain measurement using a spectrum analyzer.			20	mV
$I_{TX-SHORT}$	TX Short Circuit Current Limit	Total drive current of the transmitter when it is shorted to its ground.			50	mA
$R_{LTX-DIFF}$	Differential Return Loss at 0.675GHz at TX package pins	Straight loss line between 0.675 GHz and 1.35 GHz	12			dB
	Differential Return Loss at 1.35GHz at TX package pins	Straight loss line between 0.675 GHz and 1.35 GHz	9			dB

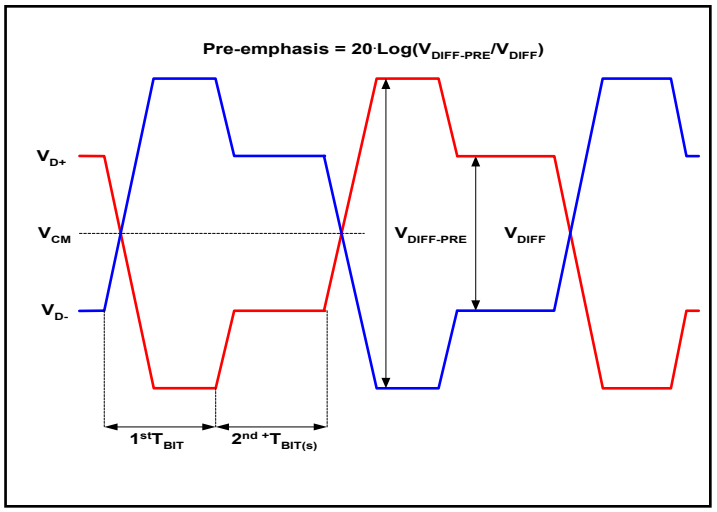
(Continued)

Symbol	Parameters	Comments	Min.	Typ.	Max.	Units
$L_{TX-SKEWINTER\_PAIR}$	Lane-to-Lane Output Skew at Tx package pins				2	UI
$L_{TX-SKEWINTRA\_PAIR}$	Lane Intra-pair Output Skew at Tx package pins				20	ps
$T_{TX-RISE\_FALL\_MISMATCH\_CHIPDIFF}$	Lane Intra-pair Rise-fall Time Mismatch at Tx package pins.	Informative. D+ rise to D- fall mismatch and D+ fall to D- rise mismatch.			5	%
C_{TX}	AC Coupling Capacitor	All DisplayPort Main Link lanes as well as AUX CH must be AC coupled. AC coupling capacitors must be placed on the transmitter side. Placement of AC coupling capacitors the receiver side is optional.	75		200	nF
J_{TOTAL}	Total Output Jitter				0.32	UIp-p

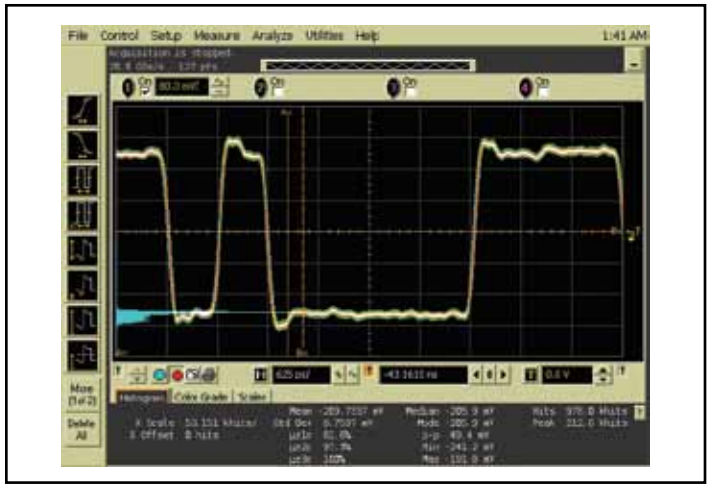
Notes:
1. Refer to Pre-emphasis waveform. For embedded connection, support of programmable voltage swing levels is optional.
2. Refer to Pre-emphasis waveform for definition of differential voltage. Support of no preemphasis, 3.5 dB and 6.0 dB pre-emphasis is required. Support of 9.5 dB level is optional. For embedded connection, support of programmable preemphasis levels is optional.



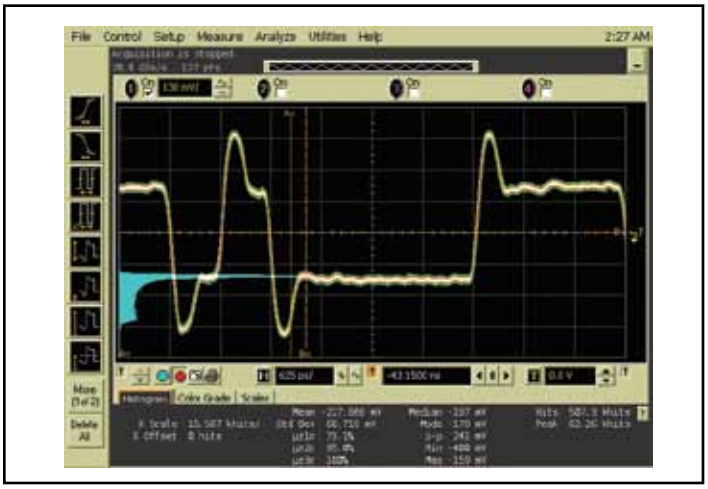
Definition of Differential Voltage and Differential Voltage Peak-to-Peak



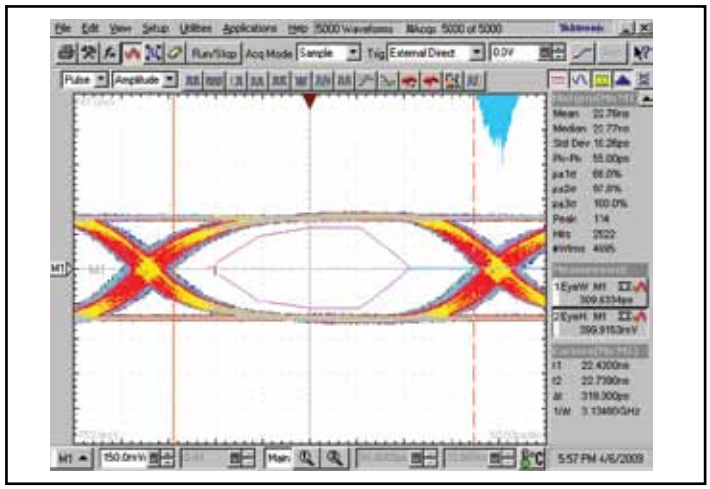
Definition of Pre-emphasis



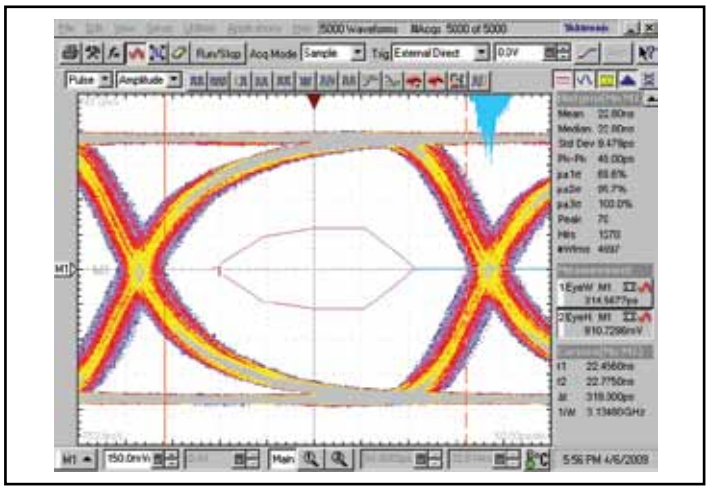
Output Waveform (400mV, 0dB pre-emphasis)



Output Waveform (400mV, 6dB pre-emphasis)

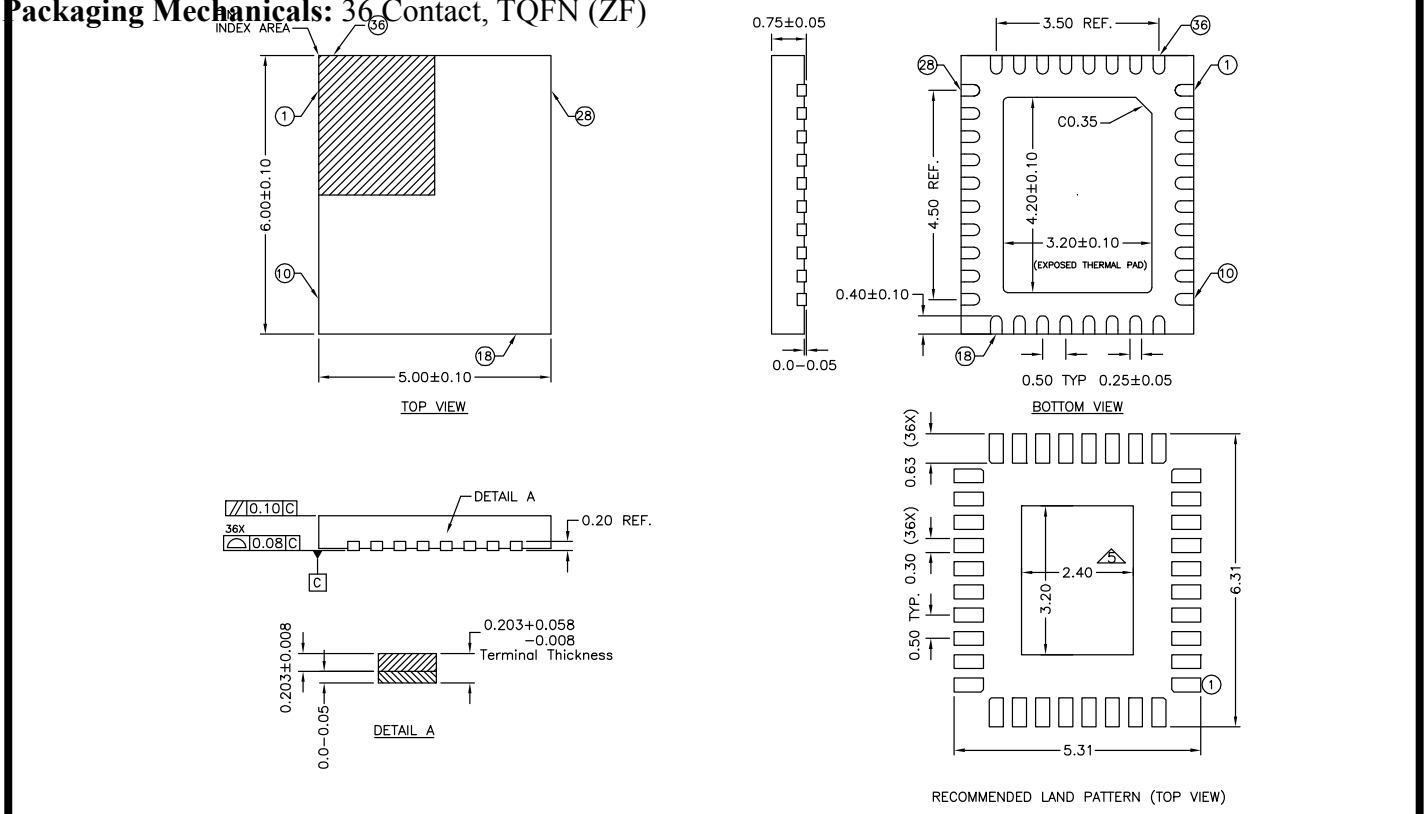


Output Eye Diagram (2.7Gbps, 400mV)



Output Eye Diagram (2.7Gbps, 1200mV)

Packaging Mechanicals: 36 Contact, TQFN (ZF)



NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO–220
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA

PERICOM® Enabling Serial Connectivity

~~DATE: 03/10/09~~

DESCRIPTION: 36-contact, Very Thin Fine Pitch Quad Flat No-Lead (TQFN)
PACKAGE CODE: ZF (ZF36)
DOCUMENT CONTROL #: PD-2023 **REVISION: C**

09-0143

Ordering Information

Ordering Code	Package Code	Package Description
PI2EQXDP101-AZFE	ZF	36-Contact, Pb-Free & Green (TQFN)

Notes:
- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- Adding an X suffix = Tape/Reel