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9P960 Active

Dual Channel DDRII/III Zero Delay Buffer

Dual Channel DDRII/III Zero Delay Buffer

Features

- High performance, low jitter zero delay buffer
- I2C for functional and output control
- Dual bank 1-6 differential clock distribution
- 2 separate feedback in & out for input to output
- synchronization for each bankSupports up to 4 DDR DIMMs
- Supports up to DDRII - 1066MHz
- Supports up to DDRIII (1.8V core) - 1333MHz

Product Options

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Orderable Part ID	Part Status	Pkg. Code	Pkg. Type	Lead Count (#)	Temp. Grade	Pb (Lead) Free	Carrier Type	Buy Sample
9P960AFLF	Active	PVG48	SSOP	48	C	Yes	Tube	Availability
9P960AFLFT	Active	PVG48	SSOP	48	C	Yes	Reel	Availability

Technical Documentation

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Title	Other Languages	Type	Format	File Size	Date
Datasheets & Errata					
9P960 Datasheet	-	Datasheet	PDF	131 KB	Nov 20, 2013
Application Notes & White Papers					
AN-828 Termination - LVPECL	-	Application Note	PDF	229 KB	Jul 5, 2016
AN-815 Understanding Jitter Units	-	Application Note	PDF	476 KB	Apr 23, 2014
AN-844 Termination - AC Coupling Clock Receivers	-	Application Note	PDF	82 KB	May 12, 2014
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PCNs & PDNs					
PCN# : A1506-02 Gold wire to Copper wire	-	Product Change Notice	PDF	35 KB	Oct 7, 2015
PCN# : A1504-04 Assembly Transfer from Amkor Philippines to OSE Taiwan	-	Product Change Notice	PDF	484 KB	Jul 1, 2015
PCN# : TB1303-02 Change of Tape & Reel Packing Method for Selective Products	-	Product Change Notice	PDF	361 KB	Mar 23, 2013
Other					
The IDT Communications Products Advantage	-	Overview	PDF	2.54 MB	Feb 13, 2017
The IDT Consumer Products Advantage	-	Overview	PDF	6.67 MB	Jan 27, 2017
IDT Clock Generation Overview	日本語	Overview	PDF	1.83 MB	Apr 28, 2016
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