National Semiconductor

August 2002

DS92LV040A
4 Channel Bus LVDS Transceiver

General Description

The DS92LV040A is one in a series of Bus LVDS transceivers designed specifically for high speed, low power backplane or cable interfaces. The device operates from a single 3.3V power supply and includes four differential line drivers and four receivers. To minimize bus loading, the driver outputs and receiver inputs are internally connected. The device also features a flow through pin out which allows easy PCB routing for short stubs between its pins and the connector.

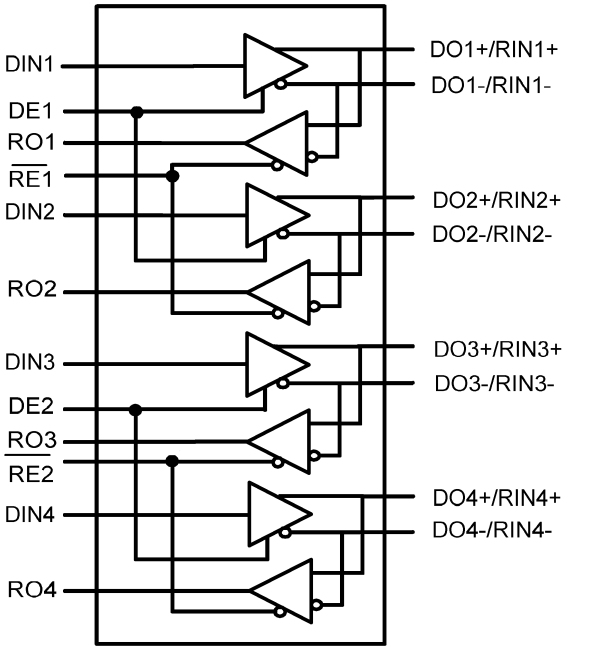
The driver translates 3V LVTTL levels (single-ended) to differential Bus LVDS (BLVDS) output levels. This allows for high speed operation while consuming minimal power and reducing EMI. In addition, the differential signaling provides common mode noise rejection greater than ±1V.

The receiver threshold is less than +0/−70 mV. The receiver translates the differential Bus LVDS to standard (LVTTL/LVCMOS) levels. (See Applications Information Section for more details.)

Features

- Bus LVDS Signaling
- Propagation delay: Driver 2.3ns max, Receiver 3.2ns max
- Low power CMOS design
- 100% Transition time 1ns driver typical, 1.3ns receiver typical
- High Signaling Rate Capability (above 155 Mbps)
- 0.1V to 2.3V Common Mode Range for V_{ID} = 200mV
- 70 mV Receiver Sensitivity
- Supports open and terminated failsafe on port pins
- 3.3V operation
- Glitch free power up/down (Driver & Receiver disabled)
- Light Bus Loading (5 pF typical) per Bus LVDS load
- Designed for Double Termination Applications
- Balanced Output Impedance
- Product offered in 44 pin LLP (Leadless Leadframe Package) package
- High impedance Bus pins on power off (V_{CC} = 0V)

Simplified Functional Diagram



10133601

© 2002 National Semiconductor Corporation

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	4.0V
Enable Input Voltage (DE, $\overline{RE}$)	−0.3V to (V_{CC} +0.3V)
Driver Input Voltage (D_{IN})	−0.3V to (V_{CC} +0.3V)
Receiver Output Voltage (R_{OUT})	−0.3V to (V_{CC} +0.3V)
Bus Pin Voltage (DO/RI±)	−0.3V to +3.9V
ESD (Note 4)	
(HBM 1.5 kΩ, 100 pF)	>4kV
Machine Model	>250V
Maximum Package Power Dissipation at 25˚C	
LLP(Note 3)	4.8 W
Derate LLP Package	38.8mW/˚C
θ_{ja} (Note 3)	25.8˚C/W
θ_{jc}	25.5˚C/W
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature (Soldering, 4 sec.)	260˚C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	3.0	3.6	V
Receiver Input Voltage	0.0	2.4	V
Operating Free Air Temperature	−40	+85	˚C
Slowest Input Edge Rate			
(Note 7)(20% to 80%)			Δt/ΔV
Data		1.0	ns/V
Control		3.0	ns/V

DC Electrical Characteristics

Over recommended operating supply voltage and temperature ranges unless otherwise specified (Notes 2, 4)

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
V_{OD}	Output Differential Voltage	R_L = 27Ω, *Figure 1*		DO+/RI+, DO−/RI−	200	300	460	mV
ΔV_{OD}	V_{OD} Magnitude Change					5	27	mV
V_{OS}	Offset Voltage				1.1	1.3	1.5	V
ΔV_{OS}	Offset Magnitude Change					5	10	mV
V_{OHD}	Driver Output High Voltage	R_L = 27Ω				1.4	1.65	V
V_{OLD}	Driver Output Low Voltage	R_L = 27Ω			0.95	1.1		V
I_{OSD}	Driver Output Short Circuit Current (Note 11)	V_{OD} = 0V, DE = V_{CC}, Driver outputs shorted together				|30|	| 45|	mA
V_{OHR}	Receiver Voltage Output High (Note 12)	V_{ID} = +300 mV	I_{OH} = −4 mA	R_{OUT}	V_{CC}−0.2			V
		Inputs Open			V_{CC}−0.2			V
		Inputs Terminated, R_L = 27Ω			V_{CC}−0.2			V
V_{OLR}	Receiver Voltage Output Low	I_{OL} = 4.0 mA, V_{ID} = −300 mV				0.05	0.100	V
I_{OD}	Receiver Output Dynamic Current (Note 11)	V_{ID} = 300mV, V_{OUT} = V_{CC}−1.0V			−50	|33|		mA
		V_{ID} = −300mV, V_{OUT} = 1.0V				|36|	60	mA
V_{TH}	Input Threshold High (Note 9)	DE = 0V, Over common mode range		DO+/RI+, DO−/RI−		−40	0	mV
V_{TL}	Input Threshold Low (Note 9)				−70	−40		mV
V_{CMR}	Receiver Common Mode Range				|V_{ID}|/2		2.4 − |V_{ID}|/2	V
I_{IN}	Input Current	DE = 0V, $\overline{RE}$ = 2.4V, V_{IN} = +2.4V or 0V			−20	±1	+20	μA
		V_{CC} = 0V, V_{IN} = +2.4V or 0V			−20	±1	+20	μA

DC Electrical Characteristics (Continued)

Over recommended operating supply voltage and temperature ranges unless otherwise specified (Notes 2, 4)

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
V_{IH}	Minimum Input High Voltage		D_{IN}, DE, $\overline{RE}$	2.0		V_{CC}	V
V_{IL}	Maximum Input Low Voltage			GND		0.8	V
I_{IH}	Input High Current	$V_{IN} = V_{CC}$ or 2.4V		–20	±2.5	+20	µA
I_{IL}	Input Low Current	V_{IN} = GND or 0.4V		–20	±2.5	+20	µA
V_{CL}	Input Diode Clamp Voltage	I_{CLAMP} = –18 mA		–1.5	–0.8		V
I_{CCD}	Power Supply Current Drivers Enabled, Receivers Disabled	No Load, DE = $\overline{RE}$ = V_{CC}, DIN = V_{CC} or GND	V_{CC}		20	40	mA
I_{CCR}	Power Supply Current Drivers Disabled, Receivers Enabled	DE = $\overline{RE}$ = 0V, V_{ID} = ±300mV			27	40	mA
I_{CCZ}	Power Supply Current, Drivers and Receivers TRI-STATE	DE = 0V; $\overline{RE}$ = V_{CC}, DIN = V_{CC} or GND			28	40	mA
I_{CC}	Power Supply Current, Drivers and Receivers Enabled	DE = V_{CC}; $\overline{RE}$ = 0V, DIN = V_{CC} or GND, R_L = 27Ω			70	100	mA
I_{OFF}	Power Off Leakage Current	V_{CC} = 0V or OPEN, D_{IN}, DE, $\overline{RE}$ = 0V or OPEN, $V_{APPLIED}$ = 3.6V (Port Pins)	DO+/RI+, DO–/RI–	–20		+20	µA
C_{OUTPUT}	Capacitance @ Bus Pins		DO+/RI+, DO–/RI–		5		pF
c_{OUTPUT}	Capacitance @ R_{OUT}		R_{OUT}		5		pF

AC Electrical Characteristics

Over recommended operating supply voltage and temperature ranges unless otherwise specified (Note 7)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIFFERENTIAL DRIVER TIMING REQUIREMENTS						
t_{PHLD}	Differential Prop. Delay High to Low (Note 9)	R_L = 27Ω, *Figures 2, 3*, C_L = 10 pF	1.0	1.5	2.3	ns
t_{PLHD}	Differential Prop. Delay Low to High (Note 9)		1.0	1.5	2.3	ns
t_{SKD1}	Differential Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$ (duty cycle)(Note 10), (Note 9)			80	160	ps
t_{CCSK}	Channel to Channel Skew (all 4 channels), (Note 9)			220	400	ps
t_{TLH}	Transition Time Low to High (20% to 80%)		0.4	0.75	1.3	ns
t_{THL}	Transition Time High to Low (80% to 20%)		0.4	0.75	1.3	ns
t_{PHZ}	Disable Time High to Z	R_L = 27Ω, *Figures 4, 5*, C_L = 10 pF		5.0	10	ns
t_{PLZ}	Disable Time Low to Z			5.0	10	ns
t_{PZH}	Enable Time Z to High			5.0	10	ns
t_{PZL}	Enable Time Z to Low			5.0	10	ns
f_{MAXD}	Guaranteed operation per data sheet up to the Min. Duty Cycle 45/55%,Transition time ≤ 25% of period (Note 9)		85	125		MHz

AC Electrical Characteristics (Continued)

Over recommended operating supply voltage and temperature ranges unless otherwise specified (Note 7)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIFFERENTIAL RECEIVER TIMING REQUIREMENTS						
t_{PHLDR}	Differential Prop. Delay High to Low (Note 9)	*Figures 6, 7*, C_L = 15 pF	1.6	2.4	3.2	ns
t_{PLHDR}	Differential Prop Delay Low to High (Note 9)		1.6	2.4	3.2	ns
t_{SDK1R}	Differential Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$ (duty cycle)(Note 10), (Note 9)			85	160	ps
t_{CCSKR}	Channel to Channel Skew (all 4 channels)(Note 9)			140	300	ps
t_{TLHR}	Transition Time Low to High (10% to 90%) (Note 9)		0.850	1.250	2.0	ns
t_{THLR}	Transition Time High to Low (90% to 10%) (Note 9)		0.850	1.030	2.0	ns
t_{PHZ}	Disable Time High to Z	R_L = 500Ω, *Figures 8, 9*, C_L = 15 pF		3.0	10	ns
t_{PLZ}	Disable Time Low to Z			3.0	10	ns
t_{PZH}	Enable Time Z to High			3.0	10	ns
t_{PZL}	Enable Time Z to Low			3.0	10	ns
f_{MAXR}	Guaranteed operation per data sheet up to the Min. Duty Cycle 45/55%,Transition time ≤ 25% of period (Note 9)		85	125		MHz

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified except V_{OD}, ΔV_{OD} and V_{ID}.

Note 3: Package must be mounted to pc board in accordance with AN-1187 to achieve thermals.

Note 4: All typicals are given for V_{CC} = +3.3V and T_A = +25˚C, unless otherwise stated.

Note 5: ESD Rating: HBM (1.5 kΩ, 100 pF) > 4 kV EIAJ (0Ω, 200 pF) > 250.

Note 6: C_L includes probe and fixture capacitance.

Note 7: Generator waveforms for all tests unless otherwise specified: f = 25 MHz, Z_O = 50Ω, t_r, t_f = <1.0 ns (0%–100%). To ensure fastest propagation delay and minimum skew, data input edge rates should be equal to or faster than 1ns/V; control signals equal to or faster than 3ns/V. In general, the faster the input edge rate, the better the AC performance.

Note 8: The DS92LV040A functions within datasheet specification when a resistive load is applied to the driver outputs.

Note 9: Propagation delays, transition times, and receiver threshold are guaranteed by design and characterization.

Note 10: t_{SKD1} $\lvert t_{PHLD} - t_{PLHD} \rvert$ is the worst case pulse skew (measure of duty cycle) over recommended operation conditions.

Note 11: Only one output at a time should be shorted, do not exceed maximum package power dissipation capacity.

Note 12: V_{OH} fail-safe terminated test performed with 27Ω connected between RI+ and RI– inputs. No external voltage is applied.

Note 13: Chip to Chip skew is the difference in differential propagation delay between any channels of any devices, either edge.

Applications Information

General application guidelines and hints may be found in the following application notes: AN-808, AN-977, AN-971, and AN-903.

BLVDS drivers and receivers are intended to be used in a differential backplane configuration. Transceivers or receivers are connected to the driver through a balanced media such as differential PCB traces. Typically, the characteristic differential impedance of the media (Zo) is in the range of 50Ω to 100Ω. Two termination resistors of ZoΩ each are placed at the ends of the transmission line backplane. The termination resistor converts the current sourced by the driver into a voltage that is detected by the receiver. The effects of mid-stream connector(s), cable stub(s), and other impedance discontinuity as well as ground shifting, noise margin limits, and total termination loading must be taken into account. The DS92LV040A differential line driver is a balanced current mode design. A current mode driver, generally speaking has a high output impedance (100 ohms) and supplies a reasonably constant current for a range of loads (a voltage mode driver on the other hand supplies a constant voltage for a range of loads). Current is switched through the load in one direction to produce a logic state and in the other direction to produce the other logic state. The output current is typically 12 mA. The current changes as a function of load resistor. The current mode requires (as discussed above) that a resistive termination be employed to terminate the signal and to complete the loop. Unterminated configurations are not allowed. The 12 mA loop current will develop a differential voltage of about 300mV across a 27Ω (double terminated 54Ω differential transmission backplane) effective resistance, which the receiver detects with a 230 mV minimum differential noise margin neglecting resistive line losses (driven signal minus receiver threshold (300 mV – 70 mV = 230 mV)). The signal is centered around +1.2V (Driver Offset, VOS) with respect to ground. Note that the steady-state voltage (VSS) peak-to-peak swing is twice the differential voltage (VOD) and is typically 600 mV. The current mode driver provides substantial benefits over voltage mode drivers, such as an RS-422 driver. Its quiescent current remains relatively flat versus switching frequency. Whereas the RS-422 voltage mode driver increases exponentially in most case between 20 MHz–50 MHz. This is due to the overlap current that flows between the rails of the device when the internal gates switch. Whereas the current mode driver switches a fixed current between its output without any substantial overlap current. This is similar to some ECL and PECL devices, but without the heavy static ICC requirements of the ECL/PECL designs. LVDS requires 80% less current than similar PECL devices. AC specifications for the driver are a tenfold improvement over other

Applications Information (Continued)

existing RS-422 drivers. The TRI-STATE function allows the driver outputs to be disabled, thus obtaining an even lower power state when the transmission of data is not required.

There are a few common practices which should be implied when designing PCB for Bus LVDS signaling. Recommended practices are:

- Use at least 4 PCB board layer (Bus LVDS signals, ground, power and TTL signals).
- Keep drivers and receivers as close to the (Bus LVDS port side) connector as possible.
- Bypass each Bus LVDS device and also use distributed bulk capacitance between power planes. Surface mount capacitors placed close to power and ground pins work best. Three or more high frequency, multi-layer ceramic (MLC) surface mount (0.1 µF, 0.01 µF, 0.001 µF) in parallel should be used between each V_{CC} and ground.

  Multiple vias should be used to connect V_{CC} and Ground planes to the pads of the by-pass capacitors.

  In addition, it may be necessary to randomly distribute by-pass capacitors of different values (200pF to 1000pF) to achieve different resonant frequencies.
- Use the termination resistor which best matches the differential impedance of your transmission line.
- Leave unused Bus LVDS receiver inputs open (floating). Limit traces on unused inputs to <0.5 inches.
- Isolate TTL signals from Bus LVDS signals

MEDIA (CONNECTOR or BACKPLANE) SELECTION:

- The backplane and connectors should have a matched differential impedance. Use controlled impedance traces which match the differential impedance of your transmission medium (ie. backplane or cable) and termination resistor(s). Run the differential pair trace lines as close together as possible as soon as they leave the IC . This will help eliminate reflections and ensure noise is coupled as common-mode. In fact, we have seen that differential signals which are 1mm apart radiate far less noise than traces 3mm apart since magnetic field cancellation is much better with the closer traces. Plus, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver. Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result. (Note the velocity of propagation, v = c/Er where c (the speed of light) = 0.2997mm/ps or 0.0118 in/ps). Do not rely solely on the autoroute function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number of vias and other discontinuity on the line. Avoid 90˚ turns (these cause impedance discontinuity). Use arcs or 45˚ bevels. Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuity in differential impedance. Minor violations at connection points are allowable.
- Stub Length: Stub lengths should be kept to a minimum. The typical transition time of the DS92LV040A BLVDS output is 0.75ns (20% to 80%). The extrapolated 100 percent time is 0.75/0.6 or 1.25ns. For a general approximation, if the electrical length of a trace is greater than 1/5 of the transition edge, then the trace is considered a transmission line. For example, 1.25ns/5 is 250 picoseconds. Let velocity equal 160ps per inch for a typical loaded backplane. Then maximum stub length is 250ps/160ps/in or 1.56 inches. To determine the maximum stub for your backplane, you need to know the propagation velocity for the actual conditions (refer to application notes AN 905 and AN 808).

PACKAGE and SOLDERING INFORMATION:

- Refer to packaging application note AN-1187. This application note details the package attachment methods to achieve the correct solderability and thermal results.

Applications Information (Continued)

TABLE 1. Functional Table

MODE SELECTED	DE	$\overline{RE}$
DRIVER MODE	H	H
RECEIVER MODE	L	L
TRI-STATE™ MODE	L	H
LOOP BACK MODE	H	L

TABLE 2. Transmitter Mode

INPUTS		OUTPUTS	
DE	**D_{IN}**	**DO+**	**DO–**
H	L	L	H
H	H	H	L
H	0.8V< D_{IN} <2.0V	X	X
L	X	Z	Z

TABLE 3. Receiver Mode

INPUTS		OUTPUT
$\overline{RE}$	**(RI+) – (RI–)**	
L	L (< –70 mV)	L
L	H (> 0 mV)	H
L	–70 mV < V_{ID} < 0 mV	X
H	X	Z

X = High or Low logic state
L = Low state
Z = High impedance state
H = High state

Test Circuits and Timing Waveforms

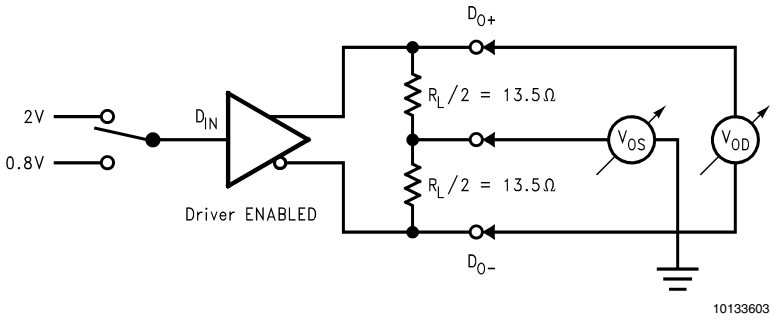


FIGURE 1. Differential Driver DC Test Circuit

Test Circuits and Timing Waveforms (Continued)

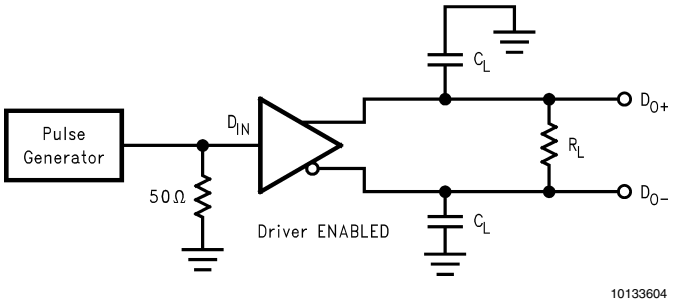


FIGURE 2. Differential Driver Propagation Delay and Transition Time Test Circuit

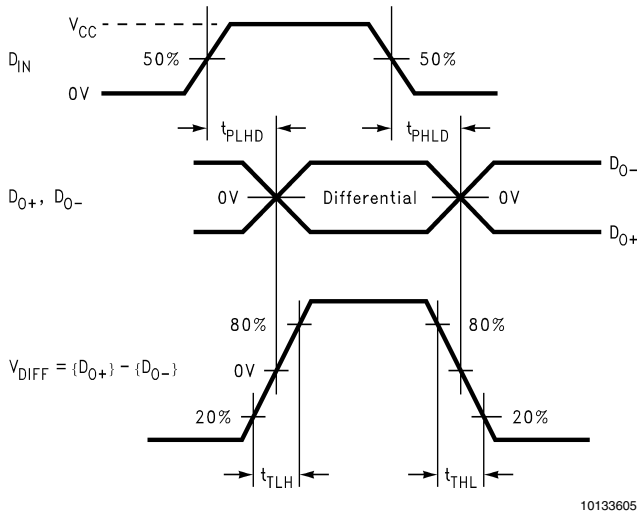


FIGURE 3. Differential Driver Propagation Delay and Transition Time Waveforms

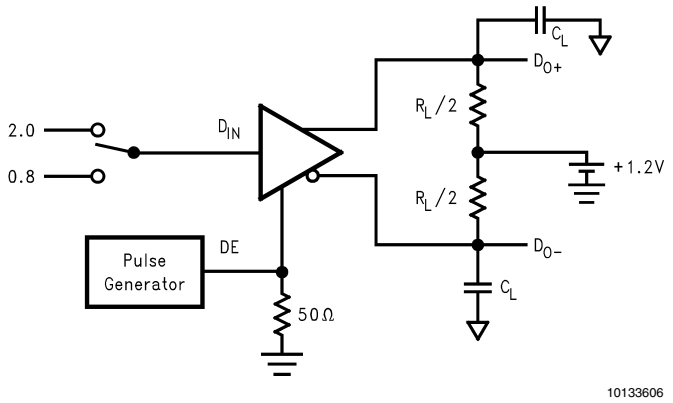


FIGURE 4. Driver TRI-STATE Delay Test Circuit

Test Circuits and Timing Waveforms (Continued)

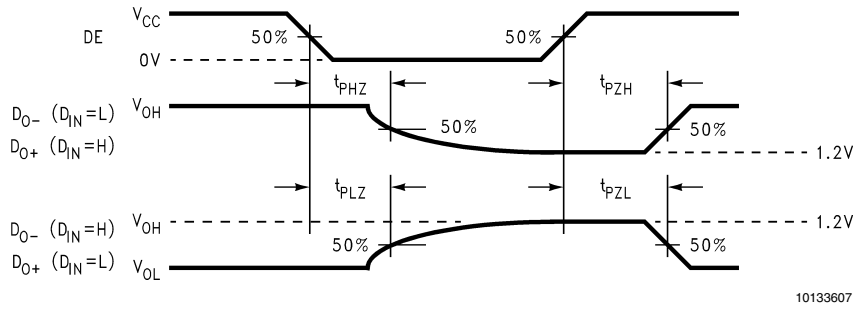


FIGURE 5. Driver TRI-STATE Delay Waveforms

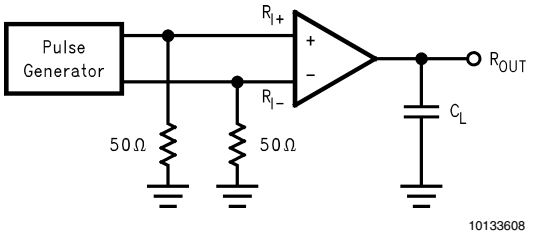


FIGURE 6. Receiver Propagation Delay and Transition Time Test Circuit

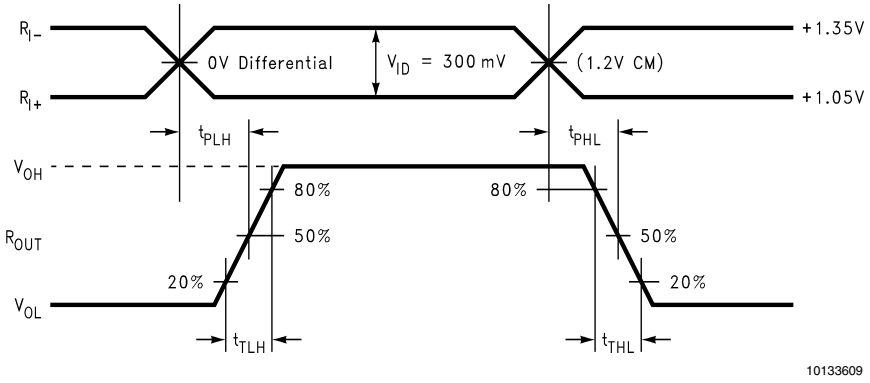


FIGURE 7. Receiver Propagation Delay and Transition Time Waveforms

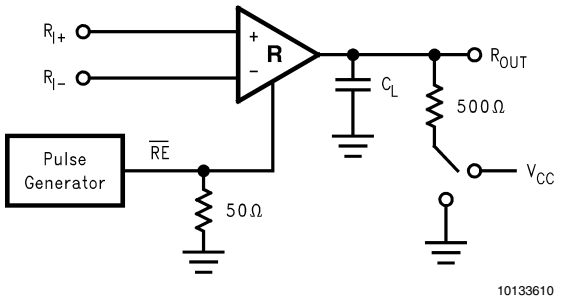


FIGURE 8. Receiver TRI-STATE Delay Test Circuit

Test Circuits and Timing Waveforms (Continued)

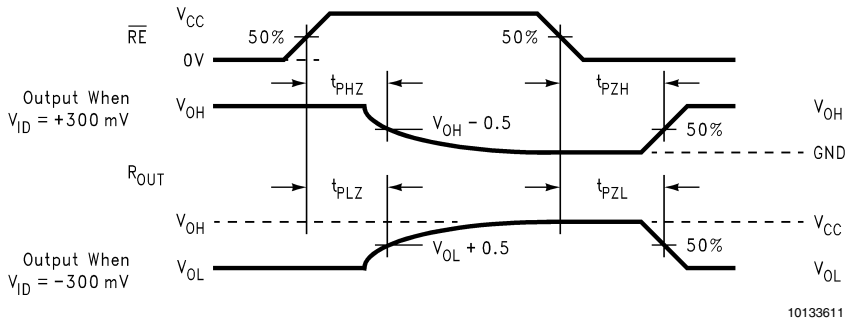
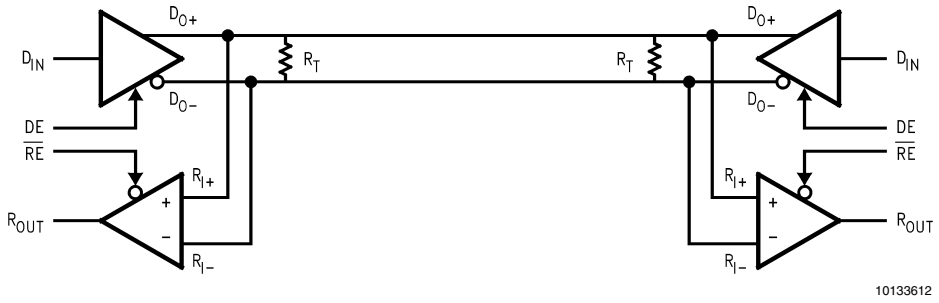
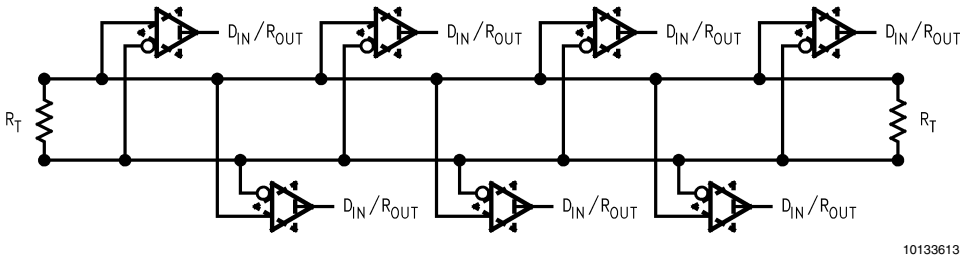


FIGURE 9. Receiver TRI-STATE Delay Waveforms

Typical Bus Application Configurations

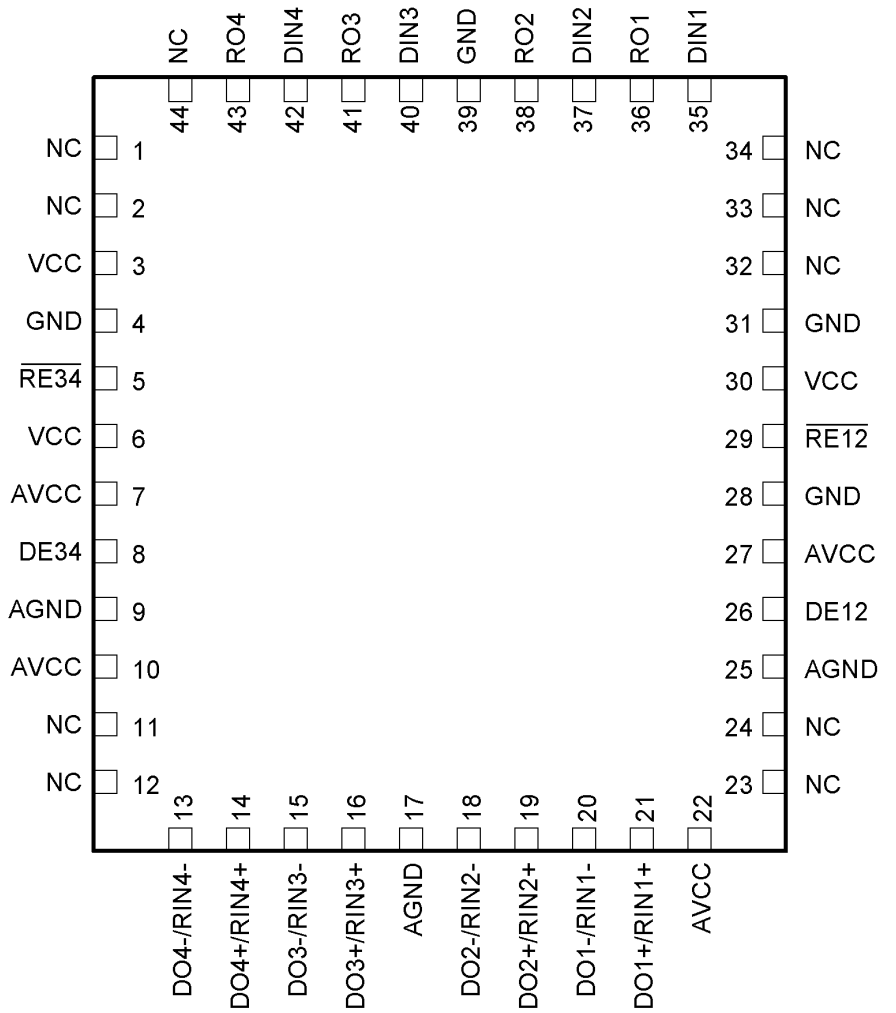


Bidirectional Half-Duplex Point-to-Point Applications



Multi-Point Bus Applications

Connection Diagram



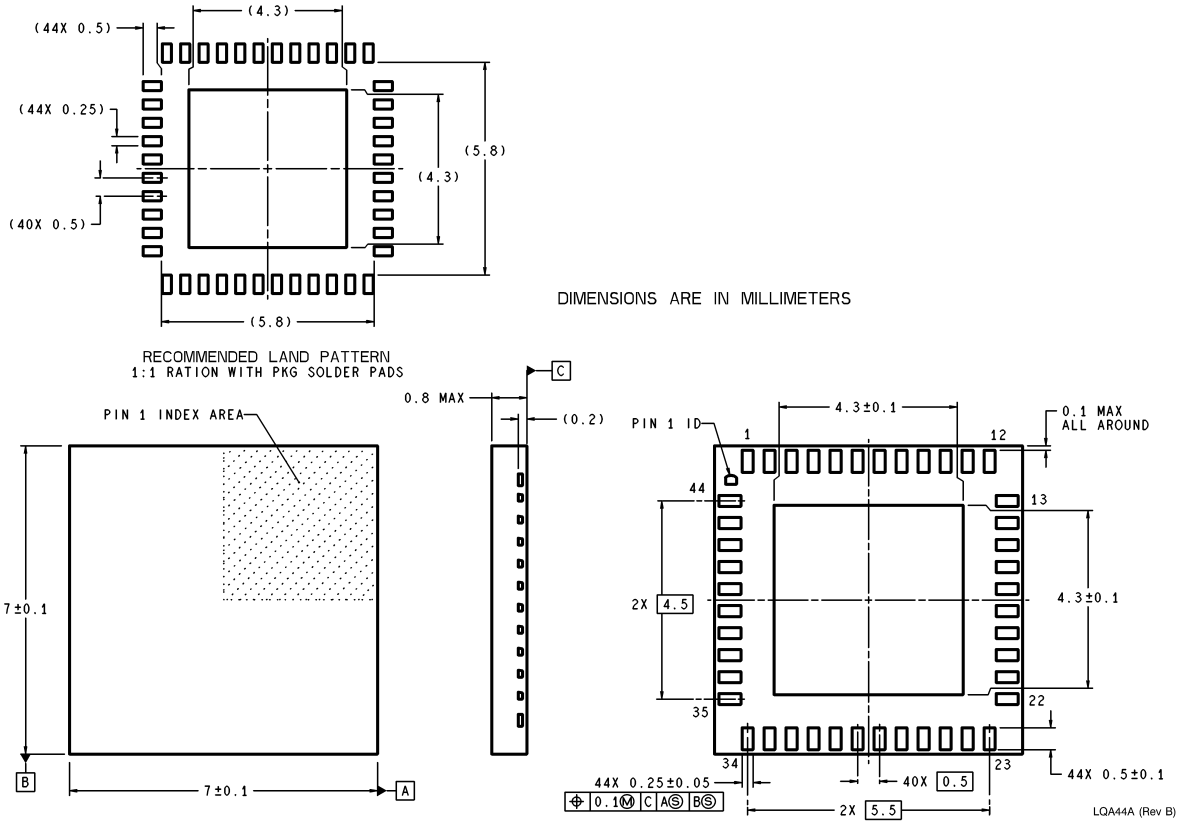
Top View
Order Number DS92LV040ATLQA
See NS Package Number LQA44A

Pinout Description

Pin Name	Pin #	Input/Output	Descriptions
DO+/RI+	14, 16, 19, 21	I/O	True Bus LVDS Driver Outputs and Receiver Inputs.
DO–/RI–	13, 15, 18, 20	I/O	Complimentary Bus LVDS Driver Outputs and Receiver Inputs.
D_{IN}	35, 37, 40, 42	I	LVTTL Driver Input. No pull up or pull down is attached to this pin
RO	36, 38, 41, 43	O	LVTTL Receiver Output.
$\overline{RE12}$	29	I	Receiver Enable LVTTL Input (Active Low). This pin, when low, configures receiver outputs, RO1 and RO2 active. When this pin is high, RO1 and RO2 are TRI-STATE. If this pin is floating, a weak current source to V_{CC} causes RO1 and RO2 to be TRI-STATE
$\overline{RE34}$	5	I	Receiver Enable LVTTL Input (Active Low). This pin, when low, configures receiver outputs, RO3 and RO4 active. When this pin is high, RO3 and RO4 are TRI-STATE. If this pin is floating, a weak current source to V_{CC} causes RO3 and RO4 to be TRI-STATE
DE12	26	I	Driver Enable LVTTL Input (Active High). This pin, when high, configures driver outputs, DO1+/RIN1+, DO1–/RIN1– and DO2+/RIN2+, DO2–/RIN2– active. When this pin is low, driver outputs 1 and 2 are TRI-STATE. If this pin is floating, a weak current source to V_{CC} causes driver outputs 1 and 2 to be active
DE34	8	I	Driver Enable LVTTL Input (Active High). This pin, when high, configures driver outputs, DO3+/RIN3+, DO3–/RIN3– and DO4+/RIN4+, DO4–/RIN4– active. When this pin is low, driver outputs 3 and 4 are TRI-STATE. If this pin is floating, a weak current source to V_{CC} causes driver outputs 3 and 4 to be active
GND	4, 28, 31, 39	Ground	Ground for digital circuitry (must connect to GND on PC board). These pins connected internally.
V_{CC}	3, 6, 30	Power	V_{CC} for digital circuitry (must connect to V_{CC} on PC board). These pins connected internally.
AGND	9, 17, 25	Ground	Ground for analog circuitry (must connect to GND on PC board). These pins connected internally.
AV_{CC}	7, 10, 22, 27	Power	Analog V_{CC} (must connect to V_{CC} on PC board). These pins connected internally.
NC	1, 2, 11, 12, 23, 24, 32, 33, 34, 44	N/A	Reserved for future use, leave open circuit.
DAP		GND	Must connect to GND plane through vias to achieve the theta ja specified under Absolute Maximum Ratings. The DAP (die attach pad) is the heat transfer material that is centered on the bottom of the LLP package. Refer to application note AN-1187 for attachment details.

All dimensions are in millimeters

Physical Dimensions inches (millimeters) unless otherwise noted



44 pin Plastic LLP Package
Order Number DS92LV040ATLQA
NS Package Number LQA44A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
Americas
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: ap.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.