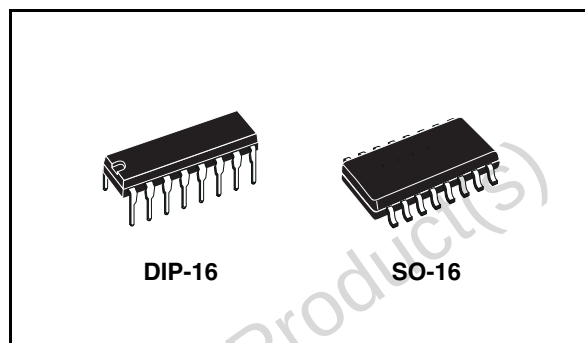


Dual decade counter

Features

- High Speed:
 $f_{MAX} = 79\text{MHz}$ (Typ.) at $V_{CC} = 6\text{V}$
- Low power dissipation:
 $I_{CC} = 4\mu\text{A}$ (Max.) at $T_A = 25^\circ\text{C}$
- High noise immunity:
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)
- Balanced propagation delays:
 $t_{PLH} \approx t_{PHL}$
- Wide operating voltage range:
 $V_{CC} \text{ (Opr)} = 2\text{V to } 6\text{V}$
- Pin and function compatible with 74 series 390



Description

The M74HC390 is an high speed CMOS dual decade counter fabricated with silicon gate C2MOS technology.

This dual decade counter contains two independent ripple carry counters. Each counter is composed of a divide by two and divide by five counter. The divide by two and divide by five counters can be cascaded to form dual decade, dual biquinary, or various combination up to a single divide by 100 counter.

Each 4-bit counter is increased on the high to low transition (negative edge) of the clock input, and each has an independent clear input. When clear is set low all four bits of each counter are set to low. This enables count truncation and allows the implementation of divide by N counter configuration.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

Order codes

Part number	Package	Packaging
M74HC390B1R	DIP-14	Tube
M74HC390RM13TR	SO-14	Tape and reel

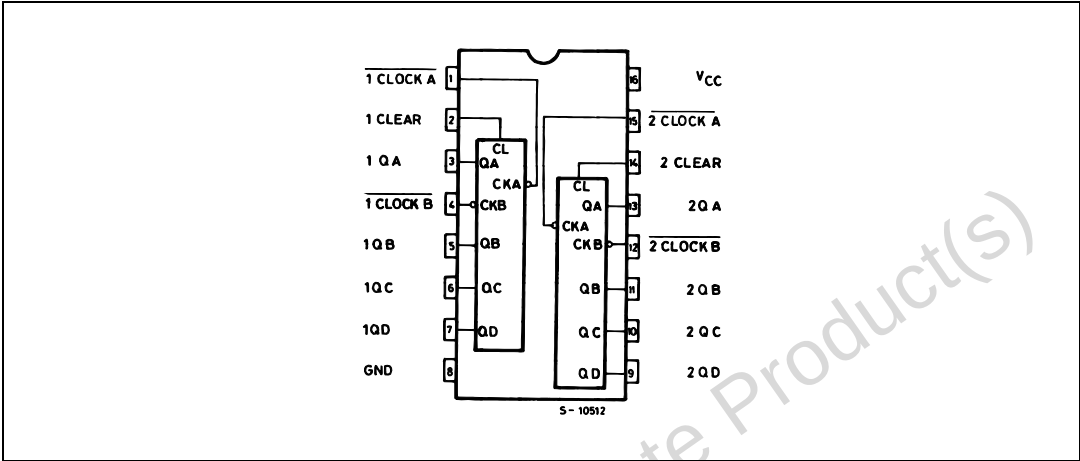
Contents

1	Pin settings	3
1.1	Pin connection	3
1.2	Pin description	3
2	Device summary	4
3	Truth table	5
4	Block and logic diagrams	6
5	Timing chart	7
6	Maximum rating	8
6.1	Recommended operating conditions	8
7	Electrical characteristics	9
8	Test circuit	12
9	Waveforms	12
10	Package mechanical data	13
11	Revision history	16

1 Pin settings

1.1 Pin connection

Figure 1. Pin connection (top through view)



1.2 Pin description

Table 1. Pin description

Pin N°	Symbol	Name and function
1, 15	$\overline{1 \text{ CLOCK A}}$ $\overline{2 \text{ CLOCK B}}$	Clock input divide by 2 section (HIGH to LOW Edge-Triggered)
2, 14	$\overline{1 \text{ CLEAR}}$ $\overline{2 \text{ CLEAR}}$	Asynchronous master reset inputs
3, 5, 6, 7	1QA to 1QD	Flip flop outputs
4, 12	$\overline{1 \text{ CLOCK A}}$ $\overline{2 \text{ CLOCK B}}$	Clock input divide by 5 section (HIGH to LOW Edge-Triggered)
13, 11, 10, 9	2QA to 2QD	Flip flop outputs
8	GND	Ground (0V)
16	Vcc	Positive supply voltage

2 Device summary

Figure 2. Input and output equivalent circuit

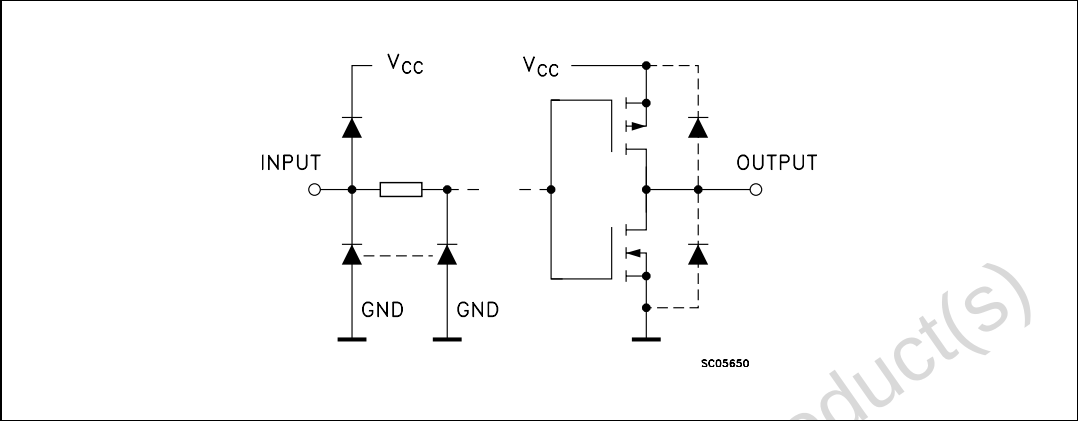
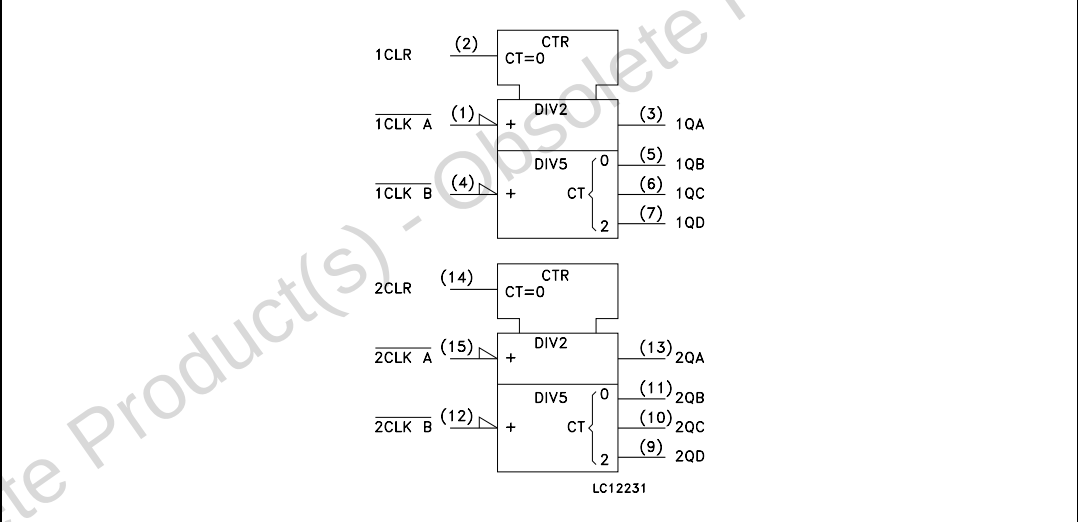


Figure 3. Logic diagram



3 Truth table

Table 2. Truth table

COUNT	Outputs							
	BCD COUNT ⁽¹⁾				BI-QUINARY ⁽²⁾			
	QD	QC	QB	QA	QA	QD	QC	QB
0	L	L	L	L	L	L	L	L
1	L	L	L	H	L	L	L	H
2	L	L	H	L	L	L	H	L
3	L	L	H	H	L	L	H	H
4	L	H	L	L	L	H	L	L
5	L	H	L	H	H	H	L	L
6	L	H	H	L	H	L	L	H
7	L	H	H	H	H	L	H	L
8	H	L	L	L	H	L	H	H
9	H	L	L	H	H	H	L	L

1. Output QA is connected to input $\overline{\text{CLOCK B}}$ for BCD count.
2. Output QD is connected to input $\overline{\text{CLOCK A}}$ for bi-quinary count.

Table 3. Truth table

Inputs			Outputs			
CLOCK A	CLOCK B	CLEAR	QA	QB	QC	QD
X	X	H	L	L	L	L
$\overline{\text{L}}$	X	L	BINARY COUNT UP			
X	$\overline{\text{L}}$	L	QUINARY COUNT UP			

4 Block and logic diagrams

Figure 4. Block diagram

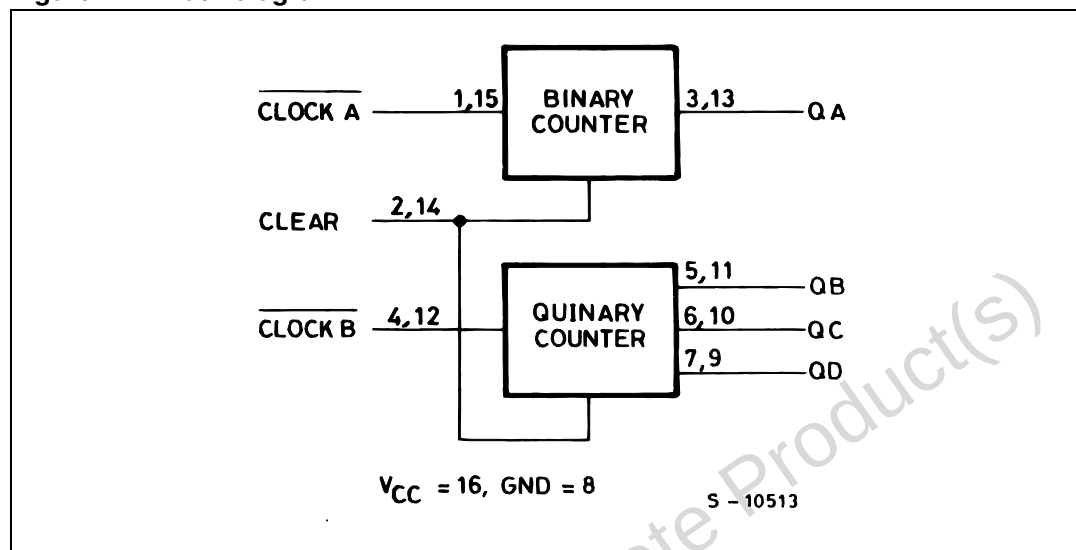
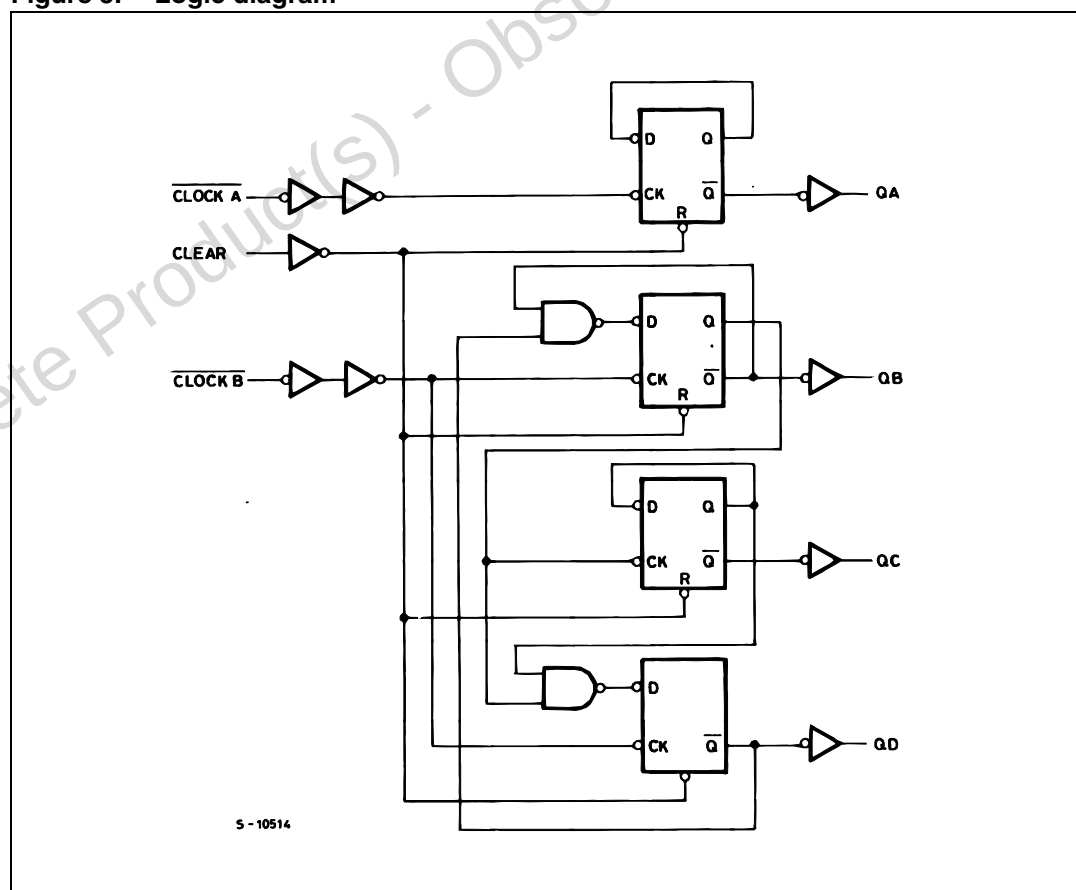


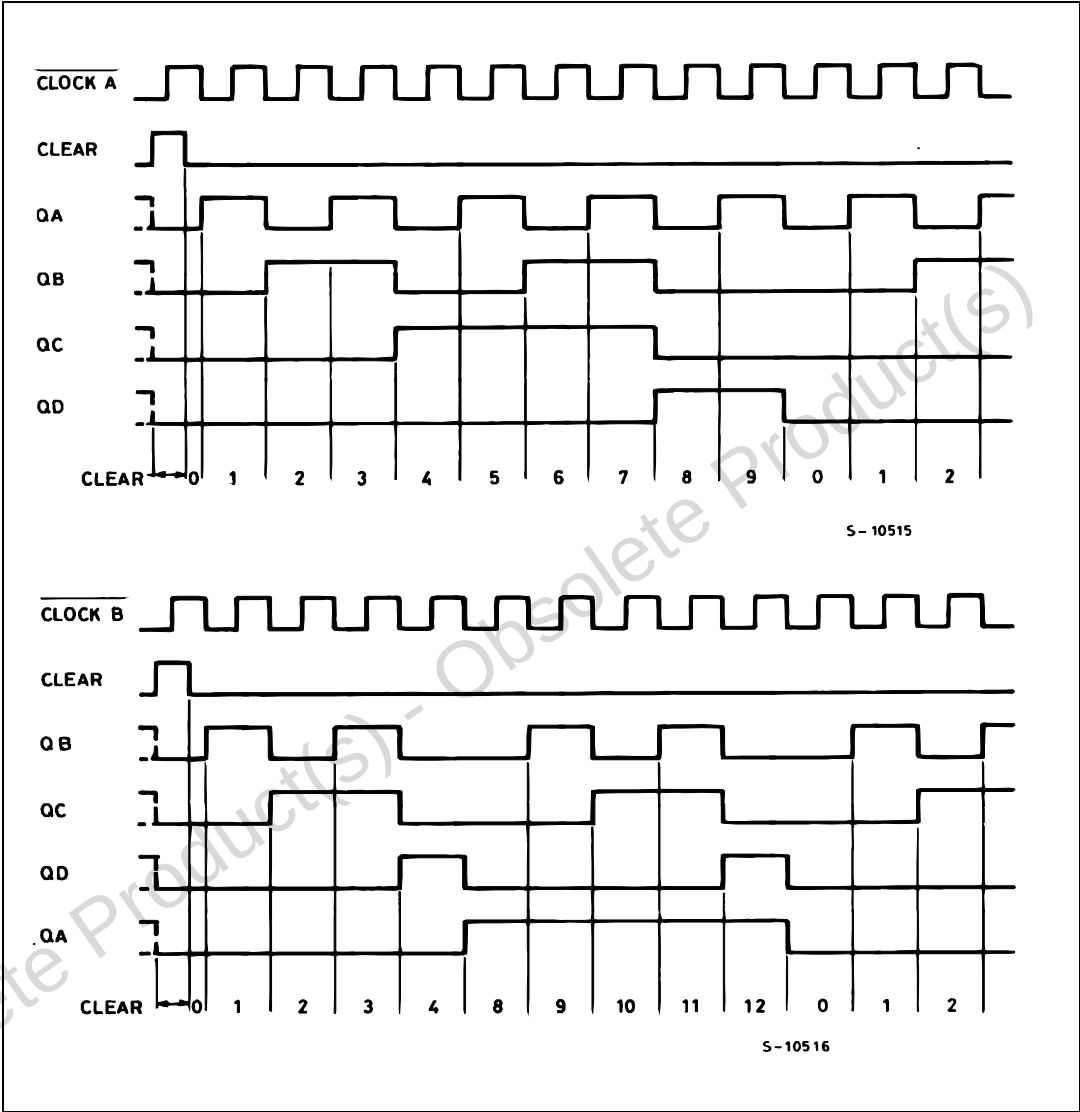
Figure 5. Logic diagram



Note: This logic diagram has not be used to estimate propagation delays

5 Timing chart

Figure 6. Timing chart



6 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to +7	V
V_I	DC input voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC output voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC input diode current	± 20	mA
I_{OK}	DC output diode current	± 20	mA
I_O	DC output current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or ground current	± 50	mA
P_D	Power dissipation	500 ⁽¹⁾	mW
T_{stg}	Storage temperature	-65 to +150	°C
T_L	Lead temperature (10 sec)	300	°C

1. 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

6.1 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter		Value	Unit
V _{CC}	Supply voltage		2 to 6	V
V _I	Input voltage		0 to V _{CC}	V
V _O	Output voltage		0 to V _{CC}	V
T _{op}	Operating temperature		-55 to 125	°C
t _r t _f	Input rise and fall time	V _{CC} = 2.0V	0 to 1000	ns
		V _{CC} = 4.5V	0 to 500	ns
		V _{CC} = 6.0V	0 to 400	ns

7 Electrical characteristics

Table 6. DC specifications

Symbol	Parameter	Test condition		Value								Unit
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C			
				Min	Typ	Max	Min	Max	Min	Max		
V _{IH}	High level input voltage	2.0		1.5			1.5		1.5		V	
		4.5		3.15			3.15		3.15			
		6.0		4.2			4.2		4.2			
V _{IL}	Low level input voltage	2.0				0.5		0.5		0.5	V	
		4.5				1.35		1.35		1.35		
		6.0				1.8		1.8		1.8		
V _{OH}	High level output voltage	2.0	I _O =-20μA	1.9	2.0		1.9		1.9		V	
		4.5	I _O =-20μA	4.4	4.5		4.4		4.4			
		6.0	I _O =-20μA	5.9	6.0		5.9		5.9			
		4.5	I _O =-4.0 mA	4.18	4.31		4.13		4.10			
		6.0	I _O =-5.2 mA	5.68	5.8		5.63		5.60			
V _{OL}	Low level output voltage	2.0	I _O =20μA		0.0	0.1		0.1		0.1	V	
		4.5	I _O =20μA		0.0	0.1		0.1		0.1		
		6.0	I _O =20μA		0.0	0.1		0.1		0.1		
		4.5	I _O =4.0 mA		0.17	0.26		0.33		0.40		
		6.0	I _O =5.2 mA		0.18	0.26		0.33		0.40		
I _I	Input leakage current	6.0	V _I = V _{CC} or GND			±0.1		±1		±1	μA	
I _{OZ}	Output leakage current	6.0	V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND			±0.5		±5		±10	μA	
I _{CC}	Quiescent supply current	6.0	V _I = V _{CC} or GND			1		10		20	μA	

Table 7. AC electrical characteristics ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Symbol	Parameter	Test condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min	Typ	Max	Min	Max	Min		Max
t _{TLH} t _{THL}	Output transition time	2.0			30	75		95		110	ns
		4.5			8	15		19		22	
		6.0			7	13		16		19	
t _{PLH} t _{PHL}	Propagation delay time (CLOCK A - QA)	2.0			42	120		150		180	ns
		4.5			14	24		30		36	
		6.0			12	20		26		31	
t _{PLH} t _{PHL}	Propagation delay time (CLOCK A - QB,QD)	2.0			45	120		150		180	ns
		4.5			15	24		30		36	
		6.0			13	20		26		31	
t _{PLH} t _{PHL}	Propagation delay time (CLOCK A - QC)	2.0	QA Connected to $\overline{CKB}$		108	280		350		420	ns
		4.5			36	56		70		84	
		6.0			31	48		60		71	
t _{PLH} t _{PHL}	Propagation delay time (CLOCK B - QC)	2.0			72	185		230		280	ns
		4.5			24	37		46		56	
		6.0			20	31		39		48	
t _{PHL}	Propagation delay time (CLEAR - Qn)	2.0			45	125		155		190	ns
		4.5			15	25		31		38	
		6.0			13	21		26		32	
f _{MAX}	Maximum clock frequency (CLOCK A - QA)	2.0		8.4	17		6.8		5.6		MHz
		4.5		42	65		34		28		
		6.0		50	79		40		33		
f _{MAX}	Maximum clock frequency (CLOCK B - QB)	2.0		8.4	17		6.8		5.6		MHz
		4.5		42	67		34		28		
		6.0		50	79		40		33		
t _{W(H)} t _{W(L)}	Minimum pulse width (CLOCK)	2.0			24	75		95		110	ns
		4.5			6	15		19		22	
		6.0			5	13		16		19	
t _{W(H)}	Minimum pulse width (CLEAR)	2.0			24	75		95		110	ns
		4.5			6	15		19		22	
		6.0			5	13		16		19	
t _{REM}	Minimum removal time	2.0				25		30		35	ns
		4.5				5		6		7	
		6.0				5		5		6	

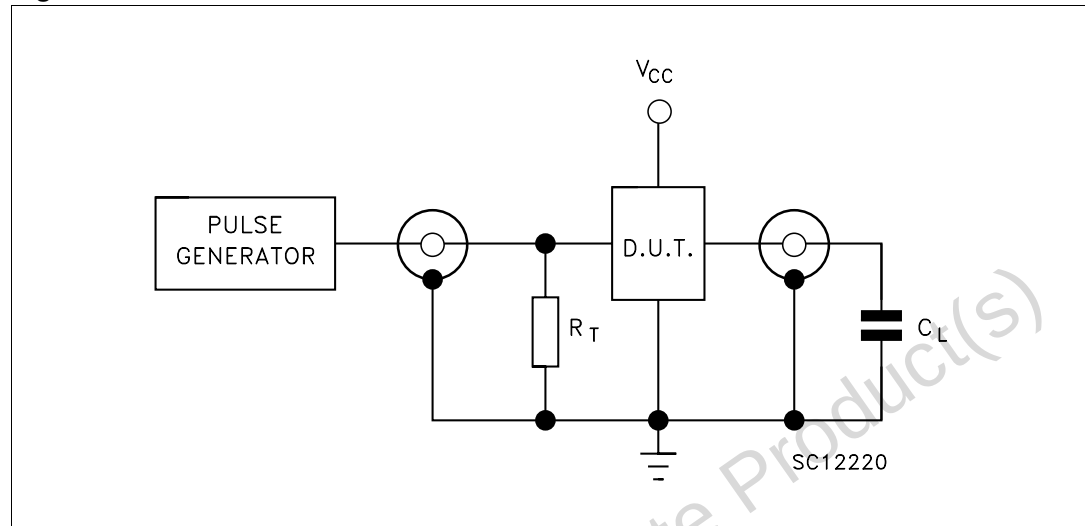
Table 8. Capacitive characteristics

Symbol	Parameter	Test condition		Value							Unit
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min	Typ	Max	Min	Max	Min	Max	
C _{IN}	Input capacitance				5	10		10		10	pF
C _{PD}	Power dissipation capacitance (1)				84						pF

1. C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

8 Test circuit

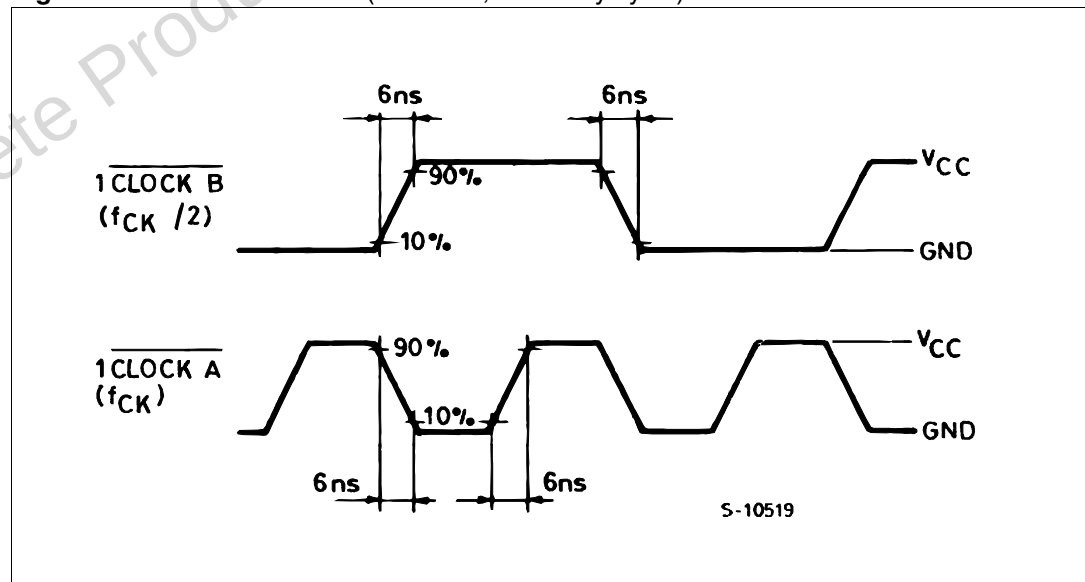
Figure 7. Test circuit



Note: $C_L = 50\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

9 Waveforms

Figure 8. Clock waveform ($f = 1\text{MHz}$; 50% duty cycle)



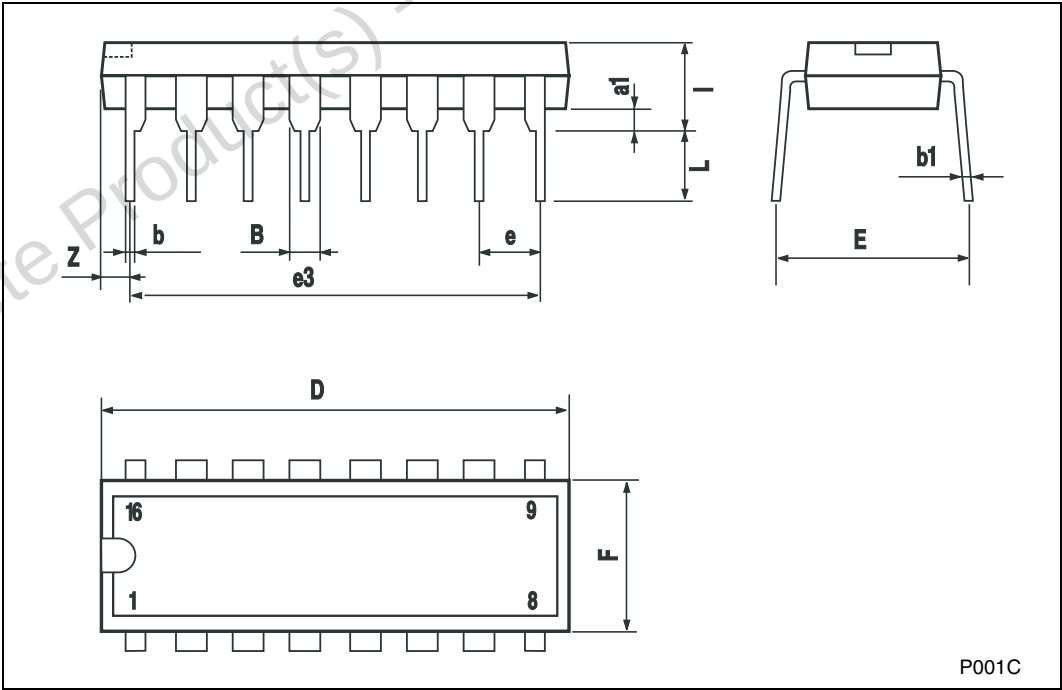
10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Obsolete Product(s) - Obsolete Product(s)

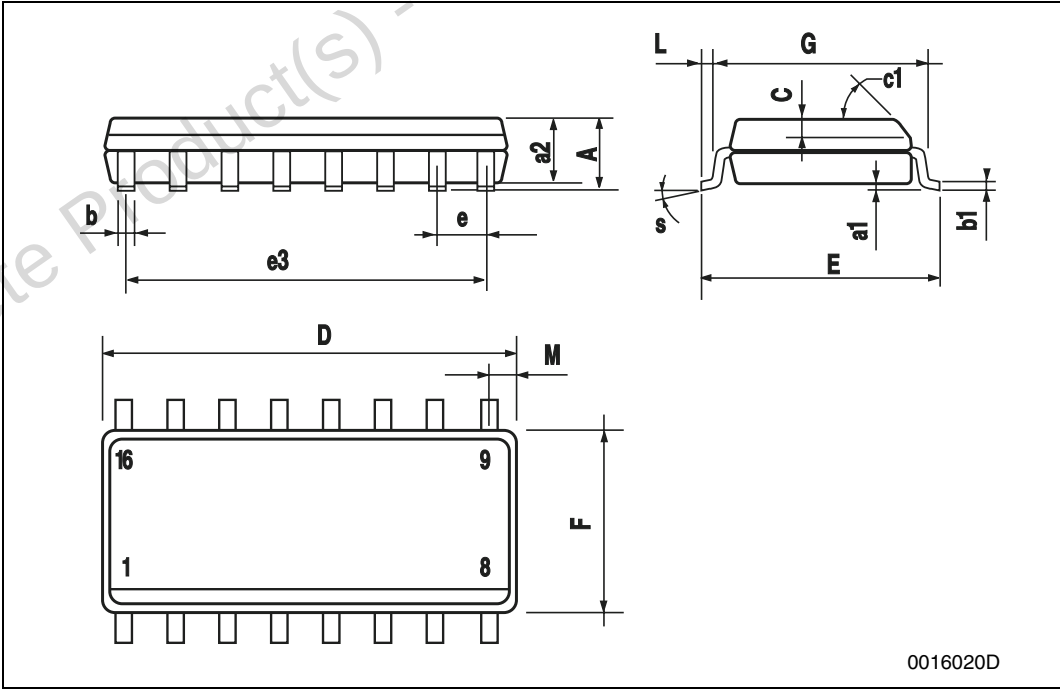
Plastic DIP-16 (0.25) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



SO-16 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.004		0.010
a2			1.64			0.063
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



11 Revision history

Table 9. Revision history

Date	Revision	Changes
07-Aug-2001	1	First Release
21-Jul-2006	2	New template, deleted TSSOP16 package information

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2006 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com