



74LVC07A

Hex buffer with open-drain outputs

Rev. 10 — 2 May 2025

Product data sheet

1. General description

The 74LVC07A is a hex buffer with open-drain outputs. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

2. Features and benefits

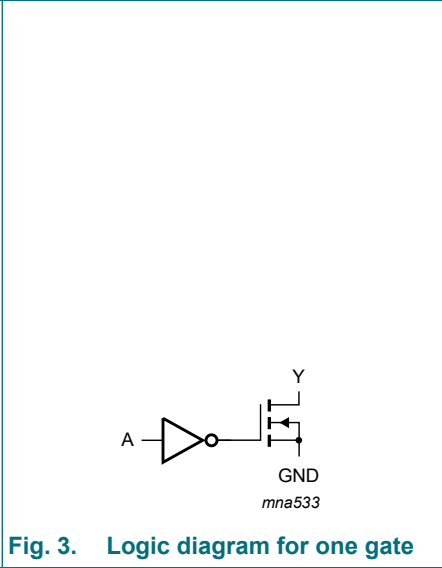
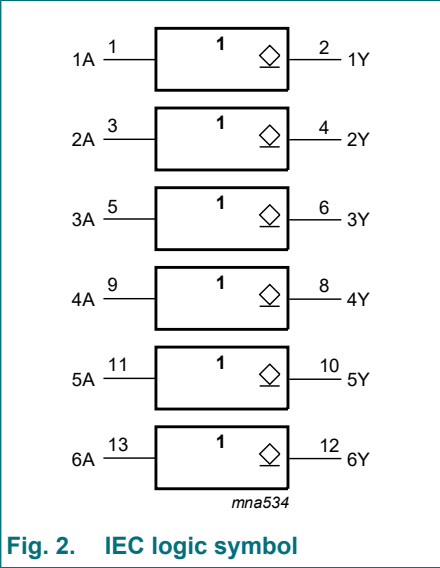
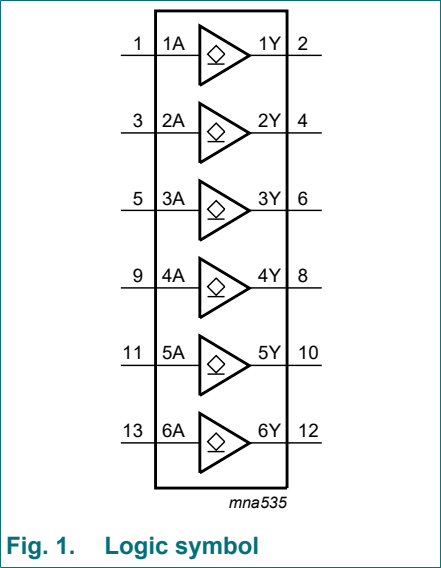
- 5 V tolerant inputs and outputs (open-drain) for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Overvoltage tolerant inputs to 5.5 V
- Complies with JEDEC standard:
 - JESD8-7A (1.65 V to 1.95 V)
 - JESD8-5A (2.3 V to 2.7 V)
 - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

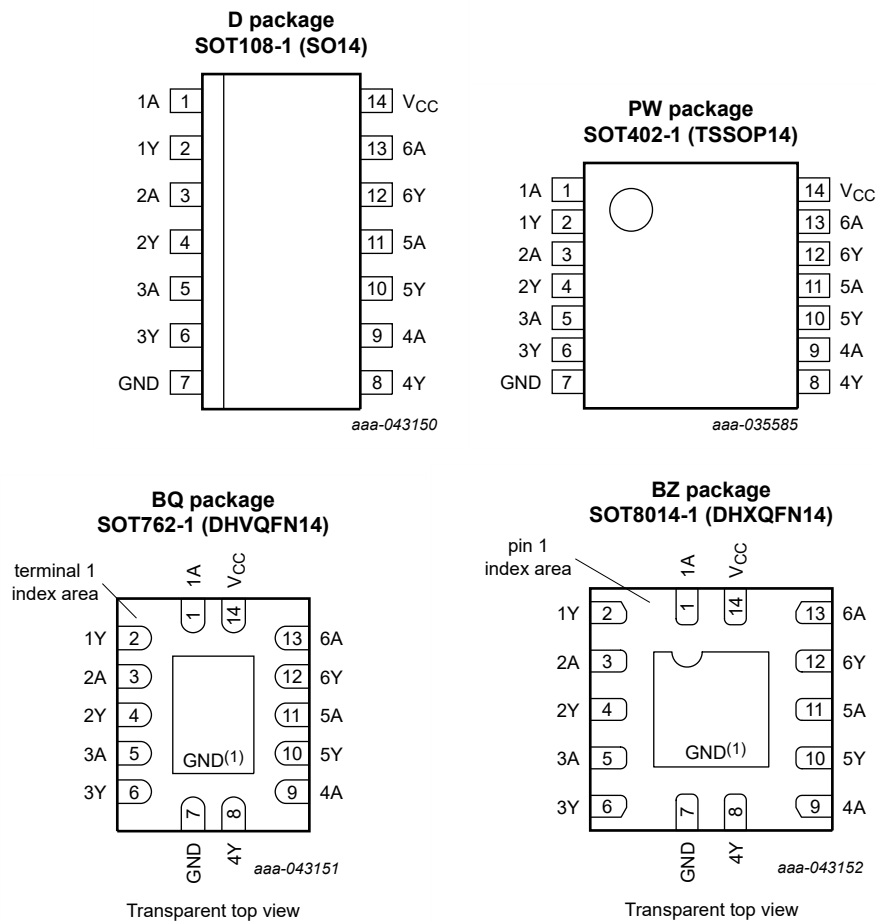
Type number	Package			
	Temperature range	Name	Description	Version
74LVC07AD	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVC07APW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVC07ABQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1
74LVC07ABZ	-40 °C to +125 °C	DHXQFN14	plastic, leadless dual in-line compatible thermal enhanced extreme thin quad flat package; no leads; 14 terminals; 0.4 mm pitch; body 2 mm × 2 mm × 0.48 mm	SOT8014-1

4. Functional diagram



5. Pinning information

5.1. Pinning



(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state

Input	Output
nA	nY
L	L
H	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
V _I	input voltage	[1]	-0.5	+6.5	V
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
V _O	output voltage	active mode [2]	-0.5	+6.5	V
		high-impedance mode [2]	-0.5	+6.5	V
I _O	output current	V _O = 0 V to V _{CC}	-	50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C			
		SOT108-1 (SO14) [3] SOT402-1 (TSSOP14) SOT762-1 (DHVQFN14)	-	500	mW
		SOT8014-1 (DHXQFN14) [4]	-	250	mW
T _{stg}	storage temperature		-65	+150	°C

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.
[2] The output voltage ratings may be exceeded if the output current ratings are observed.
[3] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.
For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.
For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.
[4] For SOT8014-1 (DHXQFN14) package: P_{tot} derates linearly with 8.7 mW/K above 121 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		1.65	-	5.5	V
		functional	1.2	-	-	V
V _I	input voltage		0	-	5.5	V
V _O	output voltage	active mode	0	-	5.5	V
		high-impedance mode	0	-	5.5	V
T _{amb}	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
		V _{CC} = 2.7 V to 5.5 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V _{CC} = 1.65 V to 1.95 V	0.65V _{CC}	-	-	0.65V _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7V _{CC}	-	-	0.7V _{CC}	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V _{CC} = 1.65 V to 1.95 V	-	-	0.35V _{CC}	-	0.35V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.30V _{CC}	-	0.30V _{CC}	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 100 μA; V _{CC} = 1.65 V to 5.5 V	-	-	0.20	-	0.3	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.6	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.3	-	0.75	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.8	V
		I _O = 32 mA; V _{CC} = 4.5 V	-	-	0.55	-	0.8	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 1.65 V to 5.5 V	-	±0.1	±5	-	±20	μA
I _{OZ}	OFF-state output current	V _I = V _{IH} ; V _O = 5.5 V or GND; V _{CC} = 1.65 V to 5.5 V	-	±0.1	±10	-	±20	μA
I _{OFF}	power-off leakage current	V _I or V _O = 5.5 V; V _{CC} = 0 V	-	±0.1	±10	-	±20	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	0.1	10	-	40	μA

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC} - 0.6\text{ V}$; $I_O = 0\text{ A}$; $V_{CC} = 2.7\text{ V to }5.5\text{ V}$	-	5	500	-	5000	μA
C_I	input capacitance	$V_{CC} = 0\text{ V to }5.5\text{ V}$; $V_I = \text{GND to }V_{CC}$	-	5.0	-	-	-	pF

[1] All typical values are measured at $V_{CC} = 3.3\text{ V}$ (unless stated otherwise) and $T_{amb} = 25\text{ °C}$.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 5.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t_{PZL}	OFF-state to LOW propagation delay	nA to nY; see Fig. 4						
		$V_{CC} = 1.2\text{ V}$	-	8.0	-	-	-	ns
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	0.5	1.7	5.5	0.5	6.5	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.5	1.2	2.8	0.5	3.5	ns
		$V_{CC} = 2.7\text{ V}$	0.5	1.8	3.3	0.5	4.5	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	0.5	1.2	3.6	0.5	4.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	0.5	1.6	2.6	0.5	3.5	ns
t_{PLZ}	LOW to OFF-state propagation delay	nA to nY; see Fig. 4						
		$V_{CC} = 1.2\text{ V}$	-	10	-	-	-	ns
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	0.5	3.0	5.5	0.5	6.5	ns
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.5	1.7	2.8	0.5	3.5	ns
		$V_{CC} = 2.7\text{ V}$	0.5	2.1	3.3	0.5	4.5	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	0.5	2.5	3.6	0.5	4.5	ns
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	0.5	1.6	2.6	0.5	3.5	ns
C_{PD}	power dissipation capacitance	per buffer; $V_I = \text{GND to }V_{CC}$ [2]						
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	6.5	-	-	-	pF
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	6.9	-	-	-	pF
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	7.2	-	-	-	pF

[1] Typical values are measured at $T_{amb} = 25\text{ °C}$ and $V_{CC} = 1.2\text{ V}, 1.8\text{ V}, 2.5\text{ V}, 2.7\text{ V}, 3.3\text{ V}$ and 5.0 V respectively.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz

C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

10.1. Waveforms and test circuit

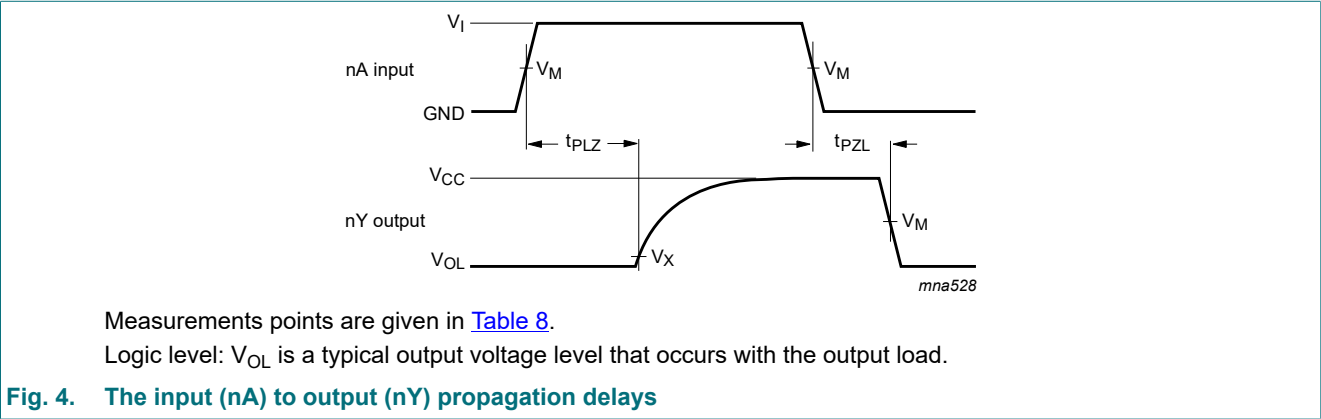


Table 8. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_X
$< 2.7\text{ V}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15\text{ V}$
$\geq 2.7\text{ V to } 3.6\text{ V}$	1.5 V	$V_{OL} + 0.3\text{ V}$
$\geq 4.5\text{ V to } 5.5\text{ V}$	$0.5 \times V_{CC}$	$V_{OL} + 0.3\text{ V}$

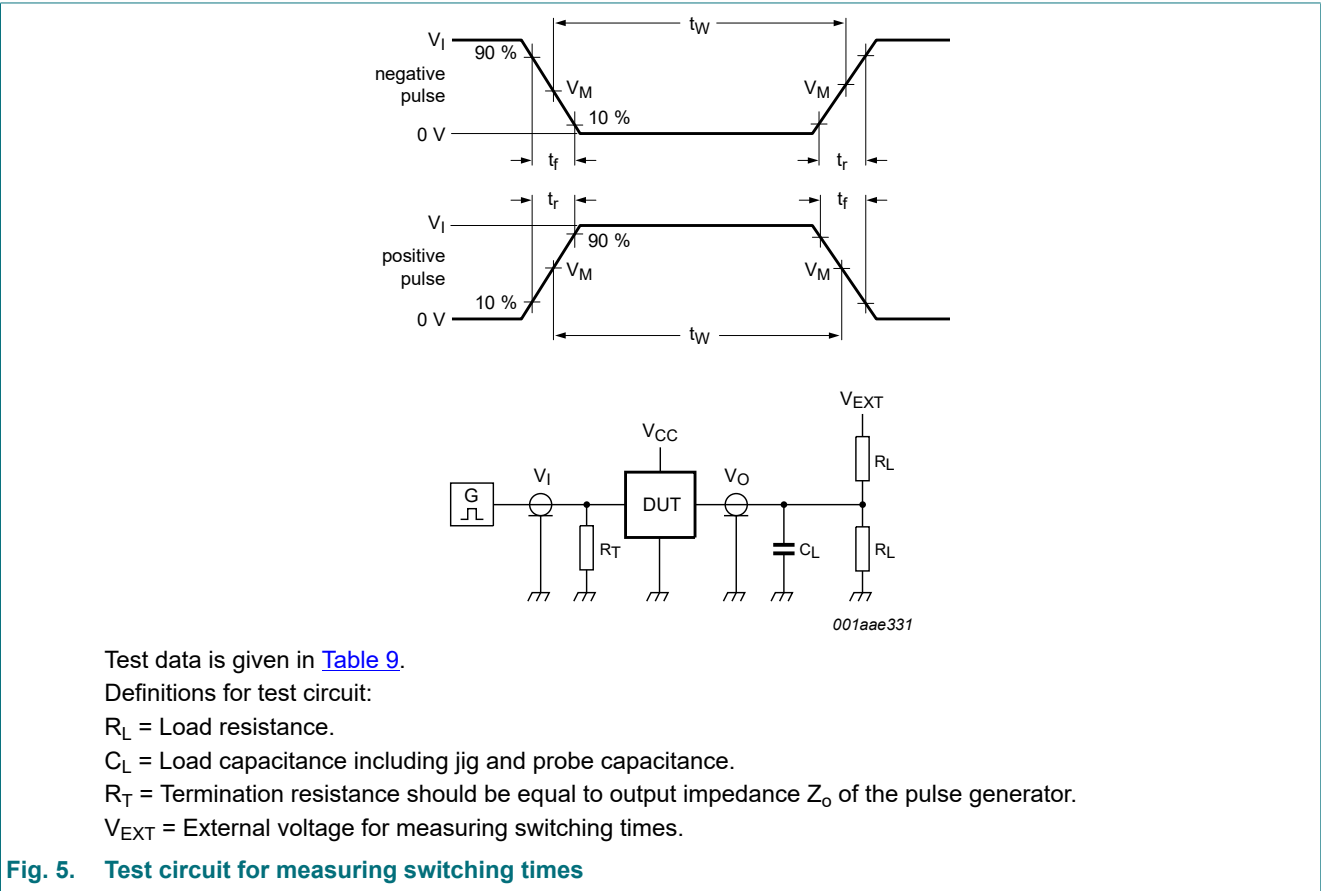


Table 9. Test data

Supply voltage	Input		Load		V _{EXT}		
	V _I	t _r , t _f	C _L	R _L	t _{PLH} , t _{PHL}	t _{PLZ} , t _{PZL}	t _{PHZ} , t _{PZH}
1.2 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V _{CC}	GND
1.65 V to 1.95 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V _{CC}	GND
2.3 V to 2.7 V	V _{CC}	≤ 2 ns	30 pF	500 Ω	open	2 × V _{CC}	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V _{CC}	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	2 × V _{CC}	GND
4.5 V to 5.5 V	V _{CC}	≤ 2.5 ns	50 pF	500 Ω	open	2 × V _{CC}	GND

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

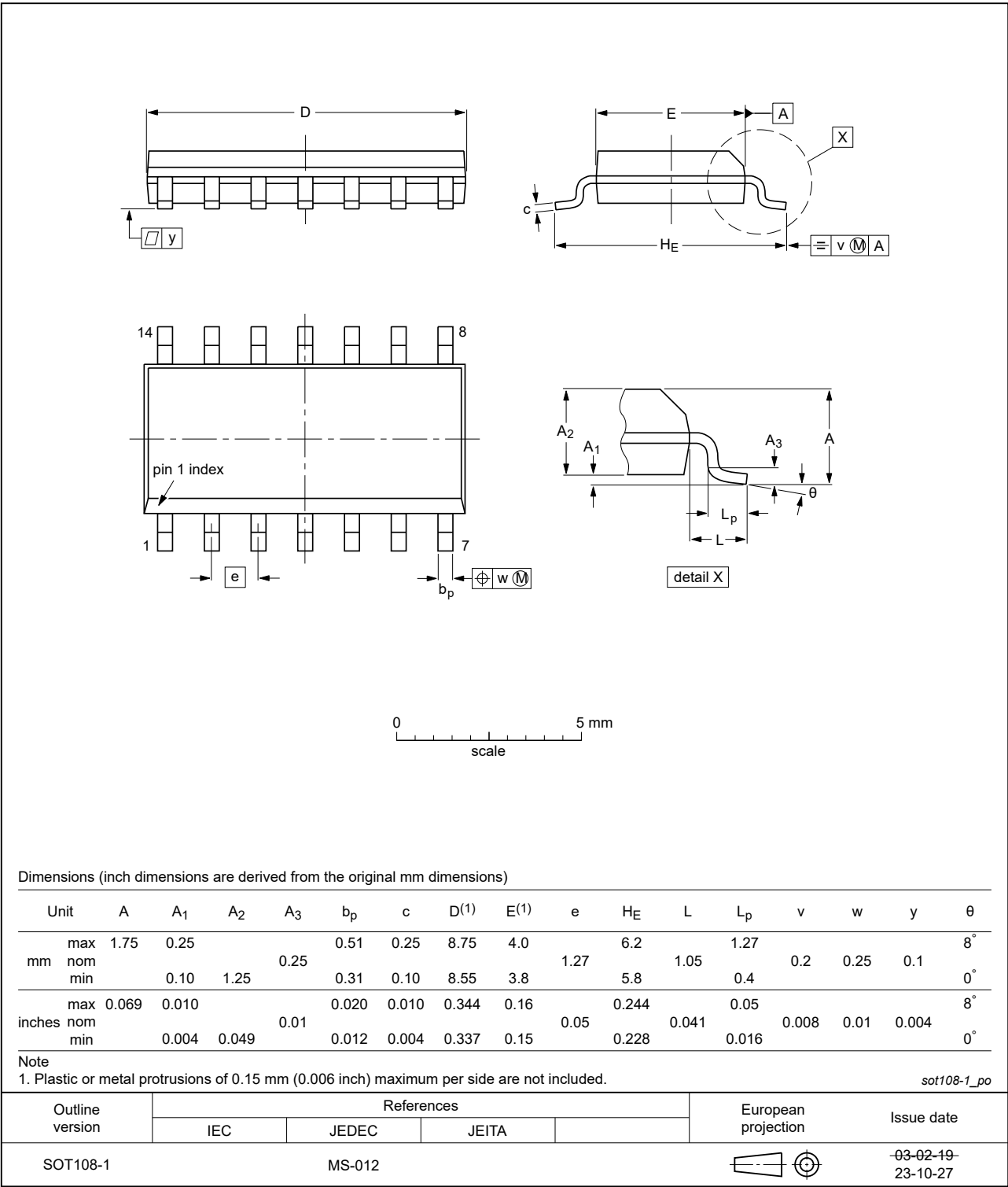


Fig. 6. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



Fig. 7. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



Fig. 8. Package outline SOT762-1 (DHVQFN14)

DHXQFN14: plastic, leadless dual in-line compatible thermal enhanced extreme thin quad flat package;
no leads; 14 terminals; 0.4 mm pitch; body 2 mm x 2 mm x 0.48 mm

SOT8014-1

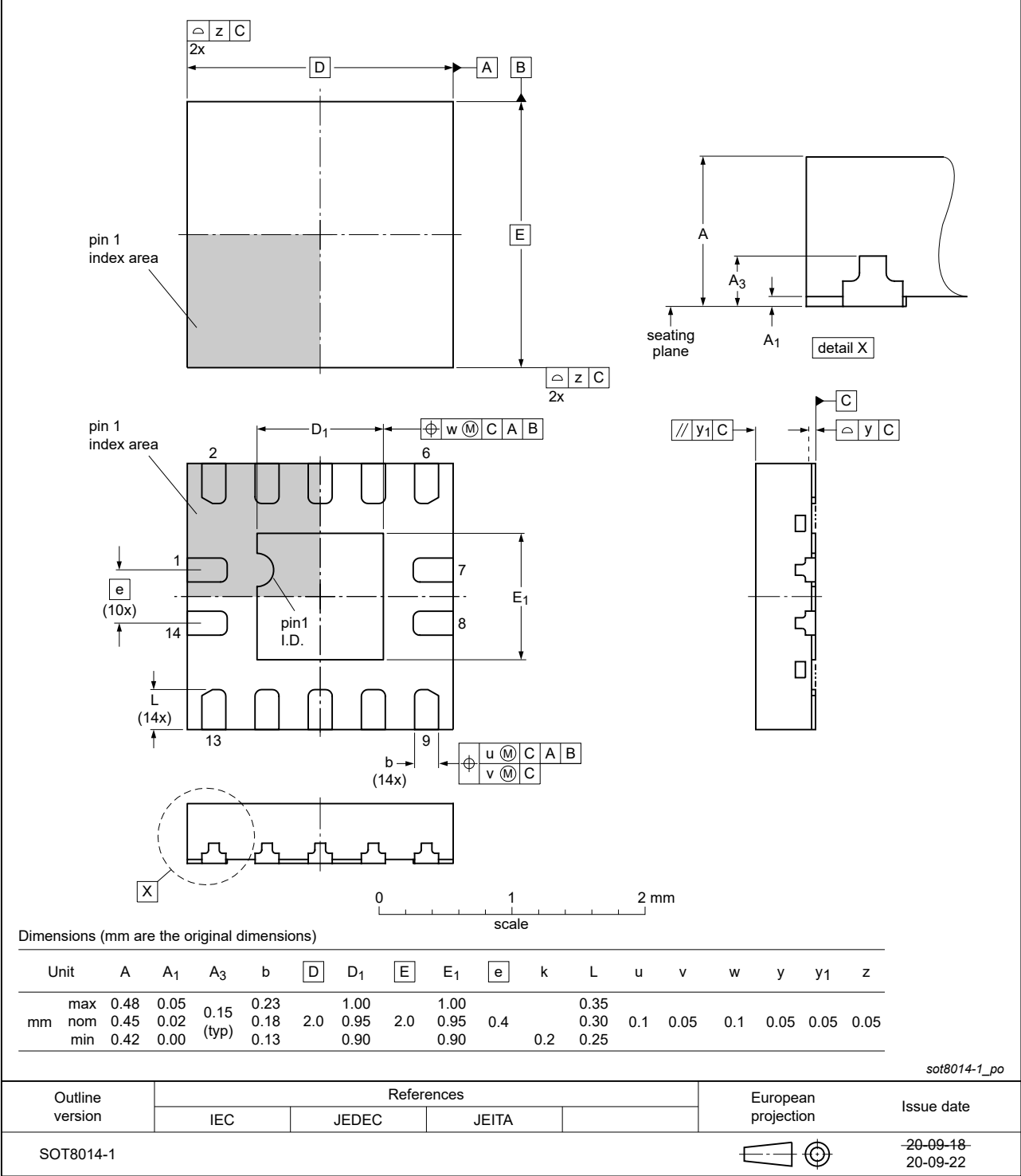


Fig. 9. Package outline SOT8014-1 (DHXQFN14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC07A v.10	20250502	Product data sheet	-	74LVC07A v.9
Modifications:	• Type number 74LVC07ABZ (SOT8014-1/DHXQFN14) added.			
74LVC07A v.9	20240208	Product data sheet	-	74LVC07A v.8
Modifications:	• Fig. 6 , Fig. 7 : Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.			
74LVC07A v.8	20230802	Product data sheet	-	74LVC07A v.7
Modifications:	• Section 2 : ESD specification updated according to the latest JEDEC standard.			
74LVC07A v.7	20200803	Product data sheet	-	74LVC07A v.6
Modifications:	• Section 1 and Section 2 updated. • Table 4 : Derating values for P _{tot} total power dissipation updated.			
74LVC07A v.6	20181214	Product data sheet	-	74LVC07A v.5
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Table 5 : Maximum output voltage (active mode) changed from V _{CC} to 5.5 V			
74LVC07A v.5	20111027	Product data sheet	-	74LVC07A v.4
Modifications:	• Table 7 : values added for lower voltage ranges.			
74LVC07A v.4	20110810	Product data sheet	-	74LVC07A v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 4 , Table 5 , Table 6 and Table 7 : values added for lower voltage ranges.			
74LVC07A v.3	20031111	Product specification	-	74LVC07A v.2
74LVC07A v.2	20030225	Product specification	-	74LVC07A v.1
74LVC07A v.1	20000307	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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- [2] The term 'short data sheet' is explained in section "Definitions".
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