TDA8579T

Dual common-mode rejection differential line receiver

Rev. 4 — 23 September 2013 Product data sheet

1. General description

The TDA8579T is a two channel differential amplifier with 0 dB gain and low distortion. The device has been primarily developed for car radio applications where long connections between signal sources and amplifiers (or boosters) are necessary and where ground noise has to be eliminated. The device is intended to be used to receive line inputs in audio applications that require a high level of common-mode rejection. The device is contained in an 8-pin Small Outline (SO) package.

2. Features and benefits

- Excellent common-mode rejection, up to high frequencies
- Elimination of source resistance dependency in the common-mode rejection
- Few external components
- High supply voltage ripple rejection
- Low noise
- Low distortion
- All pins protected against electrostatic discharge
- AC and DC short-circuit safe to ground and V_{CC}
- Fast DC settling

3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		5.0	8.5	18	V
I_{CC}	supply current	V_{CC} = 8.5 V	-	11	14	mA
G_V	voltage gain		–0.5	0	+0.5	dB
SVRR	supply voltage ripple rejection		55	60	-	dB
V_{no}	noise output voltage		-	3.7	5.0	μV
$\|Z_i\|$	input impedance		100	240	-	kΩ
CMRR	common-mode rejection ratio	R_S = 0 Ω	-	80	-	dB

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA8579T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

5. Block diagram

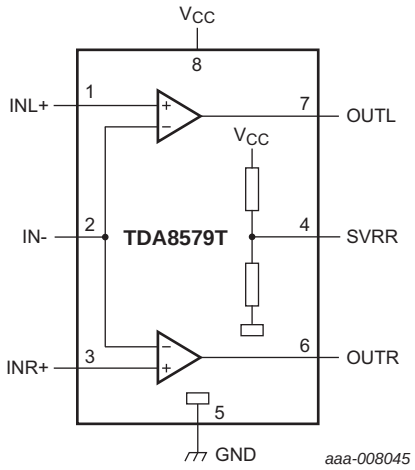


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

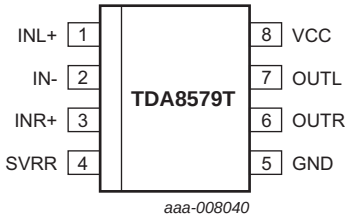


Fig 2. Pin configuration

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
INL+	1	positive input left
IN–	2	common negative input
INR+	3	positive input right
SVRR	4	half supply voltage
GND	5	ground
OUTR	6	output right
OUTL	7	output left
V_{CC}	8	supply voltage

7. Functional description

The TDA8579T contains two identical differential amplifiers with a voltage gain of 0 dB. The device is intended to receive line input signals for audio applications. The TDA8579T has a very high level of common-mode rejection and thus eliminates ground noise. The common-mode rejection remains constant up to high frequencies (the amplifier gain is fixed at 0 dB). The inputs have a high input impedance. The output stage is a class AB stage with a low output impedance. For a large common-mode rejection, also at low frequencies, an electrolytic capacitor connected to the negative input is advised. Because the input impedance is relatively high, this results in a large settling time of the DC input voltage. Therefore a quick-charge circuit is included to charge the input capacitor within 0.2 seconds.

All input and output pins are protected against high electrostatic discharge conditions (4000 V, 150 pF, 150 Ω).

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages and currents are referenced to GND unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-	18	V
I_{ORM}	repetitive peak output current		-	40	mA
V_{sc}	AC and DC short-circuit safe voltage		-	18	V
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	ambient temperature		−40	+85	°C
T_j	maximum junction temperature		-	150	°C

9. Thermal characteristics

Table 5. Thermal characteristics

According to IEC 60747-1.

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	160	K/W

10. Characteristics

Table 6. Electrical characteristics

V_{CC} = 8.5 V; T_{amb} = 25 °C; test circuit (see Figure 3); unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage			5.0	8.5	18	V
I_{CC}	supply current			-	11	14	mA
V_O	output voltage		[1]	-	4.3	-	V
t_{set}	DC input voltage settling time			-	0.2	-	s
G_v	voltage gain			−0.5	0	+0.5	dB
α_{cs}	channel separation	R_s = 5 kΩ		70	80	-	dB
$\lvert\Delta G_v\rvert$	channel unbalance			-	-	0.5	dB
f_L	LOW frequency roll-off	−1 dB	[2]	20	-	-	Hz
f_H	HIGH frequency roll-off	−1 dB		20	-	-	kHz
$\lvert Z_i\rvert$	input impedance			100	240	-	kΩ
$\lvert Z_o\rvert$	output impedance			-	-	10	Ω
$V_{i(max)}$	maximum input voltage	THD = 1 %		-	2.0	-	V
V_{no}	noise output voltage	R_s = 0 Ω	[3]	-	3.7	5.0	μV
$V_{CM(rms)}$	common-mode input voltage (RMS value)			-	-	1.0	V
CMRR	common-mode rejection ratio	R_s = 5 kΩ		66	70	-	dB
		R_s = 0 Ω	[4]	-	80	-	dB
SVRR	supply voltage ripple rejection		[5]	55	65	-	dB
			[6]	-	60	-	dB
THD	total harmonic distortion	V_i = 1 V;		-	0.02	-	%
		V_i = 1 V; f = 20 Hz to 20 kHz		-	-	0.1	%
THD_{max}	total harmonic distortion at maximum output current	V_i = 1 V; R_L = 150 Ω		-	-	1	%

[1] The DC output voltage with respect to ground is approximately $0.5V_{CC}$.

[2] The input coupling capacitors set the frequency response externally.

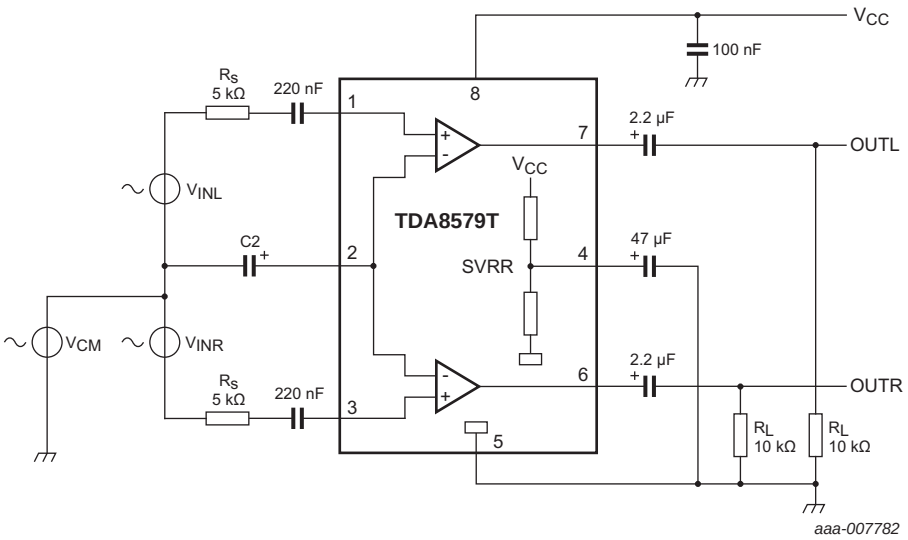
[3] The noise output voltage is measured in a bandwidth of 20 Hz to 20 kHz (unweighted).

[4] The common-mode rejection ratio is measured at the output with a voltage source 1 V (RMS) in accordance with the test circuit (see Figure 3). V_{INL} and V_{INR} are short-circuited. Frequencies are between 100 Hz and 100 kHz.

[5] The ripple rejection is measured at the output, with R_s = 2 kΩ, f = 1 kHz and a ripple amplitude of 2 V (p-p).

[6] The ripple rejection is measured at the output. R_s = 0 Ω to 2 kΩ, f = 100 Hz to 20 kHz and a maximum ripple amplitude of 2 V (p-p).

11. Application information



C2 = nominal 22 µF

Fig 3. Test and application circuit

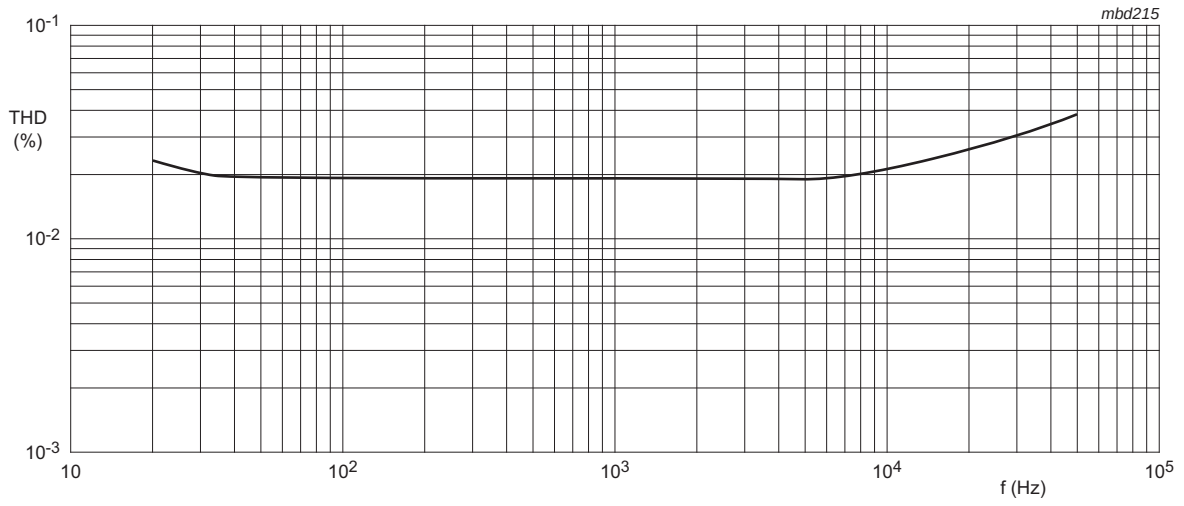
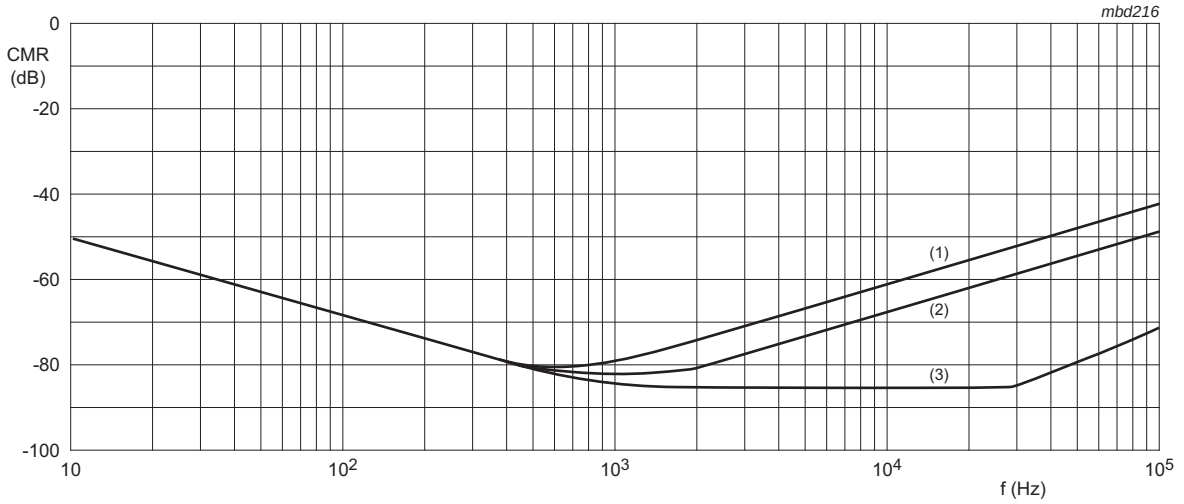


Fig 4. Total harmonic distortion as a function of frequency; V_i = 1 V (RMS)



(1) R_s = 5 kΩ

(2) R_s = 2 kΩ

(3) R_s = 0 kΩ

Fig 5. Common-mode rejection ratio as a function of frequency; V_{CM} = 1 V (RMS)

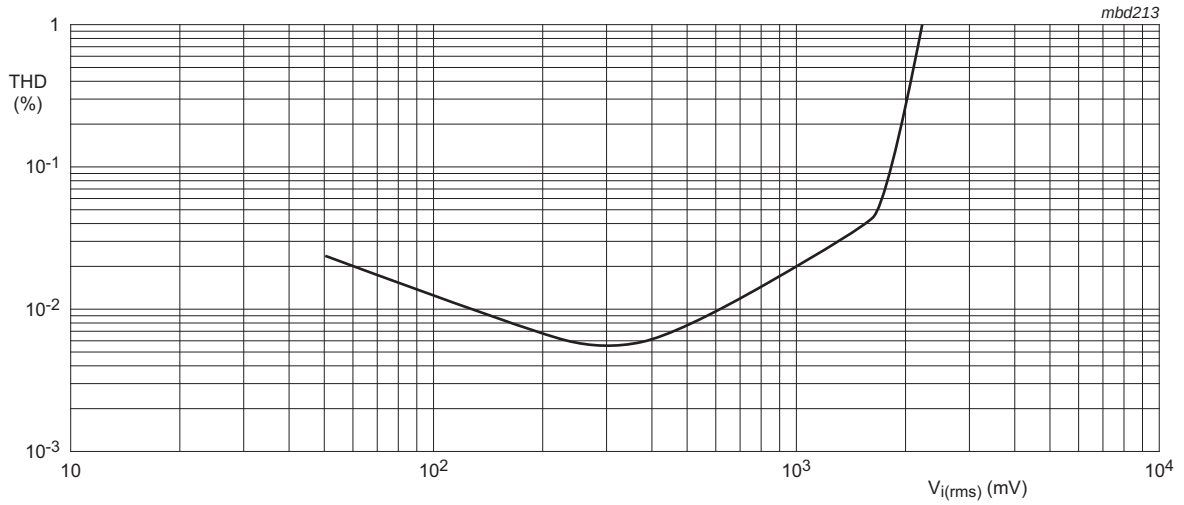


Fig 6. Total harmonic distortion as a function of input voltage; f = 1 kHz

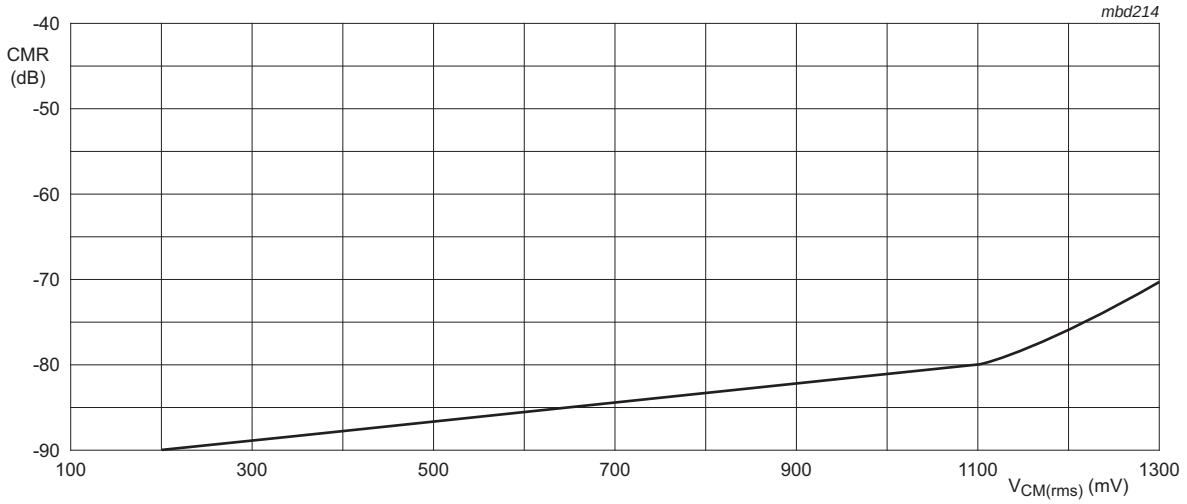
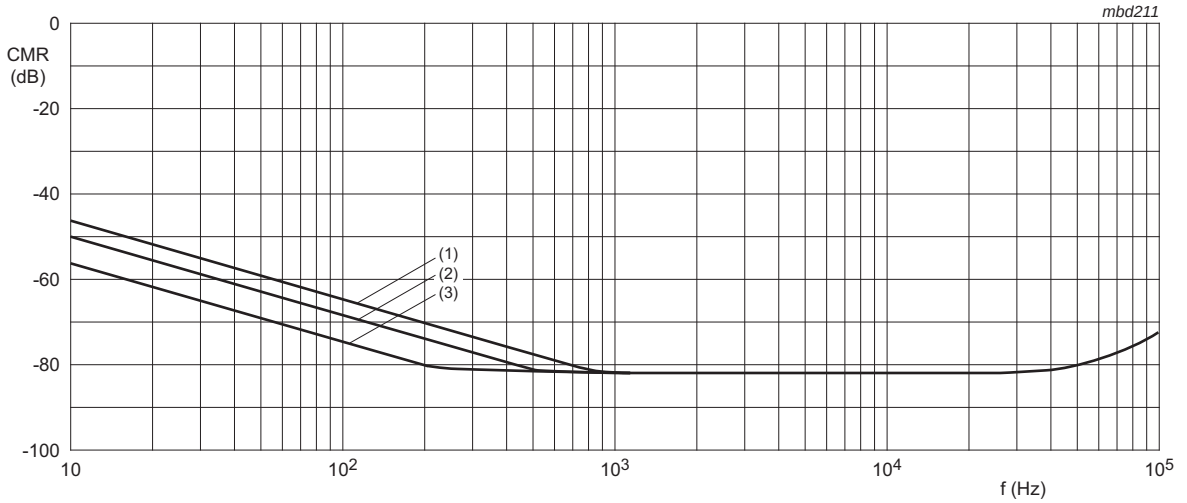


Fig 7. Common-mode rejection ratio as a function of common-mode input voltage; f = 1 kHz, R_s = 0 Ω



(1) C2 = 22 μF

(2) C2 = 47 μF

(3) C2 = 100 μF

Fig 8. Common-mode rejection ratio as a function of frequency; V_{CM} = 1 V (RMS)

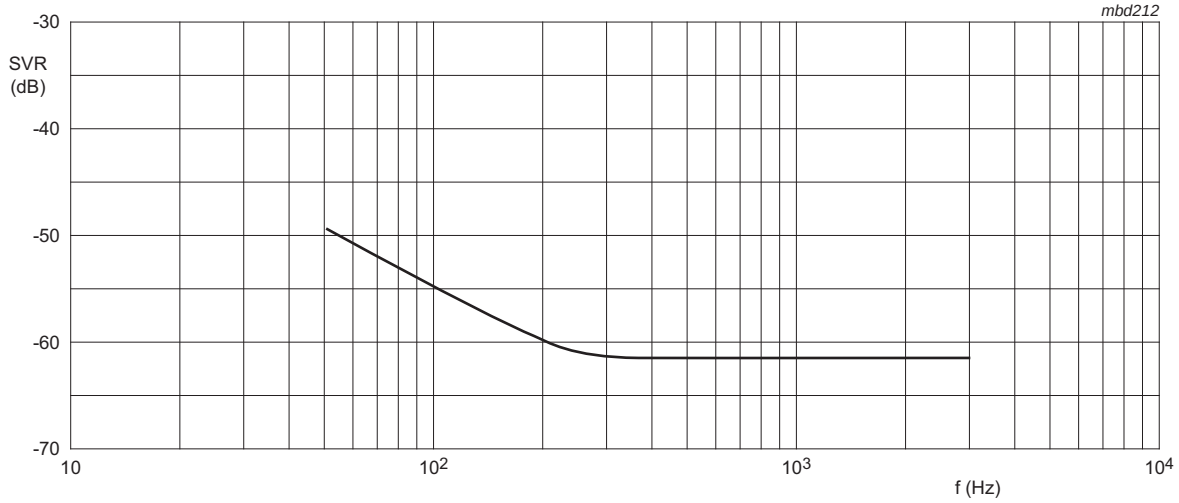
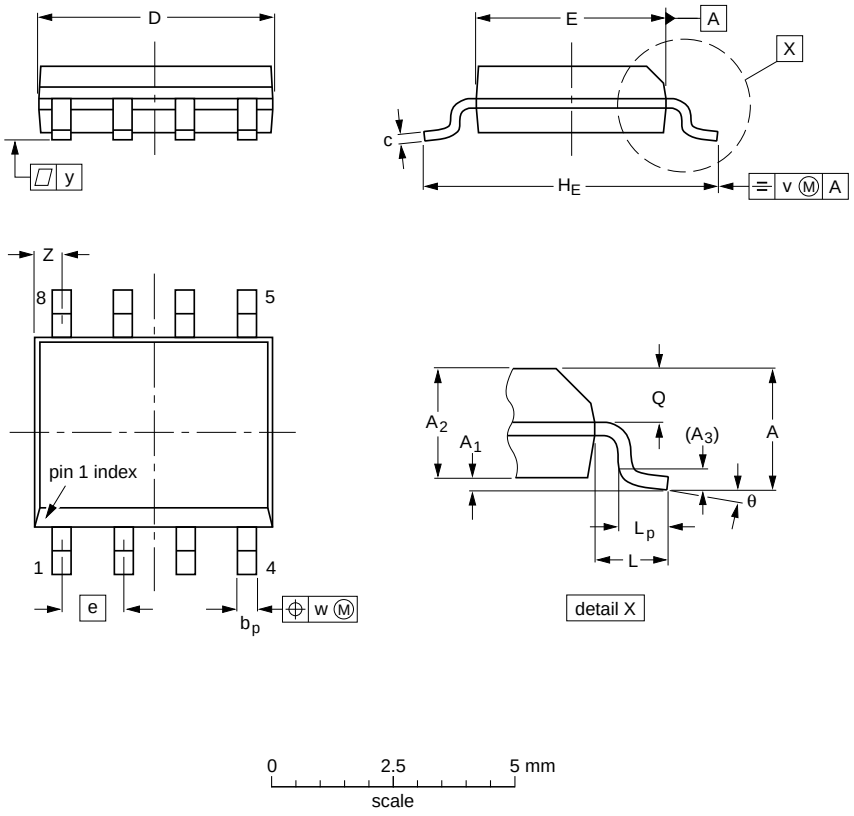


Fig 9. Supply voltage ripple rejection as a function of frequency; V_{ripple} = 2 V (p-p), R_s = 2 kΩ

12. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 10. Package outline SOT96-1 (SO8)

13. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 11) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 7 and 8

Table 7. SnPb eutectic process (from J-STD-020D)

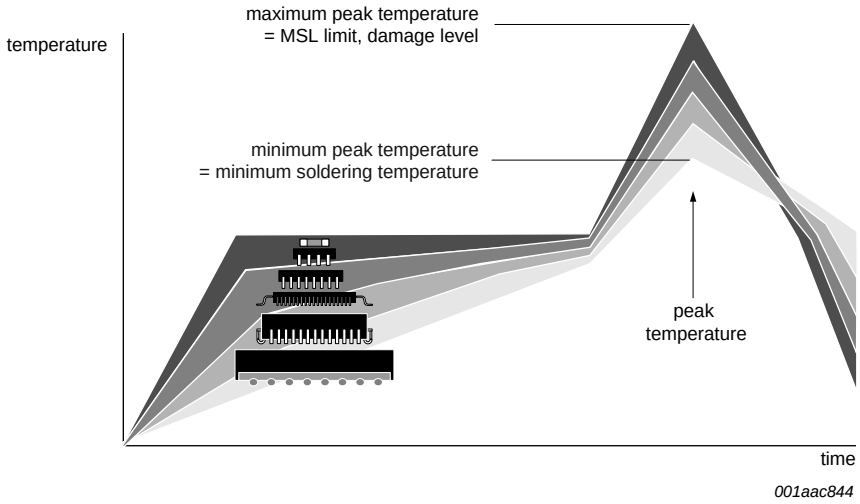
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 8. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 11.



MSL: Moisture Sensitivity Level

Fig 11. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

15. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA8579T v.4	20130923	Product data sheet	-	TDA8579 v.3
Modifications:	• Security status changed from company confidential to company public.			
TDA8579T v.3	20130606	Product data sheet	-	TDA8579 v.2
Modifications:	• The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
TDA8579 v.2	19951215	Product data sheet	-	TDA8579 v.1
TDA8579 v.1	19940125	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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