



QUICKSWITCH® PRODUCTS 2.5V / 3.3V QUAD ACTIVE LOW, HIGH BANDWIDTH BUS SWITCH

IDTQS3VH125

FEATURES:

- **N channel FET switches with no parasitic diode to Vcc**
 - Isolation under power-off conditions
 - No DC path to Vcc or GND
 - 5V tolerant in OFF and ON state
- **5V tolerant I/Os**
- **Low RON - 4Ω typical**
- **Flat RON characteristics over operating range**
- **Rail-to-rail switching 0 - 5V**
- **Bidirectional dataflow with near-zero delay: no added ground bounce**
- **Excellent RON matching between channels**
- **Vcc operation: 2.3V to 3.6V**
- **High bandwidth - up to 500MHz**
- **LVTTL-compatible control Inputs**
- **Undershoot Clamp Diodes on all switch and control Inputs**
- **Low I/O capacitance, 4pF typical**
- **Available in QSOP, TSSOP, and SOIC packages**

APPLICATIONS:

- Hot-swapping
- 10/100 Base-T, Ethernet LAN switch
- Low distortion analog switch
- Replaces mechanical relay
- ATM 25/155 switching

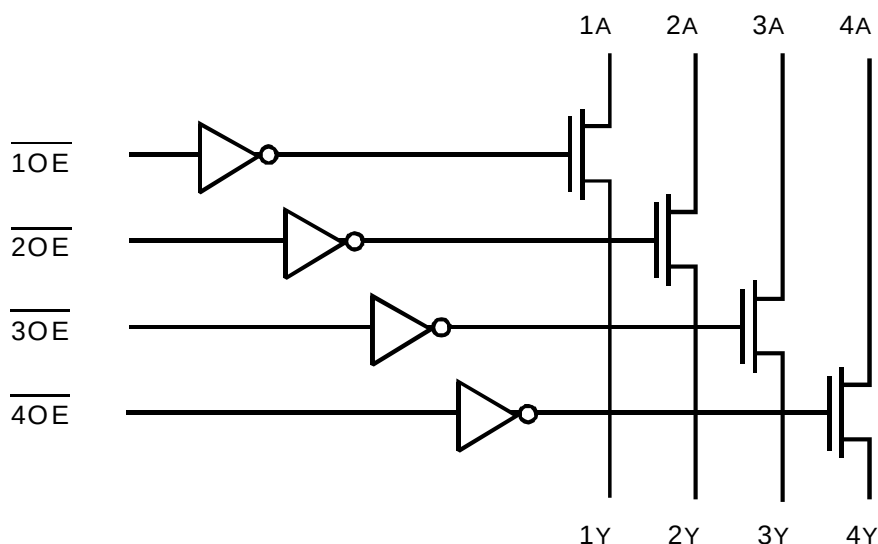
DESCRIPTION:

The QS3VH125 is a high bandwidth, Quad bus switch. The QS3VH125 has very low ON resistance, resulting in under 250ps propagation delay through the switch. The switches can be turned ON under the control of individual LVTTL-compatible active low Output Enable signals for bidirectional data flow with no added delay or ground bounce. In the ON state, the switches can pass signals up to 5V. In the OFF state, the switches offer very high impedance at the terminals.

The combination of near-zero propagation delay, high OFF impedance, and over-voltage tolerance makes the QS3VH125 ideal for high performance communications applications.

The QS3VH125 is characterized for operation from -40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

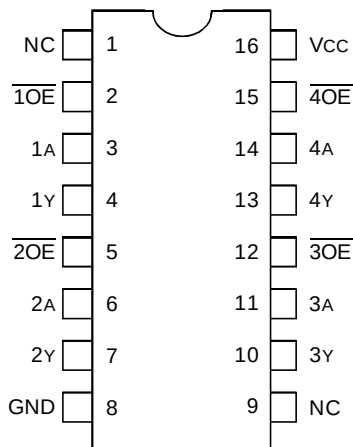


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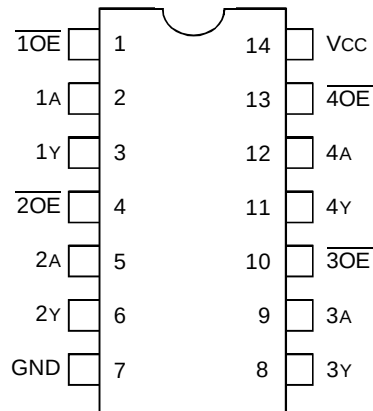
INDUSTRIAL TEMPERATURE RANGE

MARCH 2003

PIN CONFIGURATION



QSOP
TOP VIEW



SOIC/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Supply Voltage to Ground	-0.5 to +4.6	V
VTERM ⁽³⁾	DC Switch Voltage V _S	-0.5 to +5.5	V
VTERM ⁽³⁾	DC Input Voltage V _{IN}	-0.5 to +5.5	V
VAC	AC Input Voltage (pulse width ≤20ns)	-3	V
I _{OUT}	DC Output Current (max. sink current/pin)	120	mA
TSTG	Storage Temperature	-65 to +150	°C

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, F = 1MHz, V_{IN} = 0V, V_{OUT} = 0V)

Symbol	Parameter ⁽¹⁾	Typ.	Max.	Unit
C _{IN}	Control Inputs	3	5	pF
C _{I/O}	Quickswitch Channels (Switch OFF)	4	6	pF
C _{I/O}	Quickswitch Channels (Switch ON)	8	12	pF

NOTE:

- This parameter is guaranteed but not production tested.

PIN DESCRIPTION

Pin Names	I/O	Description
1A - 4A	I/O	Bus A
1Y - 4Y	I/O	Bus Y
1OE - 4OE	I	Output Enable

FUNCTION TABLE⁽¹⁾

OE	A	Y	Function
L	H	H	Connect
L	L	L	Connect
H	X	X	Disconnect

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

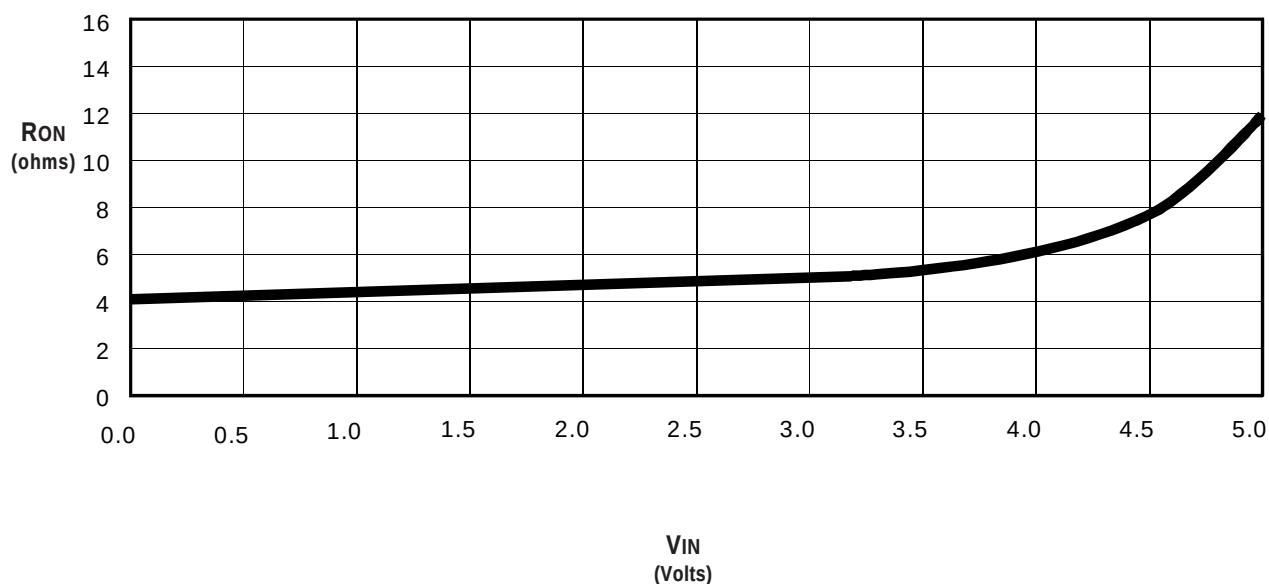
Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$

Symbol	Parameter	Test Conditions			Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	V _{CC} = 2.3V to 2.7V		1.7	—	—	V
			V _{CC} = 2.7V to 3.6V		2	—	—	
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	V _{CC} = 2.3V to 2.7V		—	—	0.7	V
			V _{CC} = 2.7V to 3.6V		—	—	0.8	
I _{IN}	Input Leakage Current (Control Inputs)	0V ≤ V _{IN} ≤ V _{CC}			—	—	±1	μA
I _{OZ}	Off-State Current (Hi-Z)	0V ≤ V _{OUT} ≤ 5V, Switches OFF			—	—	±1	μA
I _{OFF}	Data Input/Output Power Off Leakage	V _{IN} or V _{OUT} 0V to 5V, V _{CC} = 0V			—	—	±1	μA
R _{ON}	Switch ON Resistance	V _{CC} = 2.3V Typical at V _{CC} = 2.5V	V _{IN} = 0V	I _{ON} = 30mA	—	6	8	Ω
			V _{IN} = 1.7V	I _{ON} = 15mA	—	7	9	
		V _{CC} = 3V	V _{IN} = 0V	I _{ON} = 30mA	—	4	6	
			V _{IN} = 2.4V	I _{ON} = 15mA	—	5	8	

NOTE:

1. Typical values are at $V_{CC} = 3.3\text{V}$ and $T_A = 25^{\circ}\text{C}$.

TYPICAL ON RESISTANCE vs V_{IN} AT $V_{CC} = 3.3\text{V}$



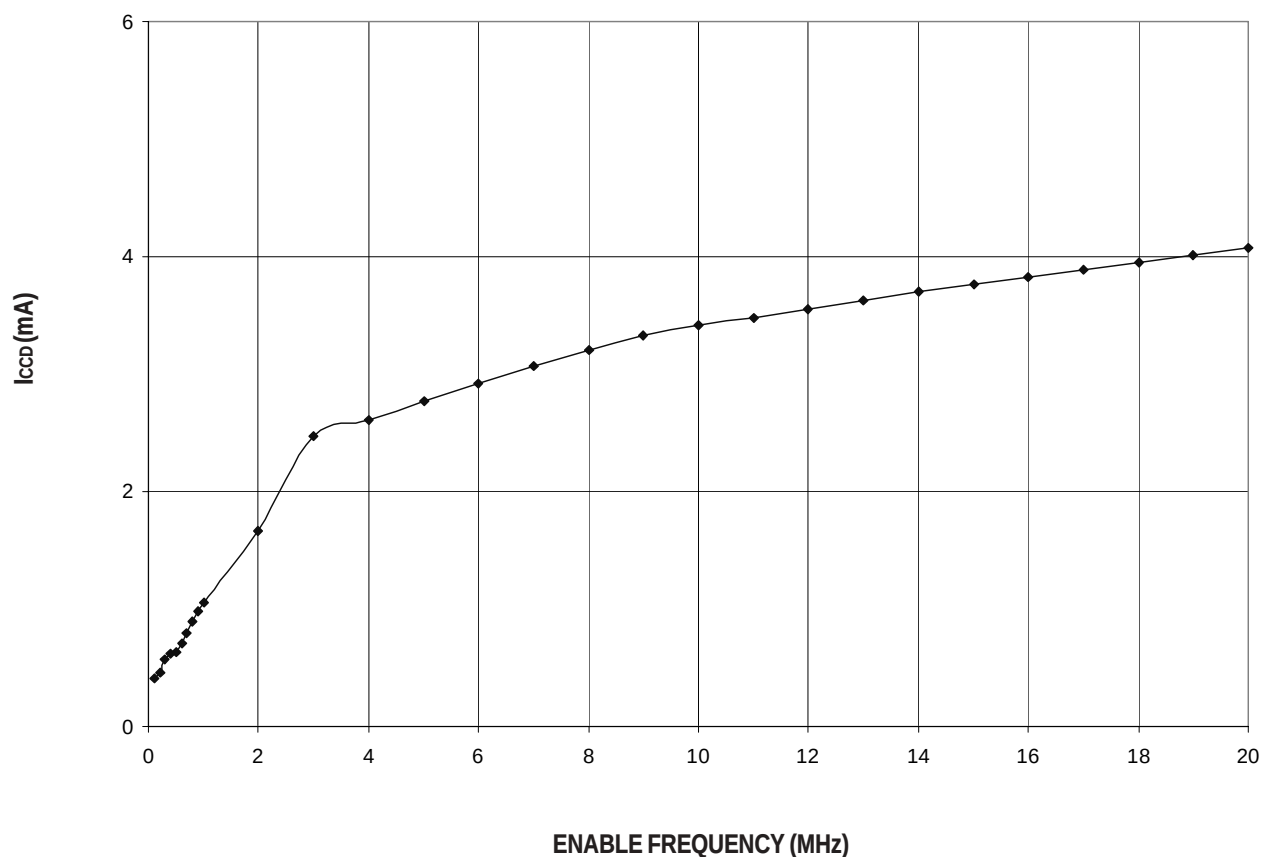
POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ.	Max.	Unit
I _{ccQ}	Quiescent Power Supply Current	V _{CC} = Max., V _{IN} = GND or V _{CC} , f = 0	—	1	3	mA
ΔI _{cc}	Power Supply Current ^(2,3) per Input HIGH	V _{CC} = Max., V _{IN} = 3V, f = 0 per Control Input	—	—	30	μA
I _{ccD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = 3.3V, A and Y Pins Open, Control Inputs Toggling @ 50% Duty Cycle	See Typical I _{ccD} vs Enable Frequency graph below			

NOTES:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
2. Per input driven at the specified level. A and Y pins do not contribute to ΔI_{cc}.
3. This parameter is guaranteed but not tested.
4. This parameter represents the current required to switch internal capacitance at the specified frequency. The A and Y inputs do not contribute to the Dynamic Power Supply Current. This parameter is guaranteed but not production tested.

TYPICAL I_{CCD} vs ENABLE FREQUENCY CURVE AT V_{CC} = 3.3V



SWITCHING CHARACTERISTICS OVER OPERATING RANGE

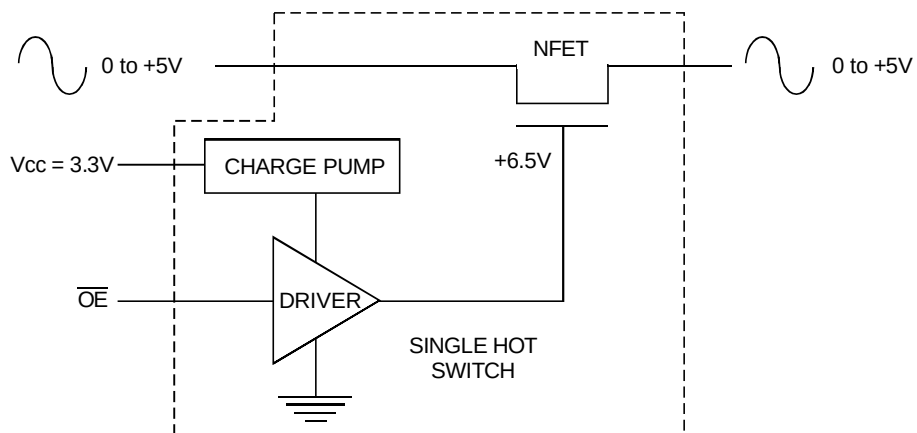
T_A = -40°C to +85°C

Symbol	Parameter	V _{CC} = 2.5 ± 0.2V ⁽¹⁾		V _{CC} = 3.3 ± 0.3V ⁽¹⁾		Unit
		Min. ⁽⁴⁾	Max.	Min. ⁽⁴⁾	Max.	
t _{PLH} t _{PHL}	Data Propagation Delay ^(2,3) A to Y	—	0.2	—	0.2	ns
t _{PZL} t _{PZH}	Switch Turn-On Delay $\overline{\text{xOE}}$ to xA/xY	1.5	8	1.5	6.5	ns
t _{PLZ} t _{PHZ}	Switch Turn-Off Delay $\overline{\text{xOE}}$ to xA/xY	1.5	7	1.5	7	ns
f _{xOE}	Operating Frequency-Enable ^(2,5)	—	10	—	20	MHz

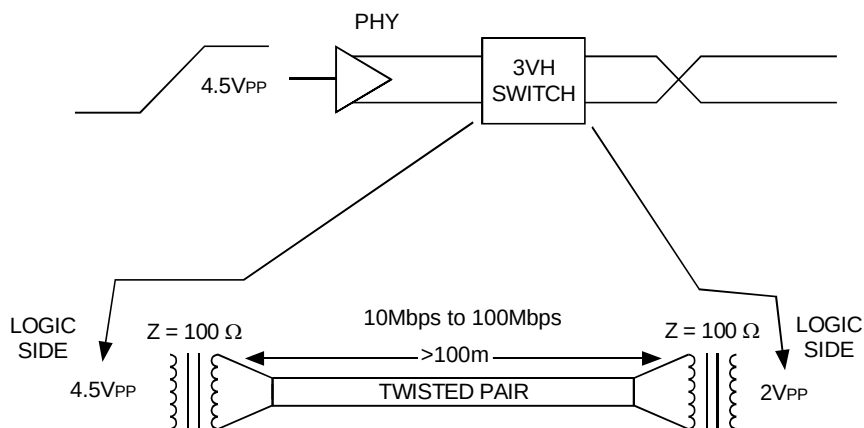
NOTES:

1. See Test Conditions under TEST CIRCUITS AND WAVEFORMS.
2. This parameter is guaranteed but not production tested.
3. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.2ns at C_L = 50pF. Since this time constant is much smaller than the rise and fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
4. Minimums are guaranteed but not production tested.
5. Maximum toggle frequency for $\overline{\text{xOE}}$ control input (pass voltage > V_{CC}, V_{IN} = 5V, R_{LOAD} ≥ 1MΩ, no C_{LOAD}).

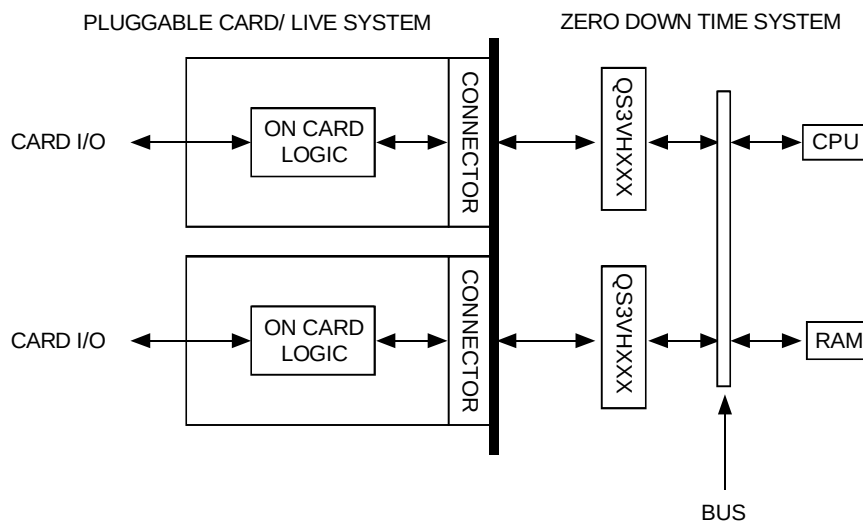
SOME APPLICATIONS FOR HOTSWITCH PRODUCTS



Rail-to-Rail Switching



Fast Ethernet Data Switching (LAN Switch)

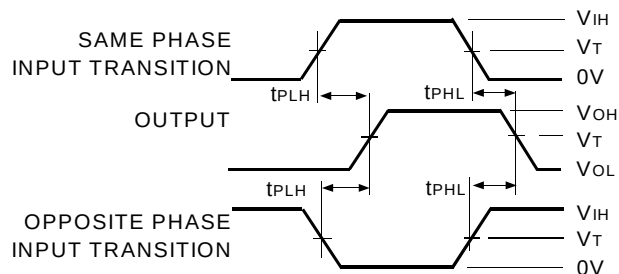


Hot-Swapping

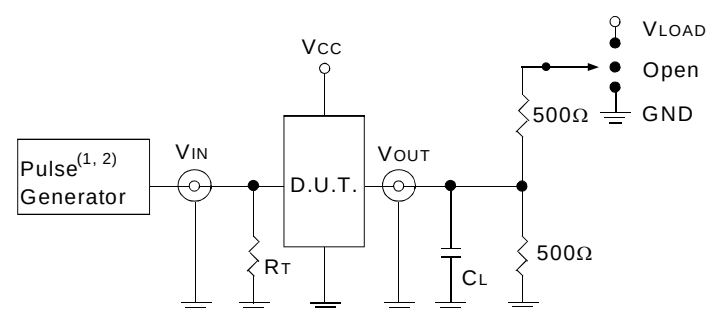
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

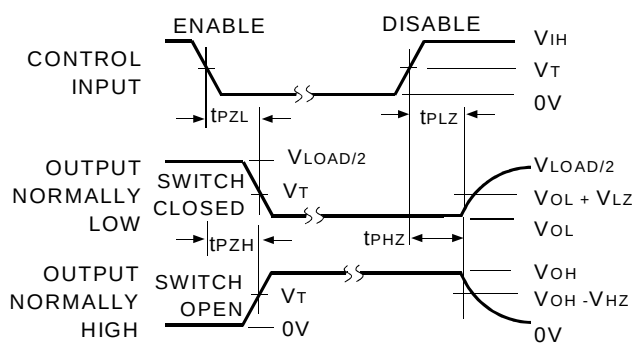
Symbol	$V_{CC}^{(1)} = 3.3V \pm 0.3V$	$V_{CC}^{(2)} = 2.5V \pm 0.2V$	Unit
V_{LOAD}	6	$2 \times V_{CC}$	V
V_{IH}	3	V_{CC}	V
V_T	1.5	$V_{CC}/2$	V
V_{LZ}	300	150	mV
V_{HZ}	300	150	mV
C_L	50	30	pF



Propagation Delay



Test Circuits for All Outputs



NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

Enable and Disable Times

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate $\leq 10\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$.

2. Pulse Generator for All Pulses: Rate $\leq 10\text{MHz}$; $t_r \leq 2\text{ns}$; $t_f \leq 2\text{ns}$.

SWITCH POSITION

Test	Switch
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND
t_{PD}	Open

ORDERING INFORMATION

IDTQS	XXXXX	XX		
	Device Type	Package		
			S1	Small Outline IC
			S1G	SOIC - Green
			Q	Quarter Size Outline Package
			QG	QSOP - Green
			PA	Thin Shrink Small Outline Package
			3VH125	2.5V / 3.3V Quad Active Low, High Bandwidth Switch

DATA SHEET DOCUMENT HISTORY

8/6/2002 Updated according to PCN Logic-0206-11
3/3/2003 Changed Icc limits



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