



## N-Channel Enhancement-Mode Vertical DMOS FETs

### Features

- ▶ Free from secondary breakdown
- ▶ Low power drive requirement
- ▶ Ease of paralleling
- ▶ Low  $C_{ISS}$  and fast switching speeds
- ▶ Excellent thermal stability
- ▶ Integral source-drain diode
- ▶ High input impedance and high gain

### Applications

- ▶ Motor controls
- ▶ Converters
- ▶ Amplifiers
- ▶ Switches
- ▶ Power supply circuits
- ▶ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

### Ordering Information

| Part Number   | Package Option | Packing   |
|---------------|----------------|-----------|
| 2N7008-G      | TO-92          | 1000/Bag  |
| 2N7008-G P002 | TO-92          | 2000/Reel |
| 2N7008-G P003 | TO-92          | 2000/Reel |
| 2N7008-G P005 | TO-92          | 2000/Reel |
| 2N7008-G P013 | TO-92          | 2000/Reel |
| 2N7008-G P014 | TO-92          | 2000/Reel |

-G denotes a lead (Pb)-free / RoHS compliant package.

Contact factory for Wafer / Die availability.

Devices in Wafer / Die form are lead (Pb)-free / RoHS compliant.

### Absolute Maximum Ratings

| Parameter                         | Value                             |
|-----------------------------------|-----------------------------------|
| Drain-to-source voltage           | $BV_{DSS}$                        |
| Drain-to-gate voltage             | $BV_{DGS}$                        |
| Gate-to-source voltage            | $\pm 30V$                         |
| Operating and storage temperature | $-55^{\circ}C$ to $+150^{\circ}C$ |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

### General Description

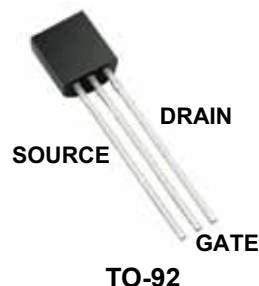
The Supertex 2N7008 is an enhancement-mode (normally-off) transistor that utilizes a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors, and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

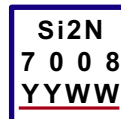
### Product Summary

| $BV_{DSX}/BV_{DGS}$ | $R_{DS(ON)}$<br>(max) | $I_{D(ON)}$ |
|---------------------|-----------------------|-------------|
| 60V                 | $7.5 \Omega$          | 500mA       |

### Pin Configuration



### Product Marking



YY = Year Sealed  
WW = Week Sealed  
\_\_\_\_\_ = "Green" Packaging

Package may or may not include the following marks: Si or

TO-92

### Typical Thermal Characteristics

| Package | $\theta_{ja}$    |
|---------|------------------|
| TO-92   | $132^{\circ}C/W$ |

\* Mounted on FR4 board; 25mm x 25mm x 1.57mm

## Thermal Characteristics

| Package | $I_D$<br>(continuous) <sup>†</sup> | $I_D$<br>(pulsed) | Power Dissipation<br>@ $T_c = 25^\circ\text{C}$ | $I_{DR}^†$ | $I_{DRM}$ |
|---------|------------------------------------|-------------------|---|------------|-----------|
| TO-92   | 230mA                              | 1.3A              | 1.0W  | 230mA      | 1.3A      |

**Note:**

<sup>†</sup>  $I_D$  (continuous) is limited by max rated  $T_J$ .

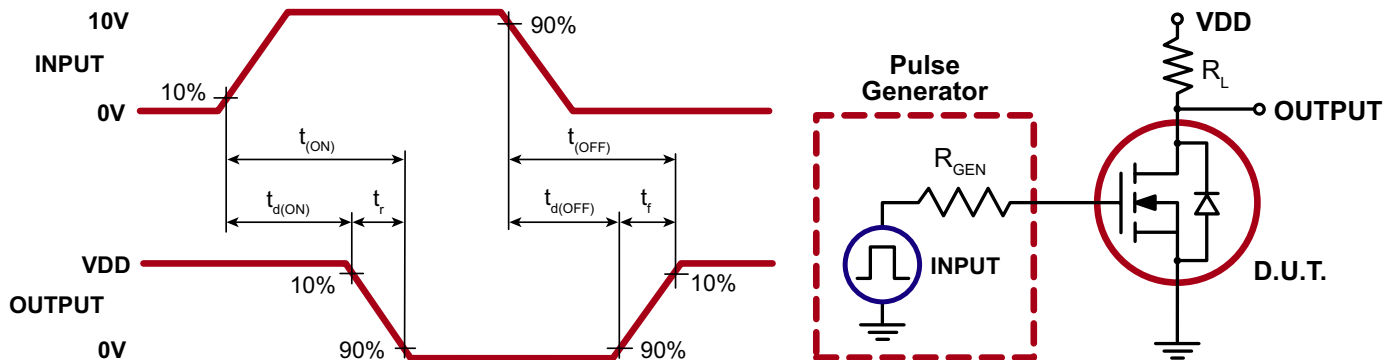
## Electrical Characteristics ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

| Sym          | Parameter                                  | Min | Typ | Max | Units    | Conditions   |
|--------------|--|-----|-----|-----|----------|--|
| $BV_{DSS}$   | Drain-to-source breakdown voltage          | 60  | -   | -   | V        | $V_{GS} = 0V, I_D = -10\mu A$                        |
| $V_{GS(th)}$ | Gate threshold voltage                     | 1.0 | -   | 2.5 | V        | $V_{GS} = V_{DS}, I_D = 250\mu A$                    |
| $I_{GSS}$    | Gate body leakage current                  | -   | -   | 100 | nA       | $V_{GS} = \pm 30V, V_{DS} = 0V$                      |
| $I_{DSS}$    | Zero gate voltage drain current            | -   | -   | 1.0 | $\mu A$  | $V_{GS} = 0V, V_{DS} = 50V$                          |
|              |  | -   | -   | 500 |          | $V_{GS} = 0V, V_{DS} = 50V, T_A = 125^\circ\text{C}$ |
| $I_{D(ON)}$  | On-state drain current                     | 500 | -   | -   | mA       | $V_{GS} = 10V, V_{DS} \geq 2.0V_{DS(ON)}$            |
| $R_{DS(ON)}$ | Static drain-to-source on-state resistance | -   | -   | 7.5 | $\Omega$ | $V_{GS} = 5.0V, I_D = 50mA$                          |
|              |  | -   | -   | 7.5 |          | $V_{GS} = 10V, I_D = 500mA$                          |
| $G_{FS}$     | Forward transconductance                   | 80  | -   | -   | mmho     | $V_{DS} = 10V, I_D = 200mA$                          |
| $C_{ISS}$    | Input capacitance                          | -   | -   | 50  | pF       | $V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz$              |
| $C_{OSS}$    | Common source output capacitance           | -   | -   | 25  |          |  |
| $C_{RSS}$    | Reverse transfer capacitance               | -   | -   | 5.0 |          |  |
| $t_{(ON)}$   | Turn-on time                               | -   | -   | 20  | ns       | $V_{DD} = 30V, I_D = 200mA, R_{GEN} = 25\Omega$      |
| $t_{(OFF)}$  | Turn-off time                              | -   | -   | 20  |          |  |
| $V_{SD}$     | Diode forward voltage drop                 | -   | -   | 1.5 | V        | $V_{GS} = 0V, I_{SD} = 150mA$                        |

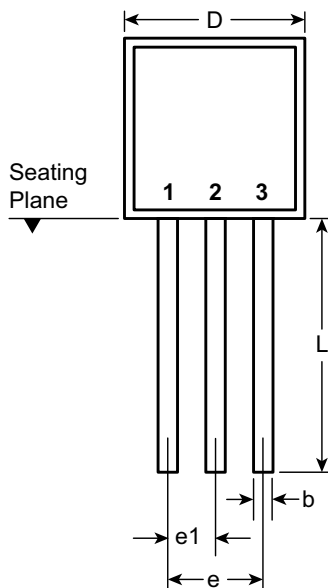
**Notes:**

1. All D.C. parameters 100% tested at  $25^\circ\text{C}$  unless otherwise stated. (Pulse test: 300 $\mu s$  pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

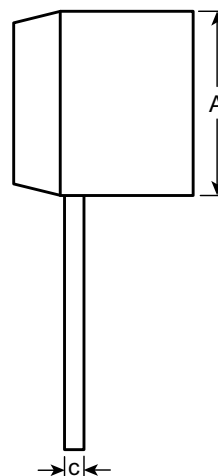
## Switching Waveforms and Test Circuit



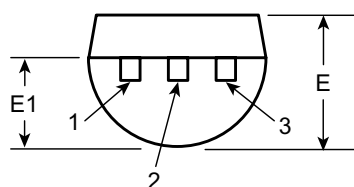
### 3-Lead TO-92 Package Outline (N3)



**Front View**



**Side View**



**Bottom View**

| Symbol                 |     | A    | b                 | c                 | D    | E    | E1   | e    | e1   | L     |
|------------------------|-----|------|-------------------|-------------------|------|------|------|------|------|-------|
| Dimensions<br>(inches) | MIN | .170 | .014 <sup>†</sup> | .014 <sup>†</sup> | .175 | .125 | .080 | .095 | .045 | .500  |
|                        | NOM | -    | -                 | -                 | -    | -    | -    | -    | -    | -     |
|                        | MAX | .210 | .022 <sup>†</sup> | .022 <sup>†</sup> | .205 | .165 | .105 | .105 | .055 | .610* |

JEDEC Registration TO-92.

\* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

**Drawings not to scale.**

**Supertex Doc.#:** DSPD-3TO92N3, Version E041009.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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