

SSM8401

Dual Enhancement Mode MOSFET

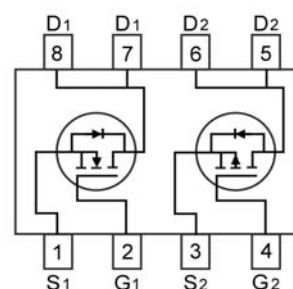
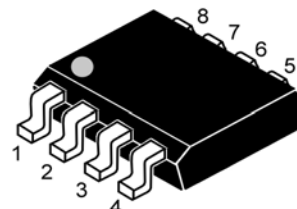
Product Summary (N-Channel)

V_{DS} (V)	I_D (A)	$R_{DS(ON)}$ (m Ω) Max
30V	7A	25 @ $V_{GS} = 10V$
		40 @ $V_{GS} = 4.5V$

Product Summary (P-Channel)

V_{DS} (V)	I_D (A)	$R_{DS(ON)}$ (m Ω) Max
-30V	-4.5A	55 @ $V_{GS} = -10V$
		85 @ $V_{GS} = -4.5V$

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ABSOLUTE MAXIMUM RATINGS ($T_A=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit (N-Channel)	Limit (P-Channel)	Unit
Drain-Source Voltage	V_{DS}	30	-30	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Drain Current-Continuous ^a @ $T_J = 125^{\circ}C$	I_D	7	-4.5	A
-Pulsed ^b	I_{DM}	30	-18	A
Drain-Source Diode Forward Current ^a	I_S	-1.7	-1.7	A
Maximum Power Dissipation ^a	P_D	2		
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150		$^{\circ}C$

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient ^a	$R_{\theta JA}$	62.5	$^{\circ}C/W$
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South Sea Semiconductor reserves the right to make changes to improve reliability or manufacturability without advance notice.

South Sea Semiconductor, August 2005 (Rev 1.0)



N-Channel ELECTRICAL CHARACTERISTICS ($T_A=25^{\circ}\text{C}$ unless otherwise noted)						
Parameter	Symbol	Condition	Min	Typ ^c	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=24V, V_{GS}=0V$			1	μA
Gate-Body Leakage	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.5	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=9A$		20	25	m Ω
		$V_{GS}=4.5V, I_D=7A$		35	40	
On-State Drain Current	$I_{D(ON)}$	$V_{DS}=10V, V_{GS}=10V$	19			A
Forward Transconductance	g_{FS}	$V_{DS}=10V, I_D=5A$		5		S
Input Capacitance	C_{ISS}	$V_{DS}=15V,$ $V_{GS}=0V,$ $f=1.0MHz$		850		pF
Output Capacitance	C_{OSS}			150		
Reverse Transfer Capacitance	C_{RSS}			105		
Turn-On Delay Time	$t_{D(ON)}$	$V_{DD}=15V,$ $I_D=1A,$ $V_{GS}=10V,$ $R_{GEN}=6\Omega$		22		ns
Rise Time	t_r			19		
Turn-Off Delay Time	$t_{D(OFF)}$			19		
Fall Time	t_f			16.5		
Total Gate Charge	Q_g	$V_{DS}=15V, I_D=9A, V_{GS}=10V$		17.5		nC
		$V_{DS}=15V, I_D=9A, V_{GS}=4.5V$		8.5		
Gate-Source Charge	Q_{gs}	$V_{DS}=15V, I_D=9A,$ $V_{GS}=10V$		3.5		
Gate-Drain Charge	Q_{gd}			3		
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=1.7A$		0.8	1.2	V



P-Channel ELECTRICAL CHARACTERISTICS ($T_A=25^{\circ}\text{C}$ unless otherwise noted)						
Parameter	Symbol	Condition	Min	Typ ^c	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-24V, V_{GS}=0V$			-1	μA
Gate-Body Leakage	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1	-1.5	-2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-10V, I_D=-4.5A$		45	55	m Ω
		$V_{GS}=-4.5V, I_D=-3.6A$		75	85	
On-State Drain Current	$I_{D(ON)}$	$V_{DS}=-5V, V_{GS}=-10V$	-11.5			A
Forward Transconductance	g_{FS}	$V_{DS}=-15V, I_D=-4.5A$		5		S
Input Capacitance	C_{ISS}	$V_{DS}=-15V,$		590		pF
Output Capacitance	C_{OSS}	$V_{GS}=0V,$		130		
Reverse Transfer Capacitance	C_{RSS}	$f=1.0MHz$		90		
Turn-On Delay Time	$t_{D(ON)}$	$V_D=-15V, I_D=-1A,$		7		ns
Rise Time	t_r	$R_L=15\Omega,$		4.5		
Turn-Off Delay Time	$t_{D(OFF)}$	$V_{GS}=-10V,$		58.5		
Fall Time	t_f	$R_{GEN}=6\Omega$		21.5		
Total Gate Charge	Q_g	$V_{DS}=-15V, I_D=-4.9A, V_{GS}=-10V$		13		nC
		$V_{DS}=-15V, I_D=-4.9A, V_{GS}=-4.5V$		6.5		
Gate-Source Charge	Q_{gs}	$V_{DS}=-15V, I_D=-4.9A,$		2.2		
Gate-Drain Charge	Q_{gd}	$V_{GS}=-10V$		3.2		
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=-1.7A$		-0.8	-1.2	V

Notes :

- Surface Mounted on FR4 Board, $t \leq 10\text{sec}$.
- Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.



N - Channel

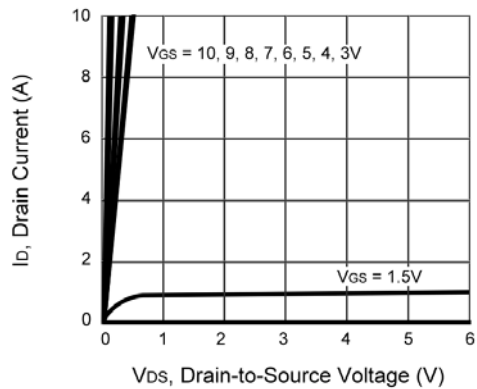


Figure 1. Output Characteristics

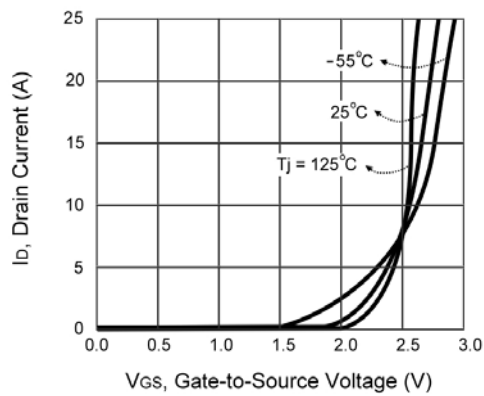


Figure 2. Transfer Characteristics

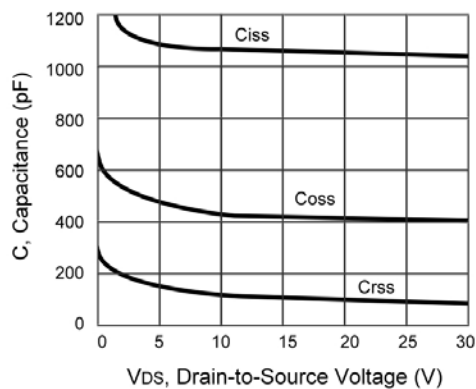


Figure 3. Capacitance

P - Channel

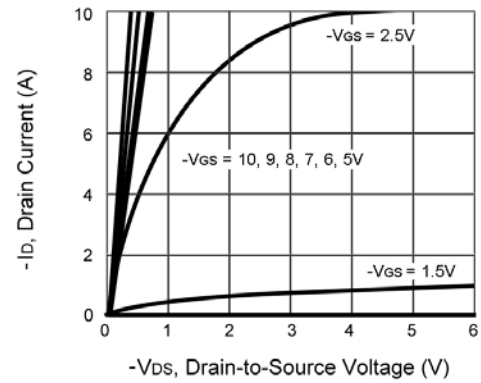


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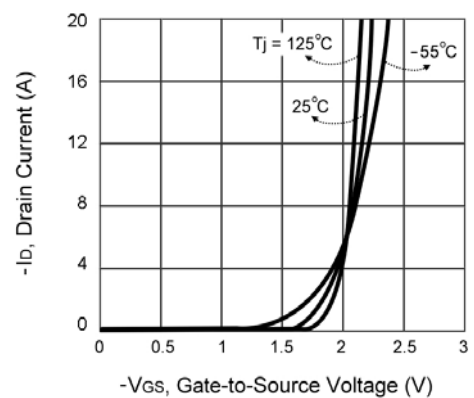


Figure 2. Transfer Characteristics

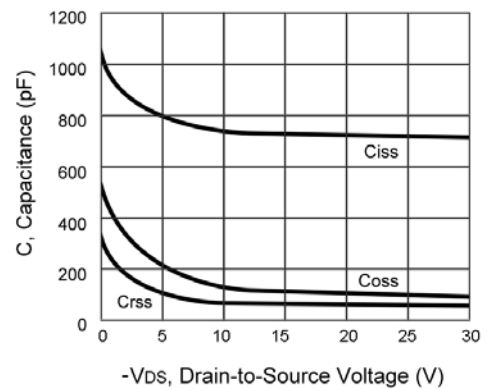


Figure 3. Capacitance



N - Channel

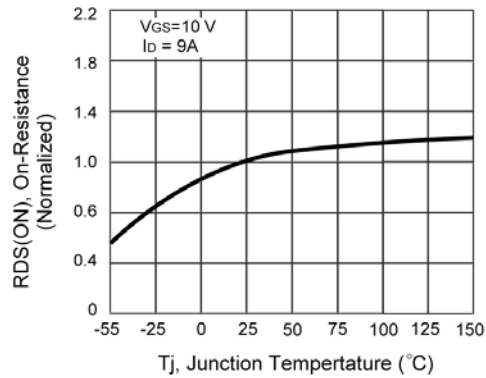


Figure 4. On-Resistance Variation with Temperature

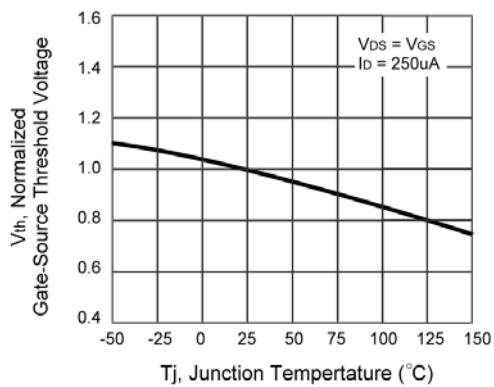


Figure 5. Gate Threshold Variation with Temperature

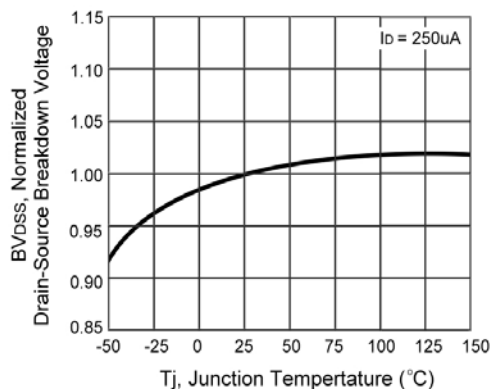


Figure 6. Breakdown Voltage Variation with Temperature

P - Channel

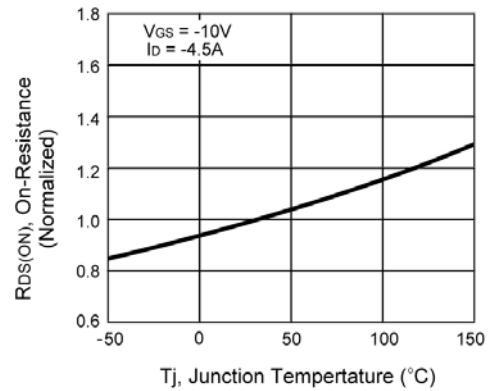


Figure 4. On-Resistance Variation with Temperature

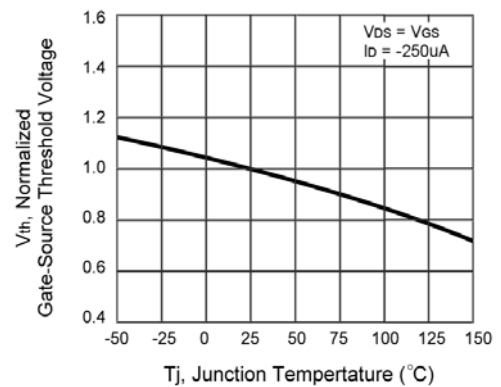


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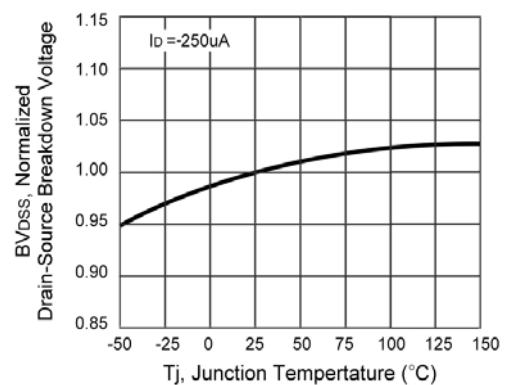


Figure 6. Breakdown Voltage Variation with Temperature



N - Channel

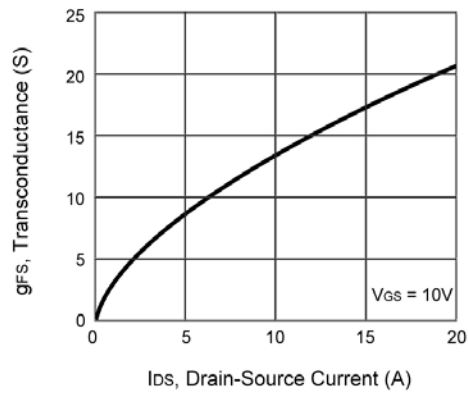


Figure 7. Transconductance Variation with Drain Current

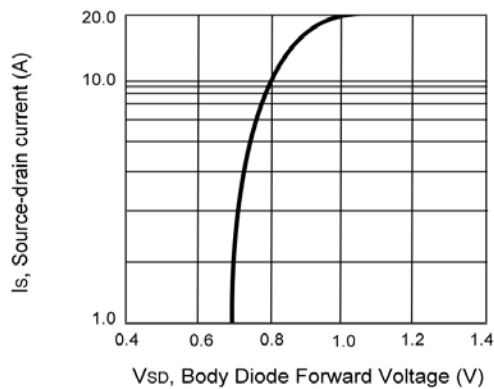


Figure 8. Body Diode Forward Voltage Variation with Source Current

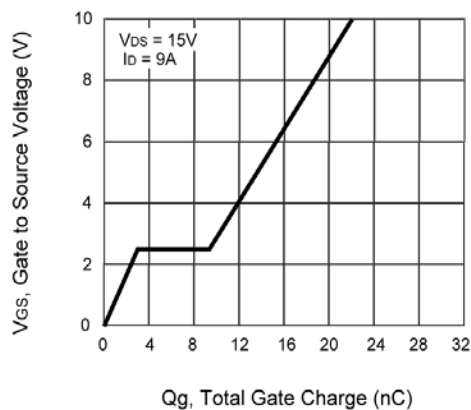


Figure 9. Gate Charge

P - Channel

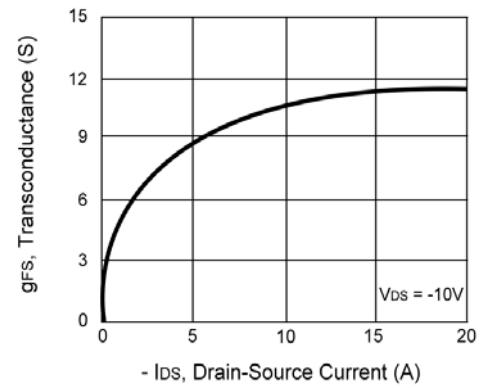


Figure 7. Transconductance Variation with Drain Current

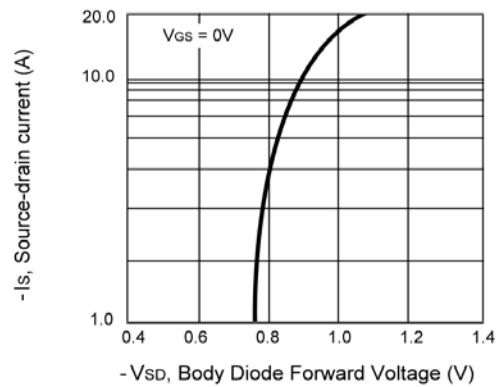


Figure 8. Body Diode Forward Voltage Variation with Source Current

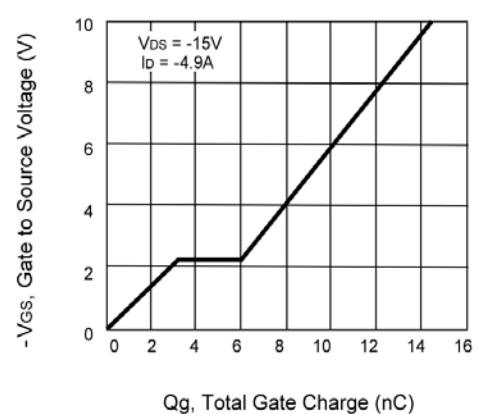


Figure 9. Gate Charge



N - Channel

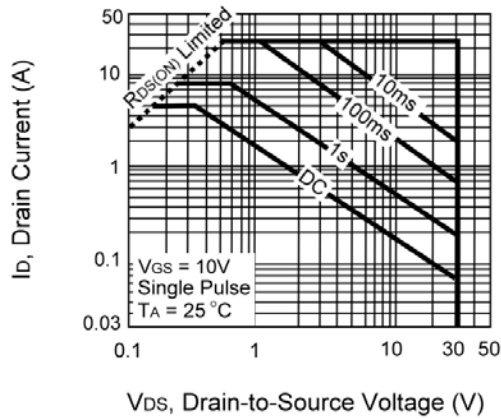


Figure 10. Maximum Safe Operating Area

P - Channel

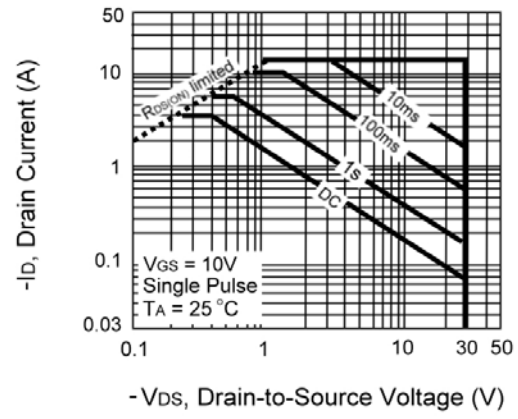


Figure 10. Maximum Safe Operating Area

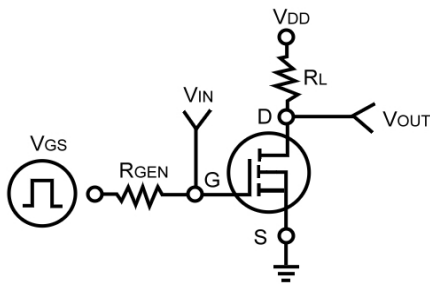


Figure 11. Switching Test Circuit

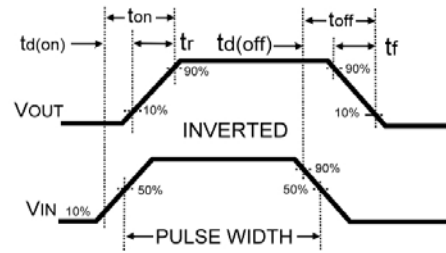


Figure 12. Switching Waveforms

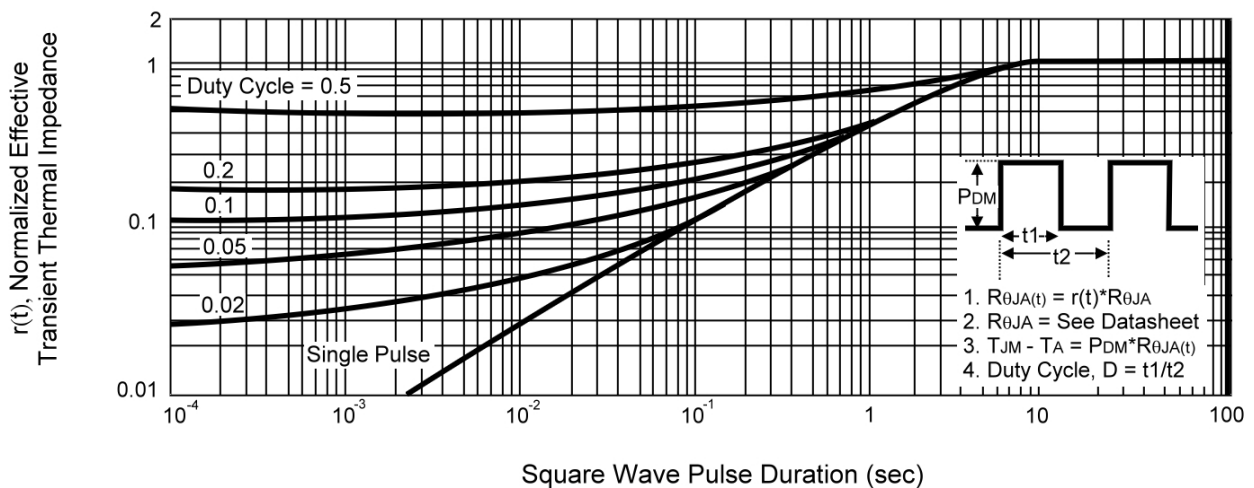
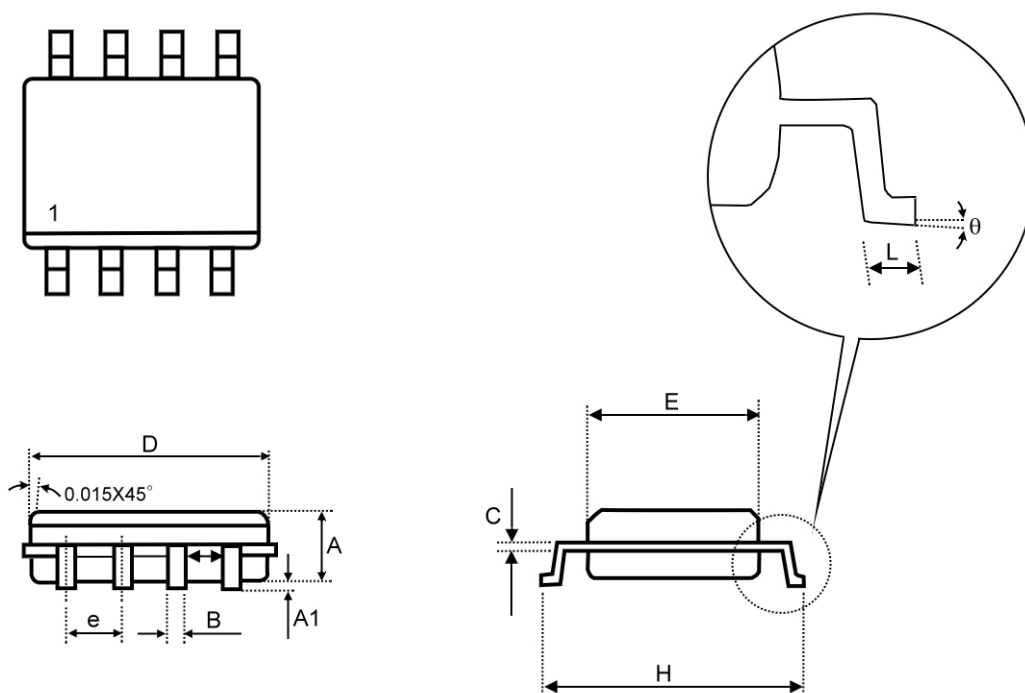


Figure 13. Normalized Thermal Transient Impedance Curve



Package Outline Dimensions

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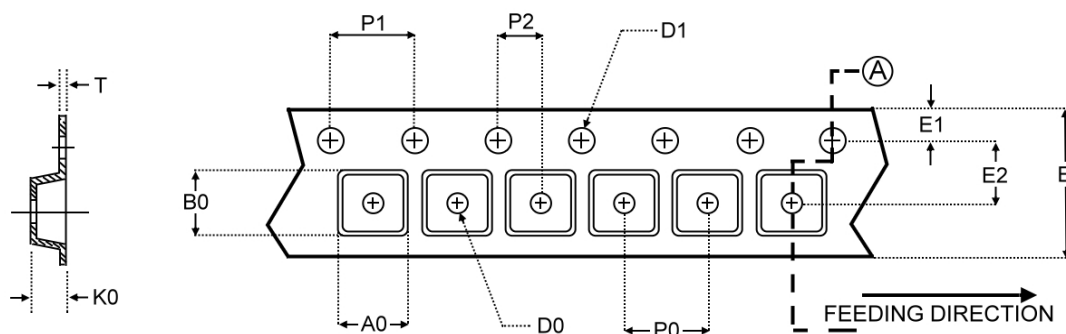


SYMBOLS	MILLIMETERS		INCHES	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
B	0.41 TYP.		0.016 TYP.	
C	0.20 TYP.		0.008 TYP.	
D	4.80	4.98	0.189	0.196
E	3.81	3.99	0.150	0.157
e	1.25 TYP.		0.05 TYP.	
H	5.79	6.20	0.228	0.244
L	0.41	1.27	0.016	0.050
θ	0°	8°	0°	8°



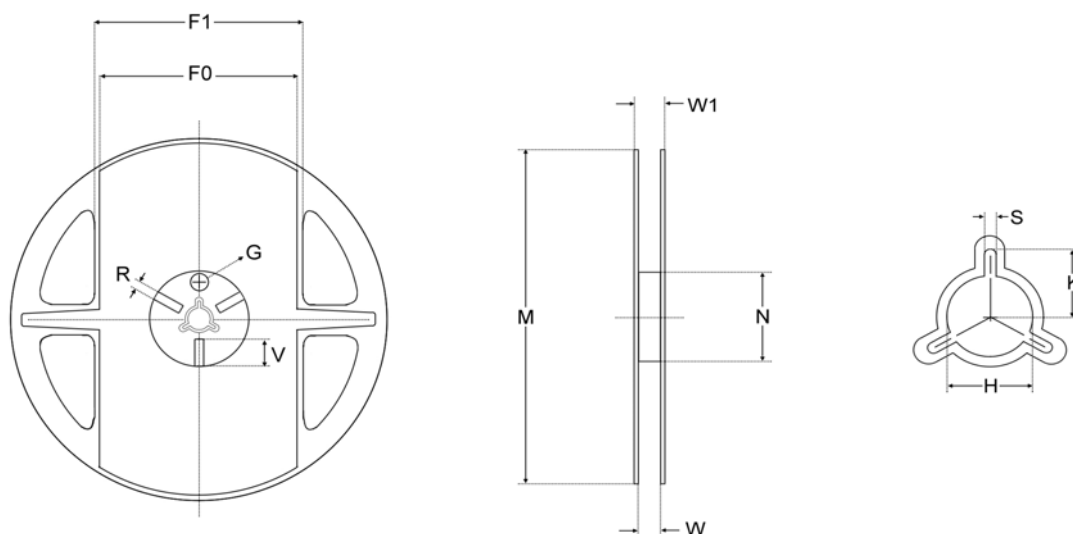
Carrier Tape & Reel Dimensions

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Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
SOP 8N 150mil	6.40	5.20	2.10	$\phi 1.50$ (Min.)	$\phi 1.50$ + 0.10 - 0.00	12.00 ± 0.30	1.75	5.50 ± 0.05	8.00	4.00	2.00 ± 0.05	0.30 ± 0.05

UNIT : mm



Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
12mm	$\phi 330$	330 ± 1	62 ± 1.5	12.4 + 0.2	16.8 - 0.4	$\phi 12.75$ 0.15	-	2.0 ± 0.15	-	-	-

UNIT : mm