

AZ100EL16VS

ECL/PECL Differential Receiver with Variable Output Swing

FEATURES

- 250ps Propagation Delay
- High Bandwidth Output Transitions
- 75k Ω Internal Input Pulldown Resistors
- Functionally Equivalent to ON Semiconductor MC100EL16
- Variable Output Swing
- Available in a 3x3mm MLP Package

PACKAGE AVAILABILITY

PACKAGE	PART NO.	MARKING
MLP 8	AZ100EL16VSL	AZM16P
MLP 8 T&R	AZ100EL16VSLR1	AZM16P
MLP 8 T&R	AZ100EL16VSLR2	AZM16P
SOIC 8	AZ100EL16VSD	AZM100EL16VS
SOIC 8 T&R	AZ100EL16VSDR1	AZM100EL16VS
SOIC 8 T&R	AZ100EL16VSDR2	AZM100EL16VS
TSSOP 8	AZ100EL16VST	AZH16VS
TSSOP 8 T&R	AZ100EL16VSTR1	AZH16VS
TSSOP 8 T&R	AZ100EL16VSTR2	AZH16VS

DESCRIPTION

The AZ100EL16VS is a differential receiver with variable output swing. The EL16VS has functionality and output transition times similar to the EL16, with an input that controls the amplitude of the Q/ $\bar{Q}$ outputs. Maximum swing is achieved by leaving the V_{CTRL} pin open or tied to V_{EE} .

The operational range of the EL16VS control input, V_{CTRL} , is from V_{BB} (full swing) to V_{CC} (min. swing). Simple control of the output swing can be obtained by a variable resistor between the V_{BB} and V_{CC} pins, with the wiper driving V_{CTRL} . Typical application circuits and results are described in this Data Sheet.

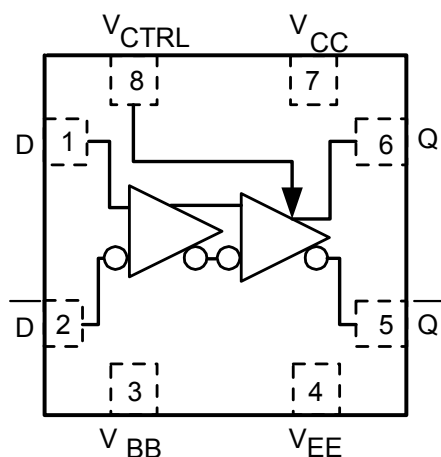
The EL16VS provides a V_{BB} output for single-ended use or a DC bias reference for AC coupling to the device. For single-ended input applications, the V_{BB} reference should be connected to one side of the D/ $\bar{D}$ differential input pair. The input signal is then fed to the other D/ $\bar{D}$ input. The V_{BB} pin can support 1.0mA sink/source current. When used, the V_{BB} pin should be bypassed to ground via a 0.01 μ F capacitor.

Under open input conditions (pulled to V_{EE}) internal input clamps will force the Q output LOW.

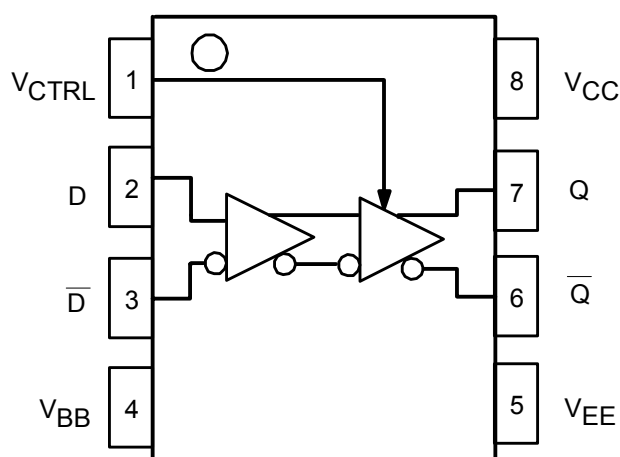
NOTE: Specifications in ECL/PECL tables are valid when thermal equilibrium is established.

AZ100EL16VS

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



8 MLP (TOP VIEW)



8 SOIC & 8 TSSOP

PIN DESCRIPTION

PIN	FUNCTION
D, $\bar{D}$	Data Inputs
V_{CTRL}	Output Swing Control
Q, $\bar{Q}$	Data Outputs
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Rating	Unit
V_{CC}	PECL Power Supply ($V_{EE} = 0V$)	0 to +8.0	Vdc
V_I	PECL Input Voltage ($V_{EE} = 0V$)	0 to +6.0	Vdc
V_{EE}	ECL Power Supply ($V_{CC} = 0V$)	-8.0 to 0	Vdc
V_I	ECL Input Voltage ($V_{CC} = 0V$)	-6.0 to 0	Vdc
I_{OUT}	Output Current --- Continuous --- Surge	50 100	mA
T_A	Operating Temperature Range	-40 to +85	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C

100K ECL DC Characteristics ($V_{EE} = -4.2V$ to $-5.5V$, $V_{CC} = GND$; $V_{CTRL} = V_{BB}$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V _{OH}	Output HIGH Voltage ²	-1085		-880	-1025		-880	-1025	-955	-880	-1025		-880	mV
V _{OL}	Output LOW Voltage ² V _{CTRL} = V _{BB} ¹	-1890		-1620	-1870		-1680	-1870	-1775	-1680	-1870		-1680	mV
V _{OL}	Output LOW Voltage ² V _{CTRL} = V _{CC}	-1180		-975	-1135		-990	-1135	-1065	-990	-1135		-990	mV
V _{IH}	Input HIGH Voltage	-1165		-880	-1165		-880	-1165		-880	-1165		-880	mV
V _{IL}	Input LOW Voltage	-1810		-1475	-1810		-1475	-1810		-1475	-1810		-1475	mV
V _{BB}	Reference Voltage	-1420		-1260	-1420		-1260	-1420		-1260	-1420		-1260	mV
I _{IH}	Input HIGH Current D, $\bar{D}$ V _{CTRL}			150 40			150 40			150 40			150 40	μA
I _{IL}	Input LOW Current	0.5			0.5			0.5			0.5			μA
I _{EE}	Power Supply Current		18	25		18	25		18	25		21	26	mA

- If V_{CTRL} is Open Circuit, use the V_{OH} (Max & Min) and V_{OL} ($V_{CTRL} = V_{REF}$: Max only) limits.
- Each output is terminated through a 50Ω resistor to $V_{CC} - 2V$.

AZ100EL16VS

100K PECL DC Characteristics ($V_{EE} = \text{GND}$, $V_{CC} = +5.0\text{V}$)

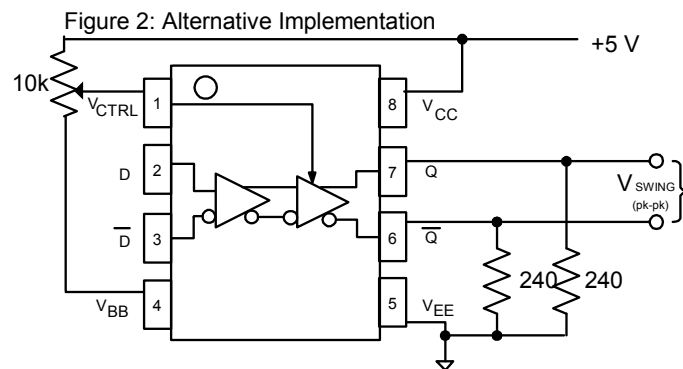
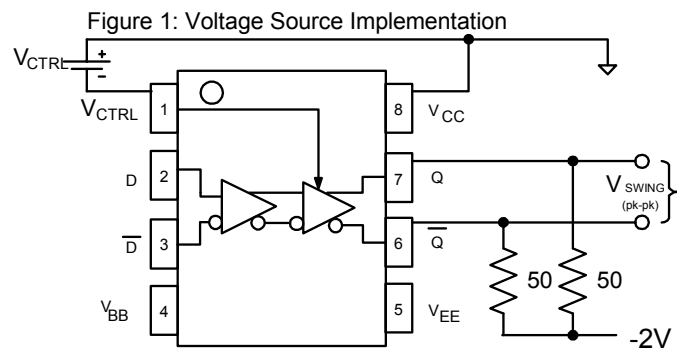
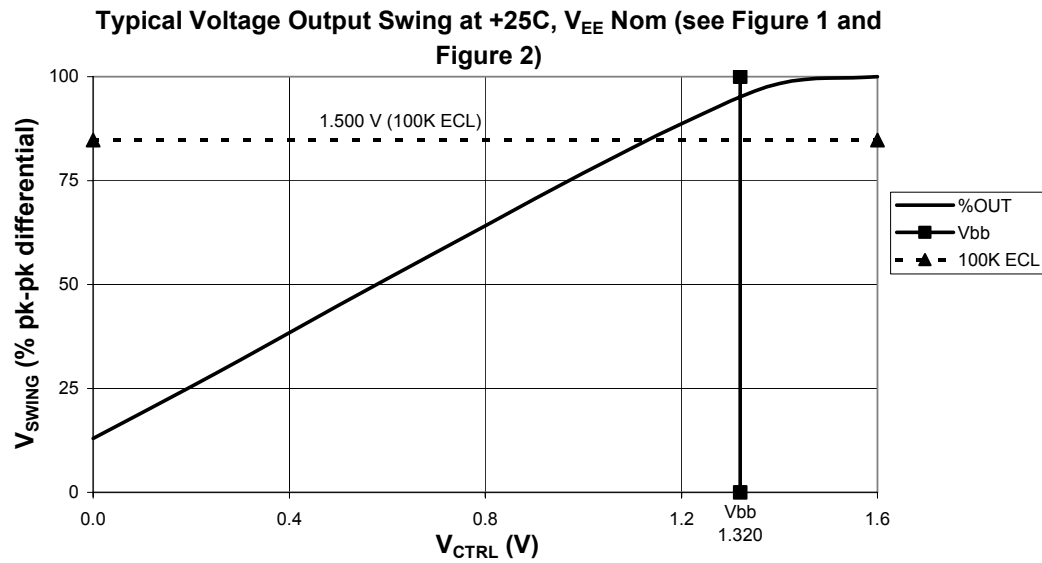
Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage ^{1,3}	3915		4120	3975		4120	3975	4045	4120	3975		4120	mV
V_{OL}	Output LOW Voltage ^{1,3} $V_{CTRL} = V_{BB}^2$	3110		3380	3130		3320	3130	3225	3320	3130		3320	mV
V_{OL}	Output LOW Voltage ^{1,3} $V_{CTRL} = V_{CC}$	3820		4025	3865		4010	3865	3935	4010	3865		4010	mV
V_{IH}	Input HIGH Voltage ¹	3835		4120	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage ¹	3190		3525	3190		3525	3190		3525	3190		3525	mV
V_{BB}	Reference Voltage ¹	3580		3740	3580		3740	3580		3740	3580		3740	mV
I_{IH}	Input HIGH Current D, $\bar{D}$ V_{CTRL}			150 40			150 40			150 40			150 40	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			0.5			μA
I_{EE}	Power Supply Current		18	25		18	25		18	25		21	26	mA

- For supply voltages other than 5.0V, use the ECL table values and ADD supply voltage value.
- If V_{CTRL} is Open Circuit, use the V_{OH} (Max & Min) and V_{OL} ($V_{CTRL} = V_{REF}$: Max only) limits.
- Each output is terminated through a 50 Ω resistor to $V_{CC} - 2\text{V}$.

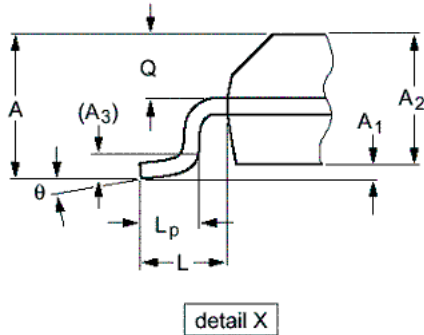
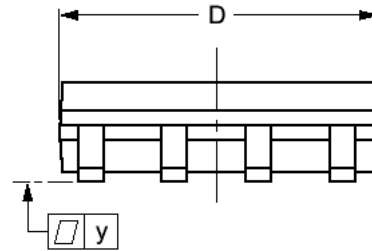
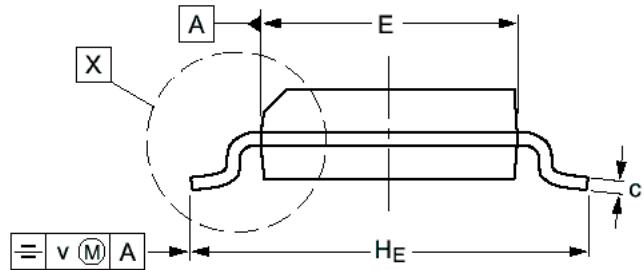
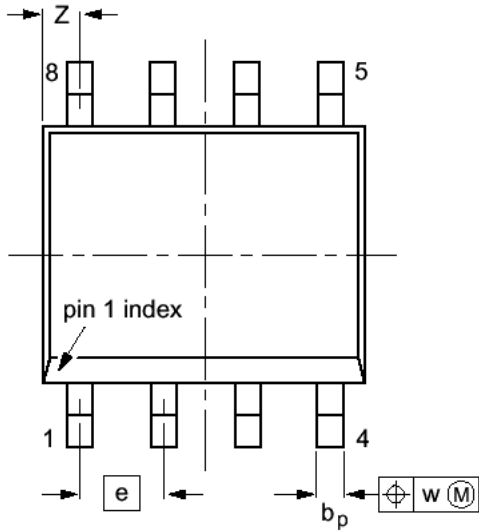
AC Characteristics ($V_{EE} = -4.2\text{V}$ to -5.5V ; $V_{CC} = \text{GND}$ or $V_{EE} = \text{GND}$; $V_{CC} = +4.2\text{V}$ to $+5.5\text{V}$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH} / t_{PHL}	Input to Output Delay (Diff) (SE)		250 250		175 125	250 250	325 375	175 125	250 250	325 375	205 155	280 280	355 405	ps
t_{SKEW}	Duty Cycle Skew ¹ (Diff)		5			5	20		5	20		5	20	ps
$V_{PP}(\text{AC})$	Minimum Input Swing ²	150			150			150			150			mV
V_{CMR}	Common Mode Range ³	$V_{CC} - 2.0$		$V_{CC} - 0.4$	$V_{CC} - 2.0$		$V_{CC} - 0.4$	$V_{CC} - 2.0$		$V_{CC} - 0.4$	$V_{CC} - 2.0$		$V_{CC} - 0.4$	V
t_r / t_f	Rise/Fall Time 20 – 80%	100		350	100		350	100		350	100		350	ps

- Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.
- V_{PP} is the minimum peak-to-peak differential input swing for which AC parameters are guaranteed.
- The V_{CMR} range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between $V_{PP}(\text{min})$ and 1V.



**PACKAGE DIAGRAM
SOIC 8**

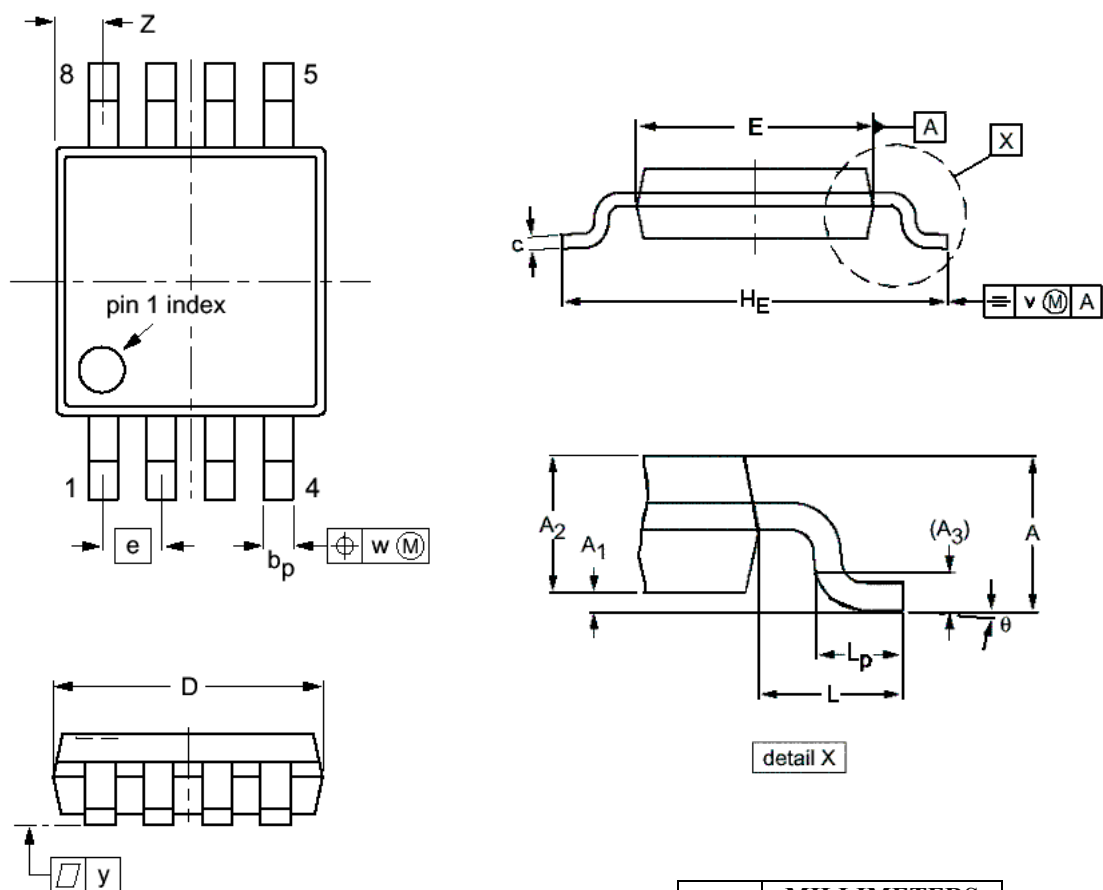


NOTES:

1. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
2. MAXIMUM MOLD PROTRUSION FOR D IS 0.15mm.
3. MAXIMUM MOLD PROTRUSION FOR E IS 0.25mm.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.32	12.57	0.485	0.495
A₁	0.10	0.25	0.004	0.010
A₂	1.25	1.45	0.049	0.057
A₃	0.25		0.01	
b_p	0.36	0.49	0.014	0.019
c	0.19	0.25	0.0075	0.0100
D	4.8	5.0	0.19	0.20
E	3.8	4.0	0.15	0.16
e	1.27		0.050	
H_E	5.80	6.20	0.228	0.244
L	1.05		0.041	
L_p	0.40	1.00	0.016	0.039
Q	0.60	0.70	0.024	0.028
v	0.25		0.01	
w	0.25		0.01	
y	0.10		0.004	
Z	0.30	0.70	0.012	0.028
θ	0°	8°	0°	8°

**PACKAGE DIAGRAM
TSSOP 8**

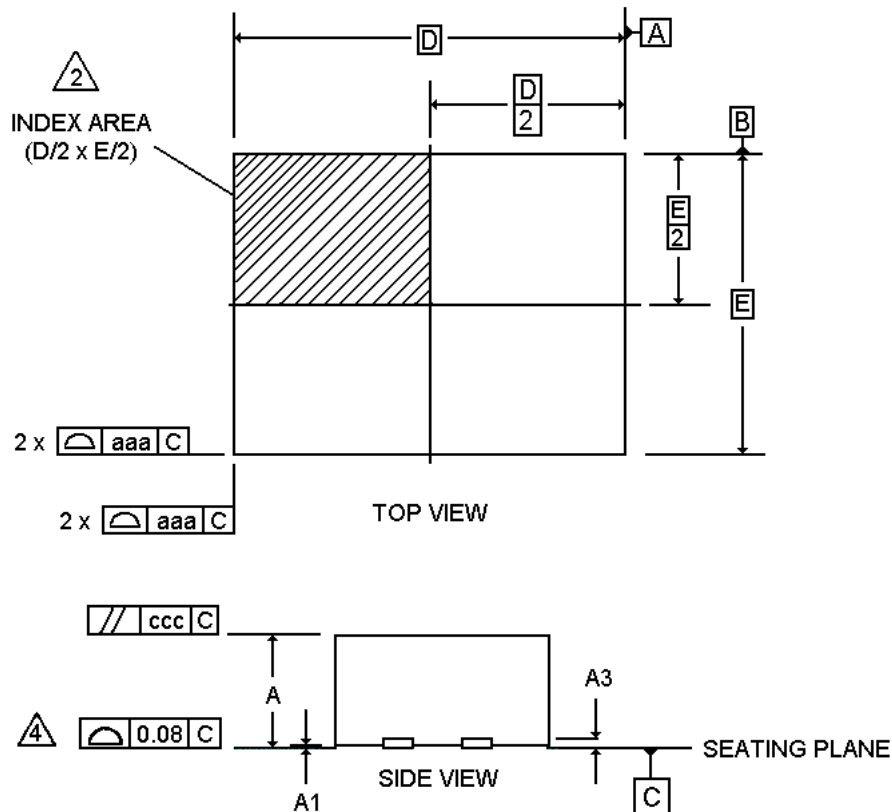


NOTES:

1. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
2. MAXIMUM MOLD PROTRUSION FOR D IS 0.15mm.
3. MAXIMUM MOLD PROTRUSION FOR E IS 0.25mm.

DIM	MILLIMETERS	
	MIN	MAX
A		1.10
A ₁	0.05	0.15
A ₂	0.80	0.95
A ₃	0.25	
b _p	0.25	0.45
c	0.15	0.28
D	2.90	3.10
E	2.90	3.10
e	0.65	
H _E	4.70	5.10
L	0.94	
L _p	0.40	0.70
v	0.10	
w	0.10	
y	0.10	
Z	0.35	0.70
θ	0°	6°

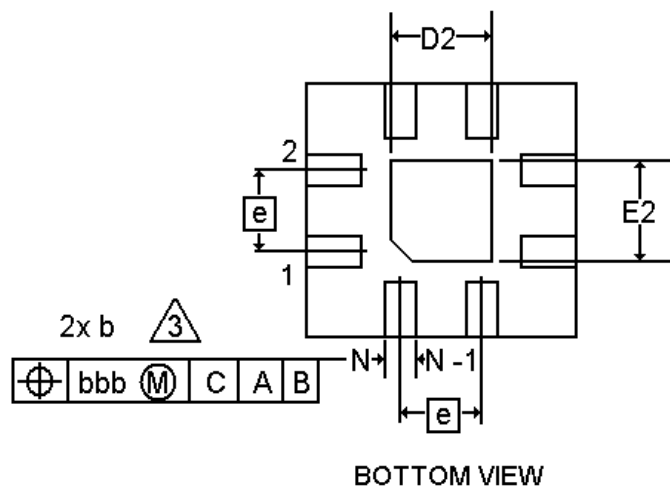
PACKAGE DIAGRAM MLP 8



NOTES

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME T14-1994.
2. THE TERMINAL #1 AND PAD NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012.
3. DIMENSION b APPLIES TO METALLIZED PAD AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM PAD TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.25 REF	
b	0.30	0.35
D	2.90	3.10
D2	1.65	1.95
E	2.90	3.10
E2	1.65	1.95
e	0.65 BSC	
L	0.35	0.45
aaa	0.25	
bbb	0.10	
ccc	0.10	



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