
Lever-Actuated ZIF PGA 603 and 604 Position Sockets

1. SCOPE

1.1. Content

This specification covers performance, tests and quality requirements for the Tyco Electronics 603 and 604 position Zero Insertion Force (ZIF), Micro Pin Grid Array (PGA) surface mounted production sockets. Sockets of this type are of square grid array design which are soldered to a printed circuit board and are intended for use with Intel® Xeon® Processors in the INT2 and INT3 packages. They are zero insertion and removal force sockets which are Single Lever (SL) operated.

1.2. Qualification

When tests are performed on the subject product line, procedures specified in Figure 1 shall be used. All inspections shall be performed using the applicable inspection plan and product drawing.

1.3. Qualification Test Results

Successful qualification testing on the subject product line was completed in Apr02. The Qualification Test Report number for this testing is 501-533. This documentation is on file at and available from Engineering Practices and Standards (EPS).

2. APPLICABLE DOCUMENTS

The following documents form a part of this specification to the extent specified herein. Unless otherwise specified, the latest edition of the document applies. In the event of conflict between the requirements of this specification and the product drawing, the product drawing shall take precedence. In the event of conflict between the requirements of this specification and the referenced documents, this specification shall take precedence.

2.1. Tyco Electronics Documents

- 109-197: AMP Test Specifications vs EIA and IEC Test Methods
- 114-13026: Application Specification
- 408-8407: Instruction Sheet
- 408-8601: Instruction Sheet
- 501-533: Qualification Test Report

2.2. Commercial Standard

EIA-364: Electrical Connector/Socket Test Procedures Including Environmental Classifications

3. REQUIREMENTS

3.1. Design and Construction

Product shall be of the design, construction and physical dimensions specified on the applicable product drawing.

3.2. Materials

Materials used in the construction of this product shall be as specified on the applicable product drawing.

3.3. Ratings

- Voltage: 120 volts AC
- Current: Signal application only, 0.8 ampere maximum per individual contact per Intel prescribed loading
- Temperature:
 - Operating: 0 to 85°C
 - Storage: -55 to 125°C
- Inductance: 4.33 nH maximum
- Capacitance: 1.1 pF maximum

3.4. Performance and Test Description

Product is designed to meet the electrical, mechanical and environmental performance requirements specified in Figure 1. Unless otherwise specified, all tests shall be performed at ambient environmental conditions per EIA-364.

3.5. Test Requirements and Procedures Summary

Test Description	Requirement	Procedure
ELECTRICAL		
Dry circuit resistance.	25 milliohms maximum average per contact.	EIA-364-23. Subject mated specimens to 100 milliamperes maximum and 20 millivolts maximum open circuit voltage. See Figure 3.
MECHANICAL		
Mechanical shock, specified pulse.	See Note.	EIA-364-27, Method A. Subject mated specimens to 50 G's trapezoidal shock pulses of 11 milliseconds duration. 3 shocks in each direction applied along 3 mutually perpendicular planes, 18 total shocks.
Vibration, random.	See Note.	EIA-364-28. Subject mated specimens to 3.13 G's rms between 5-500 Hz. 10 minutes in each of 3 mutually perpendicular planes.
Durability.	See Note.	EIA-364-9. Open and close specimens for 50 cycles using the appropriate package.

Figure 1 (cont)

Test Description	Requirement	Procedure
ENVIRONMENTAL		
Temperature/humidity.	See Note.	EIA-364-31. Subject unmated specimens to 85°C and 85% RH for 2000 hours.
Bake.	See Note.	EIA-364-17. Subject mated specimens to 125°C for 2000 hours.
Temperature cycle condition.	See Note.	EIA364-32. Subject mated specimens to 300 cycles for mPGA603 product, and 200 cycles for mPGA604 product between -55 and 125°C.

NOTE

Shall meet visual requirements, show no physical damage, and meet requirements of additional tests as specified in the Product Qualification and Requalification Test Sequence shown in Figure 2.

Figure 1 (end)

3.6. Product Qualification and Requalification Test Sequence

Test or Examination	Test Group (a)				
	1	2	3	4	5
	Test Sequence (b)				
Dry circuit resistance	1,3	1,3	1,4	1,3	1,3
Mechanical shock			2(c)		
Vibration, random			3(c)		
Durability					2
Temperature/humidity	2				
Bake		2(c)			
Temperature cycle condition				2(c)	

NOTE

- (a) See paragraph 4.1.A.
 (b) Numbers indicate sequence in which tests are performed.
 (c) Socket shall be mated with a mechanical device of the approximate size and mass of the 450 gram heat sink (thermal solution).

Figure 2

4. QUALITY ASSURANCE PROVISIONS

4.1. Qualification Testing

A. Specimen Selection

Specimens shall be prepared in accordance with applicable Instruction Sheets and shall be selected at random from current production. Test groups 1, 2, 3 and 4 shall each consist of 15 specimens of each size (603 and 604 position). Test group 5 shall consist of 10, 604 position specimens.

B. Test Sequence

Qualification inspection shall be verified by testing specimens as specified in Figure 2.

4.2. Requalification Testing

If changes significantly affecting form, fit or function are made to the product or manufacturing process, product assurance shall coordinate requalification testing, consisting of all or part of the original testing sequence as determined by development/product, quality and reliability engineering.

4.3. Acceptance

Acceptance is based on verification that the product meets the requirements of Figure 1. Failures attributed to equipment, test setup or operator deficiencies shall not disqualify the product. If product failure occurs, corrective action shall be taken and specimens resubmitted for qualification. Testing to confirm corrective action is required before resubmittal.

4.4. Quality Conformance Inspection

The applicable quality inspection plan shall specify the sampling acceptable quality level to be used. Dimensional and functional requirements shall be in accordance with the applicable product drawing and this specification.

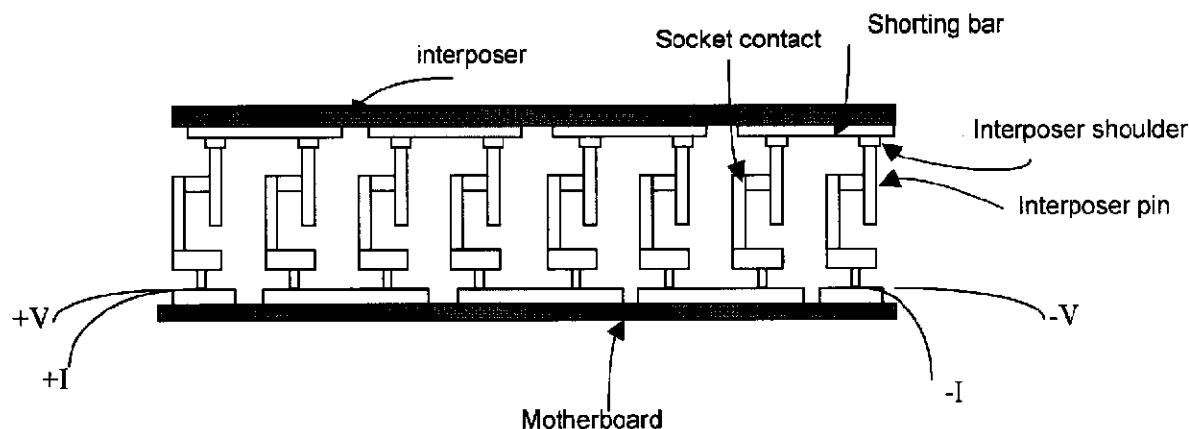


Figure 3
Dry Circuit Resistance Measurement Points