

HD74LS293

4-bit Binary Counter

REJ03D0477-0300

Rev.3.00

Jul.15.2005

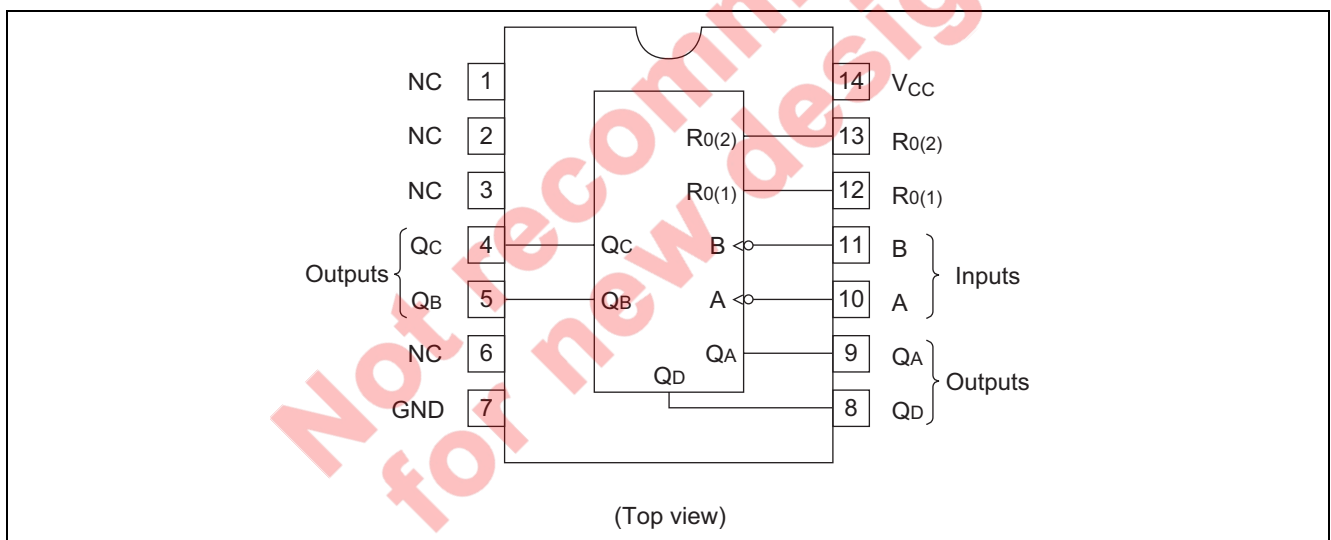
This counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and divide-by-eight counter. This counter has a gated zero reset. To use the maximum count length of this counter, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table.

Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS293P	DILP-14 pin	PRDP0014AB-B (DP-14AV)	P	—

Pin Arrangement



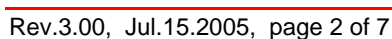
Function Table

Reset / Count

Reset Input		Outputs			
R ₀ (1)	R ₀ (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	L	L	L
L	X	Count			
X	L	Count			

Notes: 1. H; high level, L; low level, X; irrelevant
2. Output Q_A is connected to input B.

Block Diagram



Absolute Maximum Ratings

Item		Symbol	Ratings	Unit
Supply voltage		V_{CC}	7	V
Input voltage	R_0 Inputs	V_{IN}	7	V
	A, B Inputs		5.5	V
Power dissipation		P_T	400	mW
Operating temperature		T_{opr}	-20 to +75	°C
Storage temperature		T_{stg}	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}	—	—	-400	μA
		I_{OL}	—	—	8	mA
Operating temperature		T_{opr}	-20	25	75	°C
Count frequency	A input	f_{count}	0	—	32	MHz
	B input		0	—	16	
Pulse width	A input	t_w	15	—	—	ns
	B input		30	—	—	
	Reset inputs		15	—	—	
Setup time		t_{su}	25	—	—	ns

Electrical Characteristics

($T_a = -20$ to $+75$ °C)

Item		Symbol	min.	typ.*	max.	Unit	Condition	
Input voltage		V_{IH}	2.0	—	—	V		
		V_{IL}	—	—	0.8	V		
Output voltage		V_{OH}	2.7	—	—	V	$V_{CC} = 4.75\text{ V}$, $V_{IH} = 2\text{ V}$, $V_{IL} = 0.8\text{ V}$, $I_{OH} = -400\text{ }\mu\text{A}$	
		V_{OL}	—	—	0.4	V	$I_{OL} = 4\text{ mA}^{**}$	$V_{CC} = 4.75\text{ V}$, $V_{IH} = 2\text{ V}$, $V_{IL} = 0.8\text{ V}$
—	—		0.5	$I_{OL} = 8\text{ mA}^{**}$				
Input current	Any Reset	I_{IH}	—	—	20	μA	$V_{CC} = 5.25\text{ V}$, $V_I = 2.7\text{ V}$	
	A input		—	—	40			
	B input		—	—	40			
	Any Reset	I_{IL}	—	—	-0.4	mA	$V_{CC} = 5.25\text{ V}$, $V_I = 0.4\text{ V}$	
	A input		—	—	-2.4			
	B input		—	—	-1.6			
	Any Reset	I_I	—	—	0.1	mA	$V_I = 7\text{ V}$	$V_{CC} = 5.25\text{ V}$
	A input		—	—	0.2		$V_I = 5.5\text{ V}$	
	B input		—	—	0.2			
Short-circuit output current		I_{OS}	-20	—	-100	mA	$V_{CC} = 5.25\text{ V}$	
Supply current***		I_{CC}	—	9	15	mA	$V_{CC} = 5.25\text{ V}$	
Input clamp voltage		V_{IK}	—	—	-1.5	V	$V_{CC} = 4.75\text{ V}$, $I_{IN} = -18\text{ mA}$	

Notes: * $V_{CC} = 5$ V, $T_a = 25$ °C

** Q_A output is tested at specified I_{OL} plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

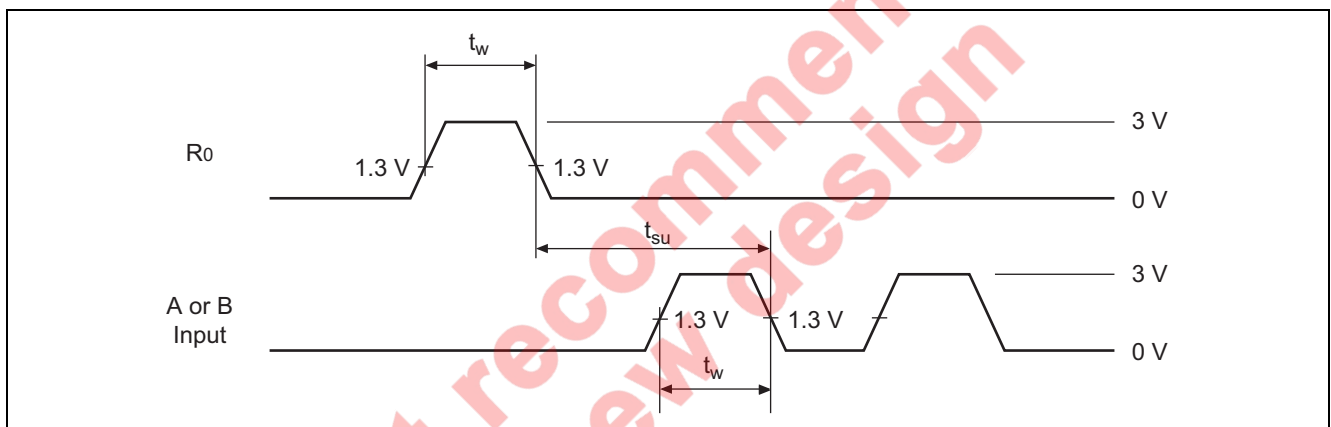
*** I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

Switching Characteristics

(V_{CC} = 5 V, T_a = 25°C)

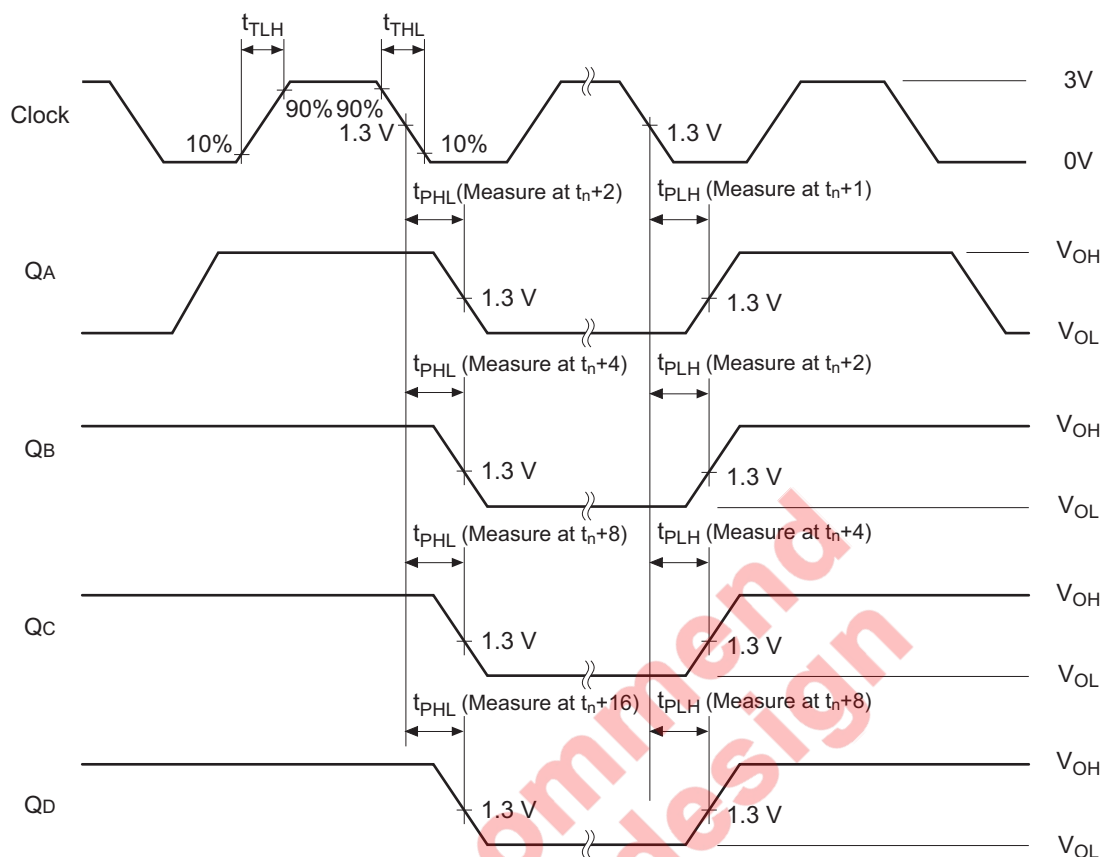
Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum count frequency	f_{\max}	A	Q _A	32	42	—	MHz	C _L = 15 pF, R _L = 2 kΩ
		B	Q _B	16	—	—		
Propagation delay time	t _{PLH}	A	Q _A	—	10	16	ns	
	t _{PHL}			—	12	18		
	t _{PLH}	A	Q _D	—	46	70	ns	
	t _{PHL}			—	46	70		
	t _{PLH}	B	Q _B	—	10	16	ns	
	t _{PHL}			—	14	21		
	t _{PLH}	B	Q _C	—	21	32	ns	
	t _{PHL}			—	23	35		
	t _{PLH}	B	Q _D	—	34	51	ns	
	t _{PHL}			—	34	51		
t _{PHL}	Set-to-0	Q _A to Q _D	—	26	40	ns		

Timing Method



Waveforms 1

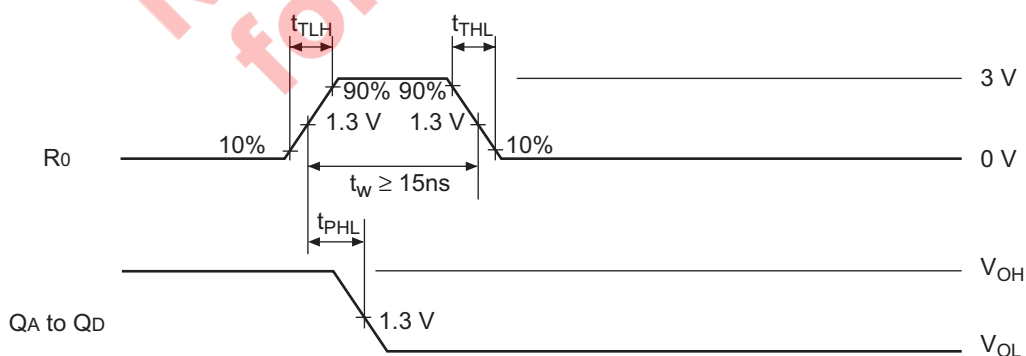
f_{max} , t_{PLH} , t_{PHL} , (Clock→Q)



- Notes:
1. Clock input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz, duty cycle = 50% and : for f_{max} , $t_{TLH} = t_{THL} \leq 2.5$ ns.
 2. t_n is reference bit time when all outputs are low.

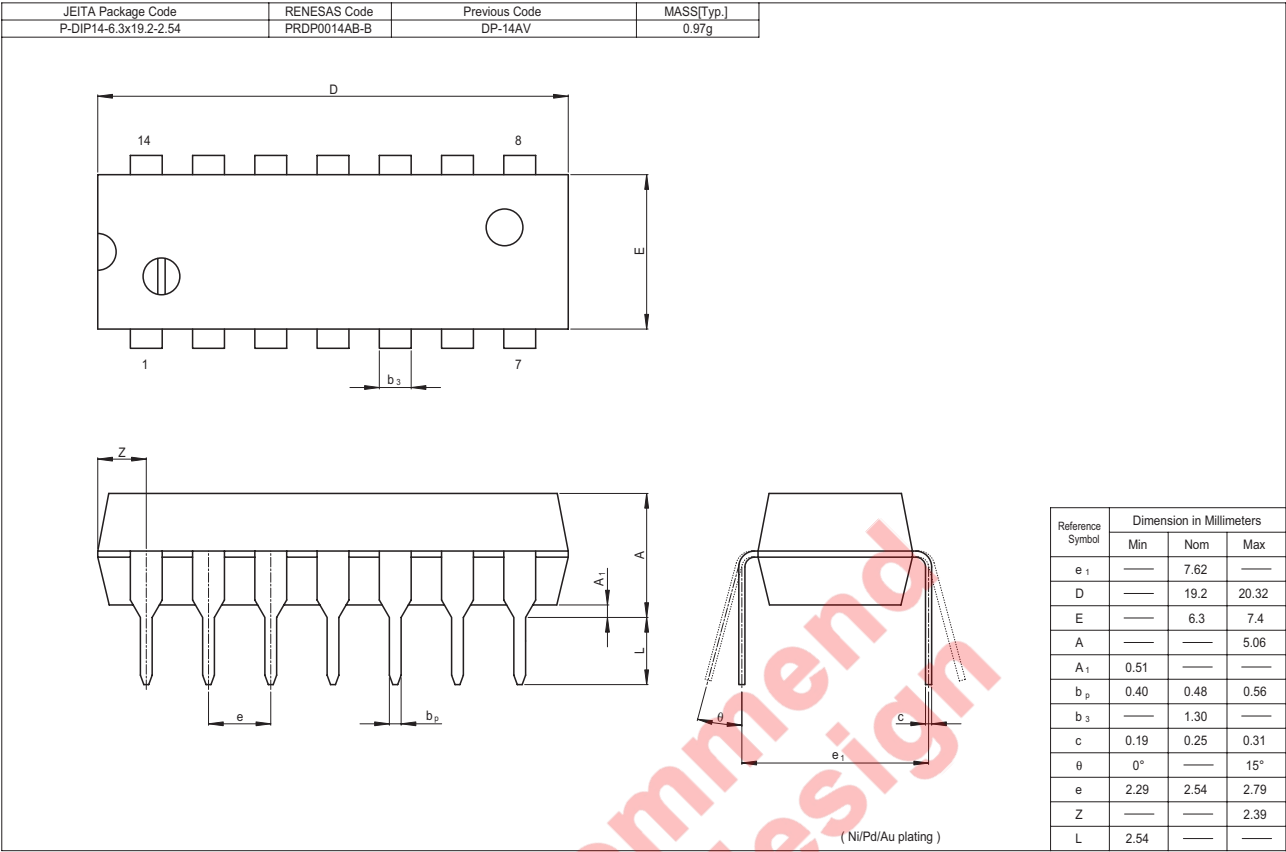
Waveforms 2

t_{PHL} , ($R_0 \rightarrow Q$)



Note: $t_{TLH} \leq 15$ ns, $t_{THL} \leq 5$ ns

Package Dimensions



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