Low Voltage / Low Power CMOS 16-bit Micro-controller

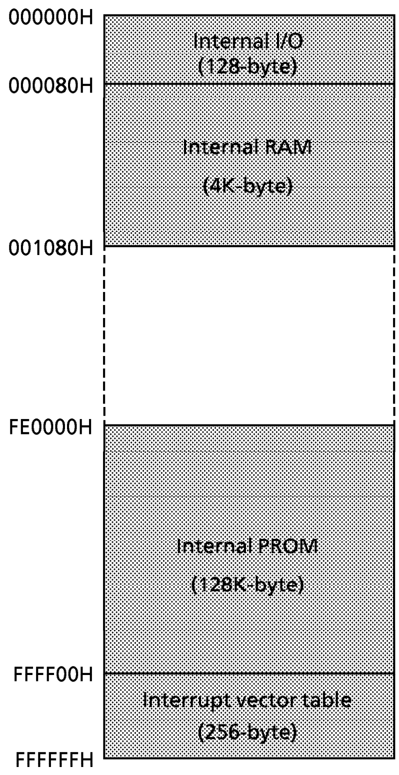
TMP93PW32F

1. OUTLINE AND DEVICE CHARACTERISTICS

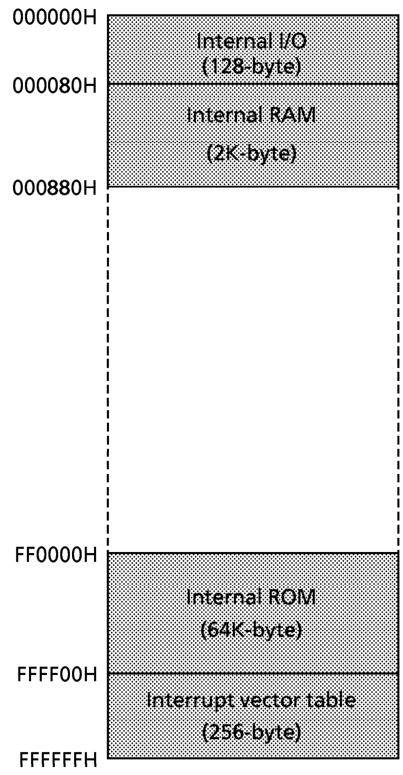
The TMP93PW32 is OTP type MCU which includes 128K byte One-time PROM. Using the adapter-socket (BM11132), you can write and verify the data for the TMP93PW32. The TMP93PW32F has the same pin-assignment as TMP93CS32 (Mask ROM type).

Writing the program to Built-in PROM, the TMP93PW32 operates as the same way as the TMP93CS32.

The memory map and capacity of built in ROM and RAM are different between TMP93CS32 and TMP93PW32. The TMP93PW32 has the PROM of 128K-byte and the RAM of 4K-byte, and the TMP93CS32 has the ROM of 64K-byte and the RAM of 2K-byte. Following figure shows each memory map.

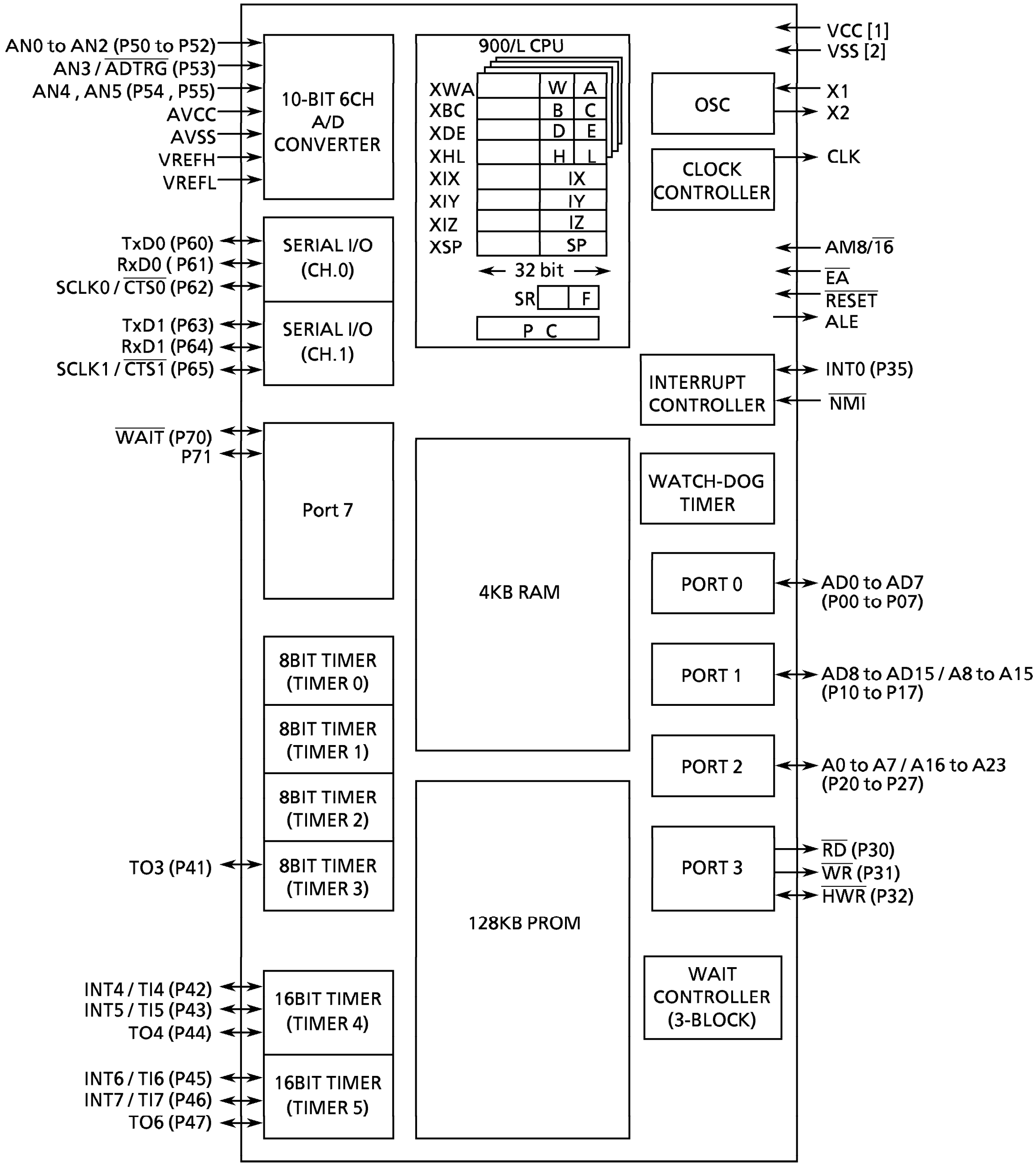


TMP93PW32 memory map



TMP93CS32 memory map

MCU	ROM	RAM	Package	Adapter Socket
TMP93PW32F	OTP 128K-byte	4K-byte	64-QFP	BM11132



Note : The items in parentheses ( ) are the initial setting after reset.

Figure 1 TMP93PW32 block diagram

2. PIN ASSIGNMENT AND FUNCTIONS

The assignment of input / output pins for the TMP93PW32, their names and functions are described below.

2.1 Pin Assignment

Figure 2.1 shows pin assignment of the TMP93PW32F.

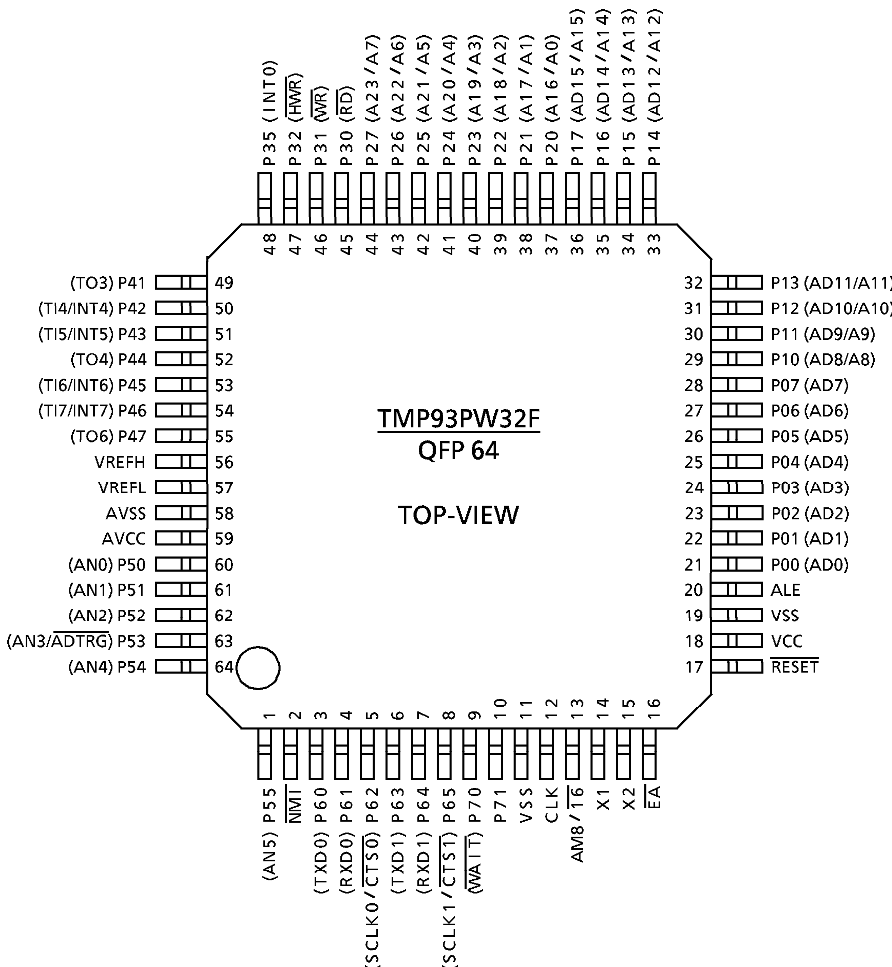


Figure 2.1 Pin Assignment (64-pin QFP)

2.2 Pin Names and Functions

The TMP93PW32 has MCU mode and PROM mode.

(1) Table 2.2 (1) shows pin function of TMP93PW32 in MCU mode.

Table 2.2 (1) Pin Names and Function (1/3)

Pin name	Number of pins	I/O	Functions
P00 to P07	8	I/O	Port 0: I/O port that allows selection of I/O on a bit basis
/ AD0 to AD7		3-state	Address/data (lower): Bits 0 to 7 for address/data bus
P10 to P17	8	I/O	Port 1: I/O port that allows selection of I/O on a bit basis
/ AD8 to AD15		3-state	Address data (upper): Bits 8 to 15 for address/data bus
/ A8 to A15		Output	Address: Bits 8 to 15 for address bus
P20 to P27	8	I/O	Port 2: I/O port that allows selection of I/O on a bit basis (with pull-up resistor)
/ A0 to A7		Output	Address: Bits 0 to 7 for address bus
/ A16 to A23		Output	Address: Bits 16 to 23 for address bus
P30	1	Output	Port 30: Output port
/ $\overline{RD}$		Output	Read: Strobe signal for reading external memory
P31	1	Output	Port 31: Output port
/ $\overline{WR}$		Output	Write: Strobe signal for writing data on pins AD0 to 7
P32	1	I/O	Port 32: I/O port (with pull-up resistor)
/ $\overline{HWR}$		Output	High write: Strobe signal for writing data on pins AD8 to 15
P35	1	I/O	Port 35: I/O port
/ INT0		Input	Interrupt request pin 0: Interrupt request pin with programmable level/rising edge
P41	1	I/O	Port 41: I/O port
/ TO3		Output	PWM output 3: 8-bit PWM timer 3 output
P42	1	I/O	Port 42: I/O port
/ TI4		Input	Timer input 4: Timer 4 count / capture trigger signal input
/ INT4		Input	Interrupt request pin 4: Interrupt request pin with programmable rising / falling edge
P43	1	I/O	Port 43: I/O port
/ TI5		Input	Timer input 5: Timer 4 count / capture trigger signal input
/ INT5		Input	Interrupt request pin 5: Interrupt request pin with rising edge
P44	1	I/O	Port 44: I/O port
/ TO4		Output	Timer output 4: Timer 4 output pin

Table 2.2 (1) Pin Names and Function (2/3)

Pin name	Number of pins	I/O	Functions
P45	1	I/O	Port 45: I/O port
/ TI6		Input	Timer input 6: Timer 5 count / capture trigger signal input
/ INT6		Input	Interrupt request pin 6: Interrupt request pin with programmable rising / falling edge
P46	1	I/O	Port 46: I/O port
/ TI7		Input	Timer input 7: Timer 5 count / capture trigger signal input
/ INT7		Input	Interrupt request pin 7: Interrupt request pin with rising edge
P47	1	I/O	Port 47: I/O port
/ TO6		Output	Timer output 6: Timer 5 output pin
P50 to P52, P54, P55	5	Input	Port 50 to Port 52, Port 54, Port 55: Input port
/ AN0 to AN2, AN4, AN5		Input	Analog input: Analog signal input for A/D converter
P53	1	Input	Port53: Input Port
/ AN3		Input	Analog input: Analog signal input for A/D converter
/ $\overline{\text{ADTRG}}$		Input	A/D converter external start trigger input
P60	1	I/O	Port 60: I/O port (with pull-up resistor)
/ TXD0		Output	Serial send data 0
P61	1	I/O	Port 61: I/O port (with pull-up resistor)
/ RXD0		Input	Serial receive data 0
P62	1	I/O	Port 62: I/O port (with pull-up resistor)
/ $\overline{\text{CTS0}}$		Input	Serial data send enable 0 (Clear to Send)
/ SCLK0		I/O	Serial Clock I/O 0
P63	1	I/O	Port 63: I/O port (with pull-up resistor)
/ TXD1		Output	Serial send data 1
P64	1	I/O	Port 64: I/O port (with pull-up resistor)
/ RXD1		Input	Serial receive data 1
P65	1	I/O	Port 65: I/O port (with pull-up resistor)
/ $\overline{\text{CTS1}}$		Input	Serial data send enable 1 (Clear to Send)
/ SCLK1		I/O	Serial clock I/O 1
P70	1	I/O	Port 70: I/O port (High current output available)
/ $\overline{\text{WAIT}}$		Input	WAIT: Pin used to request CPU bus wait
P71	1	I/O	Port 71: I/O port (High current output available)
$\overline{\text{NMI}}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with falling edge. Can also be operated at falling and rising edges by program.
CLK	1	Output	Clock output: Outputs "$f_{SYS} \div 2$" Clock. Pulled-up during reset. Can be disabled for reducing noise.
$\overline{\text{EA}}$	1	Input	External access: "1" should be inputted with TMP93PW32.

Table 2.2 (1) Pin Names and Function (3/3)

Pin name	Number of pins	I/O	Functions
AM8 / $\overline{16}$	1	Input	Address Mode: Selects external Data Bus width. "1" should be inputted. The Data Bus Width for external access is set by Chip Select / WAIT Control register, Port 1 Control register.
ALE	1	Output	Address Latch Enable Can be disabled for reducing noise.
$\overline{\text{RESET}}$	1	Input	Reset: Initializes TMP93PW32. (With pull-up resistor)
VREFH	1	Input	Pin for high level reference voltage input to A/D converter
VREFL	1	Input	Pin for low level reference voltage input to A/D converter
AVCC	1	Input	Power supply pin for A/D converter
AVSS	1	Input	GND pin for A/D converter (0 V)
X1	1	Input	Oscillator connecting pin
X2	1	Output	Oscillator connecting pin
VCC	1	Input	Power supply pin
VSS	2	Input	GND pin (All VSS pins are connected to the GND (0V).))

Note : Built-in pull-up resistors can be released from the pins other than the $\overline{\text{RESET}}$ pin by software.

(2) PROM mode

Table 2.2 (2) shows pin function of the TMP93PW32 in PROM mode.

Table 2.2 (2) Pin Name and function of PROM mode

Pin function	Number of pins	Input / Output	Function	Pin name (MCU mode)
A7 to A0	8	Input	Memory address of program	P27 to P20
A15 to A8	8	Input	Memory address of program	P17 to P10
A16	1	Input	Memory address of program	P71
D7 to D0	8	I/O	Memory data of program	P07 to P00
$\overline{CE}$	1	Input	Chip enable	P32
$\overline{OE}$	1	Input	Output control	P30
$\overline{PGM}$	1	Input	Program control	P31
VPP	1	Power supply	12.75 V / 5 V (Power supply of program)	$\overline{EA}$
VCC	2	Power supply	6.25 V / 5 V	VCC, AVCC
VSS	3	Power supply	0 V	VSS, AVSS

Pin function	Number of pins	Input / Output	Disposal of pin
P60	1	Input	Fix to low level (security pin)
$\overline{RESET}$	1	Input	Fix to low level (PROM mode)
CLK	1	Input	Fix to low level (PROM mode)
ALE	1	Output	Open
X1	1	Input	Self oscillation with resonator
X2	1	Output	Self oscillation with resonator
P65 to P61 AM8 / $\overline{16}$	6	Input	Fix to high level
P35, P47 to P41 P55 to P50 P70 VREFH VREFL $\overline{NMI}$	18	I/O	Open

3. OPERATION

This section describes the functions and basic operational blocks of the TMP93PW32.

The TMP93PW32 has PROM in place of the mask ROM which is included in the TMP93CS32. The other configuration and functions are the same as the TMP93CS32. Regarding the functions of the TMP93PW32 (not described), see the part of TMP93CS32.

The TMP93PW32 has two operational modes : MCU mode and PROM mode.

3.1 MCU mode

(1) Mode-setting and function

The MCU mode is set by opening the CLK pin (pin open). In the MCU mode, the operation is same as TMP93CS32 except the followings.

(2) Memory-map

The memory map of TMP93PW32 is not same as that of TMP93CS32. Figure 3.1 (1) shows the memory map in MCU mode. Figure 3.1 (2) show that in PROM mode.

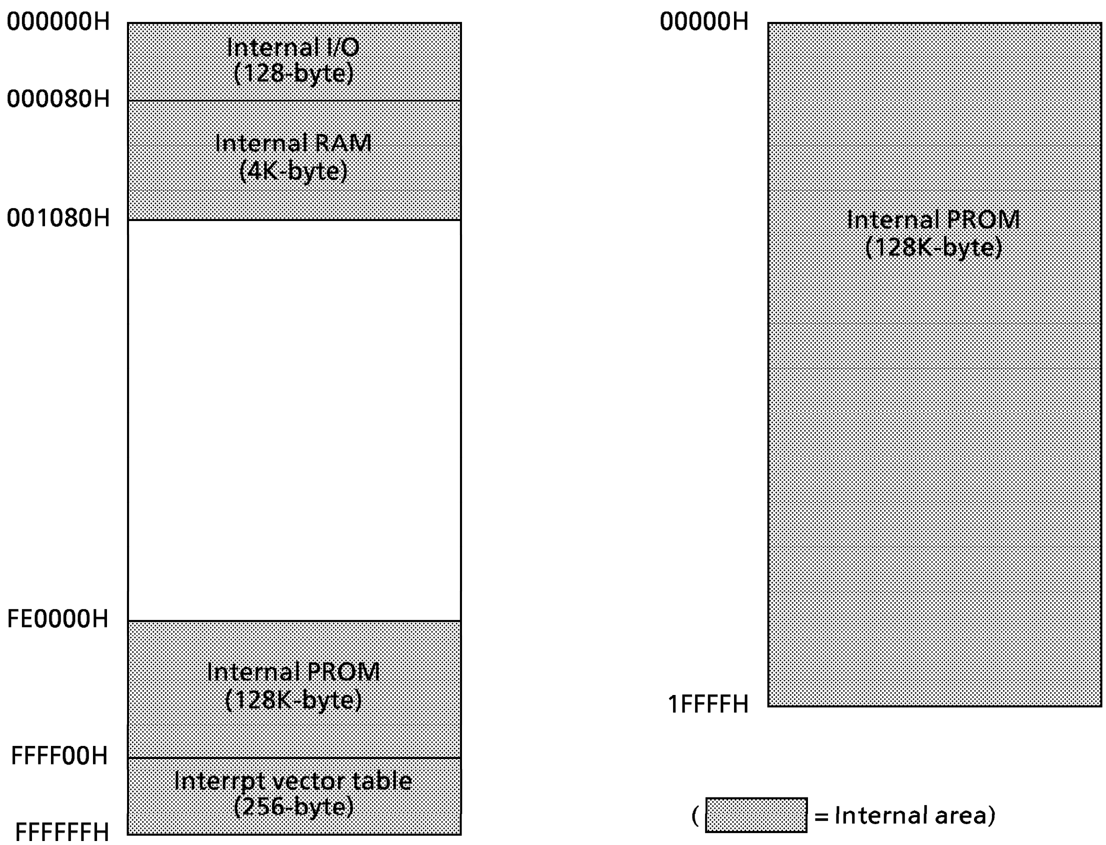


Figure 3.1 (1) Memory map in MCU mode Figure 3.1 (2) Memory map in PROM mode

(3) Care point of chip select / wait controller

The built in RAM capacity of the TMP93PW32 is larger than that of the TMP93CS32, therefor the following point is different about the accessing area of WAITC1.

Setting WAITC1<B1C1-0> to “00”

TMP93PW32	TMP93CS32
1080H to 7FFFH	880 to7FFFH

WAITC0 and WAITC2 addressing area are the same as TMP93CS32.

3.2 PROM Mode

(1) Mode setting and Function

PROM mode is set by setting the $\overline{RESET}$ and CLK pins to the "L" level. The programming and verification for the internal PROM is achieved by using a general EPROM programmer with the adaptor socket.

① Preparation of OTP adaptor
BM11132 : for TMP93PW32

② Setting of OTP adaptor
The switch (SW1) is set to N side.

③ Setting of PROM writer

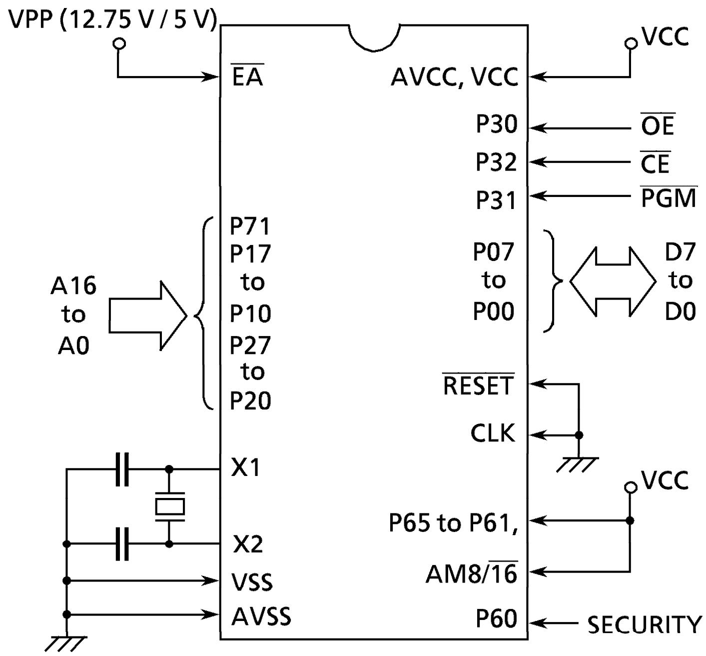
i) Set PROM type to TC 571000D.
Size : 1 Mbyte
VPP : 12.75 V
t_{PW} : 100 μs
Electric Signature mode : none

ii) Data transmittion
In TMP93PW32F, PROM is placed on addresses 00000 to 1FFFFH in PROM mode, and addresses FE0000H to FFFFFFH in MCU mode. Therefore data should be transferred to addresses 00000 to 1FFFFH in PROM mode using the object converter (tuconv) or the block transfer mode (see instruction manual of PROM programmer.)

iii) Setting of the program address
Start address : 00000H
End address : 1FFFFH

④ Programming
Program and verify according to operating process of PROM programmer.
Figure 3.2 (1) shows the setting of the pins in PROM mode.

Figure 3.2 (1) shows the setting of pins in PROM mode.



For other pins, refer to the section on pin functions (Table 2.2 (2)).

※ Use the 10 MHz resonator in case of programming and verification by a general PROM programmer.

Figure 3.2 (1) PROM Mode Pin Setting

(2) Caution for Electric Signature

The TMP93PW32 dose not support the electric signature mode (hereinafter referred to as "signature"). If PROM programmer used the signature, the device would be damaged because of applying voltage of 12±0.5V to pin 9 (A9) of the address.

Please use without setting the signature.

(3) Program Mode

All bits of the TMP93PW32 are "1" when delivered (the erase state). Data "0" is written in the necessary bit location during program operating.

Writing function can be operated at VPP=12.5 V, $\overline{OE}=V_{IH}$, $\overline{CE}$-$=V_{IL}$. Built-in one time PROM can be written in any sequence. It is possible to write only special address.

(4) Adopter Socket (BM11132)

BM11132 is the adapter sockets to write data into the TMP93PW32F. The TMP93PW32F has built-in one time PROM using a general EPROM programmer.

(5) Program Storing Area of PROM Mode

The TMP93PW32 has the program space (FE0000H to FFFFFFH) of 128 K bytes. The address 00000H to 1FFFFH of PROM mode equals to the address FE0000H to FFFFFFH of MCU mode.

(6) Program Write Setting Method Using a general EPROM programmer

PROM to be prepared should equal to TC571000D functions.

1. Set the switch (SW1) of BM11132 (hereinafter referred to as “adapter”) to the program side (NOR). (Note1)
2. Connect MCU to the adapter. (Note2)
3. Connect the adapter to PROM programmer. (Note2)
4. Set the PROM type of PROM programmer to TC571000D.
5. Set the start address for writing PROM to 00000H, and the end address to 1FFFFH. (Note 3)
6. Writing to built-in one time PROM and verifying should be operated according to the operation procedures of PROM programmer.

Note 1 : If data is written to built-in one time PROM without setting the switch (SW1) to the program side, the device would be damaged.

Note 2 : Please set with the first pin of the adapter and that of PROM programmer socket matched. If the first pin is conversely set, MCU or programmer would be damaged.

Note 3 : If data “0” is written to the address which is over 1FFFFH, the contents of the original program would be damaged because of writing “0” to the addresses 00000H to 1FFFFH.

(7) Programming Flow Chart

The programming mode is set by applying 12.75 V (programming voltage) to the VPP pin when the following pins are set as follows,
(VCC : 6.25 V, $\overline{\text{RESET}}$: "L" level, CLK : "L" level).

While address and data are fixed and $\overline{\text{CE}}$ pin is set to "L" level, 0.1 ms of "L" level pulse is applied to $\overline{\text{PGM}}$ pin to program the data.

Then the data in the address is verified.

If the programmed data is incorrect, another 0.1 ms pulse is applied to $\overline{\text{PGM}}$ pin.

This programming procedure is repeated until correct data is read from the address. (25 times maximum)

Subsequently, all data are programmed in all addresses.

The verification for all data is done under the condition of $V_{PP} = V_{CC} = 5V$ after all data were written.

Figure 3.2 (2) shows the programming flow chart.

High Speed Program Writing.

Flow chart

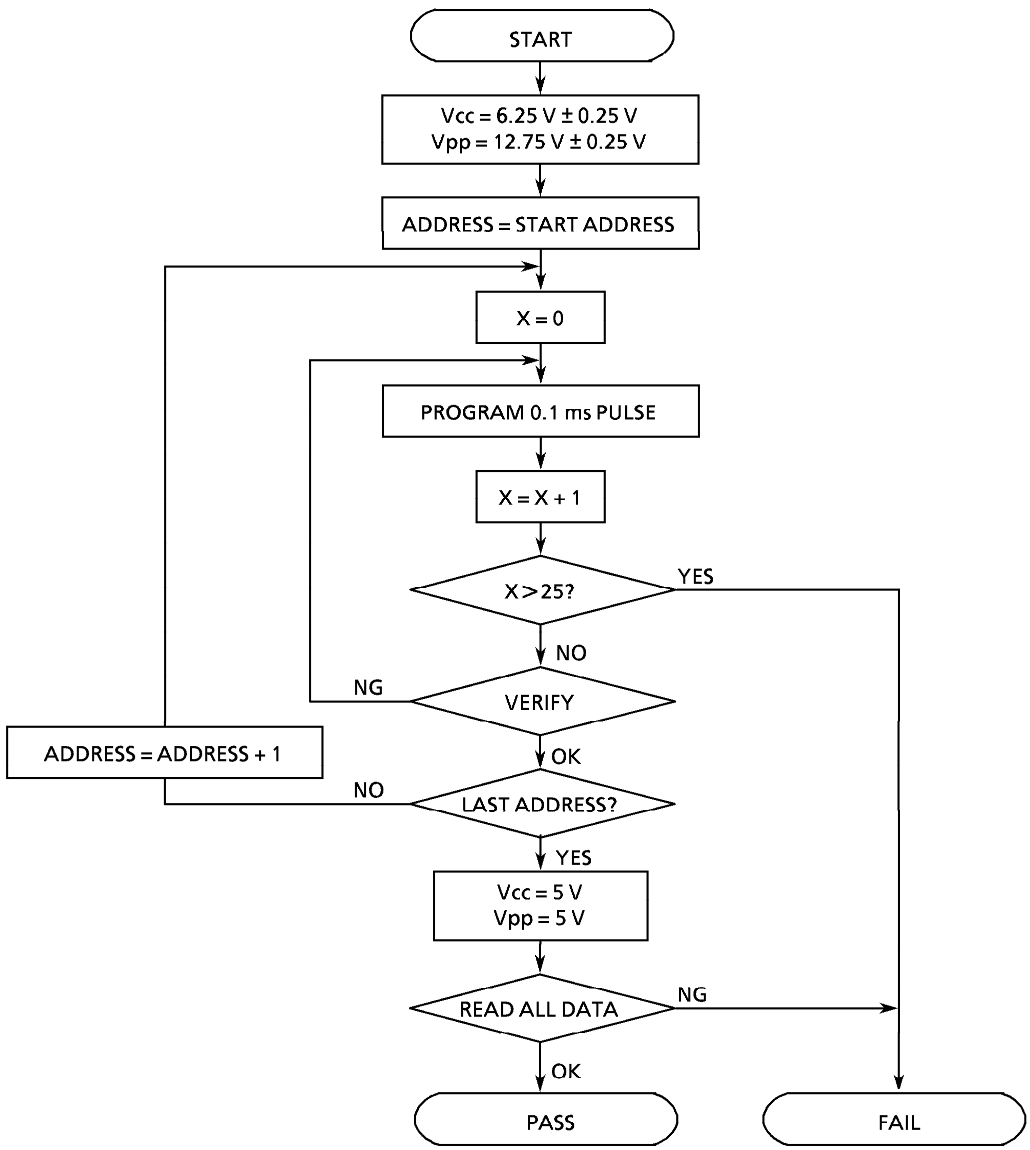


Figure 3.2 (2) Flow chart

(8) Security Bit

The TMP93PW32 has a Security Bit in PROM cell.
If the Security Bit is programmed to “0”, the content of the PROM is disable to be read (FFH data) in PROM mode.

(How to program the Security Bit.)

The difference from the programming procedures described in section 3.2 (1) are follows.

① Setting OTP adaptor
Set the switch (SW1) to S side.

② Setting PROM programmer

i) Transferring the data

ii) Setting of programming address

The security bit is in bit 0 of address 00000H.
Set the start address 00000H and the end address 00000H.
Set the data FEH at the address 00000H.

4. ELECTRICAL CHARACTERISTICS (PRELIMINARY)

"X" used in an expression shows a cycle of clock f_{FPH}. If a clock gear or a low speed oscillator is selected, a value of "X" is different. The value as an example is gear = 1/fc (SYSCR1<GEAR 2 to 0> = "000").

4.1 Absolute Maximum Ratings (TMP93PW32)

Symbol	Parameter	Rating		Unit
Vcc	Power Supply Voltage	− 0.5 to 6.5		V
V_{IN}	Input Voltage	except $\overline{EA}$ pin	− 0.5 to Vcc + 0.5	V
		$\overline{EA}$ pin	− 0.5 to 14.0	
I_{OL1}	Output current (Per 1 pin) P7	20		mA
I_{OL2}	Output current (Per 1 pin) except P7	2		mA
ΣI_{OL}	Output Current (total)	120		mA
ΣI_{OH}	Output Current (total)	− 80		mA
P_D	Power Dissipation (Ta = 85 ℃)	350		mW
T_{SOLDER}	Soldering Temperature (10 s)	260		℃
T_{STG}	Storage Temperature	− 65 to 150		℃
T_{OPR}	Operating Temperature	− 40 to 85		℃

4.2 DC Characteristics (1/2)

Ta = − 40 to 85°C

Symbol	Parameter		Min	Typ. (Note1)	Max	Unit	Condition
Vcc	Power Supply Voltage (AVcc = Vcc, AVss = Vss = 0 V)		4.5		5.5	V	fc = 4 to 20 MHz
			2.7				fc = 4 to 12.5 MHz (− 20 ≦ Ta ≦ 70°C) fc = 4 to 10 MHz (− 40 ≦ Ta ≦ 85°C)
V_{IL}	Input Low Voltage	AD0 to 15	− 0.3		0.8	V	Vcc ≧ 4.5V
					0.6		Vcc < 4.5V
V_{IL1}		Port2 to 7 (except P35)			0.3Vcc		Vcc = 2.7 to 5.5V
V_{IL2}		$\overline{RESET}$, $\overline{NMI}$, INT0			0.25Vcc		
V_{IL3}		$\overline{EA}$, AM8/$\overline{16}$			0.3		
V_{IL4}		X1			0.2Vcc		
V_{IH}	Input High Voltage	AD0 to 15	2.2		Vcc + 0.3		Vcc ≧ 4.5V
			2.0				Vcc < 4.5V
V_{IH1}		Port2 to 7 (except P35)	0.7Vcc				Vcc = 2.7 to 5.5V
V_{IH2}		$\overline{RESET}$, $\overline{NMI}$, INT0	0.75Vcc				
V_{IH3}		$\overline{EA}$, AM8/$\overline{16}$	Vcc − 0.3				
V_{IH4}		X1	0.8Vcc				
V_{OL}	Output Low Voltage				0.45	V	I_{OL} = 1.6 mA (Vcc = 2.7 to 5.5V)
I_{OL7}	Output Low current (P7)		16			mA	V_{OL} = 1.0V (Vcc = 5V ± 10 %)
			7				(Vcc = 3V ± 10 %)
V_{OH1}	Output High Voltage		2.4			V	I_{OH} = − 400 μA (Vcc = 3V ± 10 %)
V_{OH2}			4.2			V	I_{OH} = − 400 μA (Vcc = 5V ± 10 %)

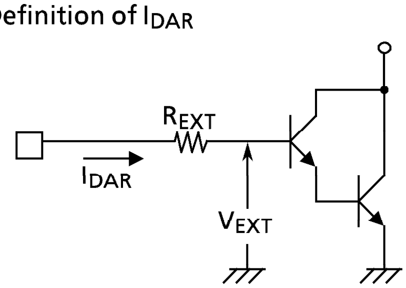
Note 1 : Typical values are for Ta = 25 °C and V_{CC} = 5 V unless otherwise noted.

4.2 DC Characteristics (2/2)

Symbol	Parameter	Min	Typ.(Note1)	Max	Unit	Condition	
I_{DAR} (Note2)	Darlington Drive Current (8 Output Pins max.)	−1.0		−3.5	mA	V_{EXT} = 1.5 V, R_{EXT} = 1.1 kΩ (Vcc = 5 V ± 10 % only)	
I_{LI}	Input Leakage Current		0.02	± 5	μA	$0.0 \leqq V_{IN} \leqq V_{CC}$	
I_{LO}	Output Leakage Current		0.05	± 10	μA	$0.2 \leqq V_{IN} \leqq V_{CC} - 0.2$	
V_{STOP}	Power Down Voltage (at STOP, RAM Back up)	2.0		6.0	V	V_{IL2} = 0.2 Vcc, V_{IH2} = 0.8 Vcc	
R_{PU}	Pull Up Resistance	45		130	kΩ	Vcc = 5.5 V	
		50		160		Vcc = 4.5 V	
		70		280		Vcc = 3.3 V	
		90		400		Vcc = 2.7 V	
C_{IO}	Pin Capacitance			10	pF	fc = 1 MHz	
V_{TH}	Schmitt Width $\overline{RESET}$, $\overline{NMI}$, INT0	0.4	1.0		V		
Icc	NORMAL (Note3)		25	30	mA	Vcc = 5 V ± 10 % fc = 20 MHz	
	RUN		22	27			
	IDLE2		13	17			
	IDLE1		3.4	5			
	NORMAL (Note3)		8.0	11		Vcc = 3 V ± 10 % fc = 12.5 MHz (Typ. : Vcc = 3.0 V)	
	RUN		7.0	10			
	IDLE2		4.2	6			
	IDLE1		1.2	1.8			
	STOP		0.2	10	μA	Ta ≦ 50 °C	Vcc = 2.7 V to 5.5 V
				20		Ta ≦ 70 °C	
				50		Ta ≦ 85 °C	

Note 1 : Typical values are for Ta = 25 °C and V_{CC} = 5 V unless otherwise noted.
Note 2 : I_{DAR} is guranteed for total of up to 8 ports.
Note 3 : I_{CC} measurement conditions (NORMAL, SLOW) :
Only CPU is operational ; output pins are open and input pins are fixed.

(Reference) Definition of I_{DAR}



4.3 AC Electrical Characteristics

(1) Vcc = 5 V ± 10 %

No.	Symbol	Parameter	Variable		16 MHz		20 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	t_{OSC}	Osc. Period (= x)	50	250	62.5		50		ns
2	t_{CLK}	CLK width	2x – 40		85		60		ns
3	t_{AK}	A0 to 23 Valid→CLK Hold	0.5x – 20		11		5		ns
4	t_{KA}	CLK Valid→A0 to 23 Hold	1.5x – 70		24		5		ns
5	t_{AL}	A0 to 15 Valid→ALE fall	0.5x – 15		16		10		ns
6	t_{LA}	ALE fall→A0 to 15 Hold	0.5x – 20		11		5		ns
7	t_{LL}	ALE High width	x – 40		23		10		ns
8	t_{LC}	ALE fall→$\overline{RD}$/$\overline{WR}$ fall	0.5x – 25		6		0		ns
9	t_{CL}	$\overline{RD}$/$\overline{WR}$ rise→ALE rise	0.5x – 20		11		5		ns
10	t_{ACL}	A0 to 15 Valid→$\overline{RD}$/$\overline{WR}$ fall	x – 25		38		25		ns
11	t_{ACH}	A0 to 23 Valid→$\overline{RD}$/$\overline{WR}$ fall	1.5x – 50		44		25		ns
12	t_{CA}	$\overline{RD}$/$\overline{WR}$ rise→A0 to 23 Hold	0.5x – 25		6		0		ns
13	t_{ADL}	A0 to 15 Valid→D0 to 15 input		3.0x – 55		133		95	ns
14	t_{ADH}	A0 to 23 Valid→D0 to 15 input		3.5x – 65		154		110	ns
15	t_{RD}	$\overline{RD}$fall →D0 to 15 input		2.0x – 60		65		40	ns
16	t_{RR}	$\overline{RD}$ Low pulse width	2.0x – 40		85		60		ns
17	t_{HR}	$\overline{RD}$rise→D0 to 15 Hold	0		0		0		ns
18	t_{RAE}	$\overline{RD}$rise→A0 to 15output	x – 15		48		35		ns
19	t_{WW}	$\overline{WR}$ Low pulse width	2.0x – 40		85		60		ns
20	t_{DW}	D0 to 15 Valid→$\overline{WR}$ rise	2.0x – 55		70		45		ns
21	t_{WD}	$\overline{WR}$ rise →D0 to 15 Hold	0.5x – 15		16		10		ns
22	t_{AWH}	A0 to 23 Valid→$\overline{WAIT}$ input (1 WAIT + n mode)		3.5x – 90		129		85	ns
23	t_{AWL}	A0 to 15 Valid→$\overline{WAIT}$ input (1 WAIT + n mode)		3.0x – 80		108		70	ns
24	t_{CW}	$\overline{RD}$/$\overline{WR}$ fall→$\overline{WAIT}$ Hold (1 WAIT + n mode)	2.0x + 0		125		100		ns
25	t_{APH}	A0 to 23 Valid→PORT input		2.5x – 120		36		5	ns
26	t_{APH2}	A0 to 23 Valid→PORT Hold	2.5x + 50		206		175		ns
27	t_{CP}	$\overline{WR}$ rise→PORT Valid		200		200		200	ns

AC Measuring Conditions

- Output Level : High 2.2 V / Low 0.8 V , CL = 50 pF
  (However CL = 100 pF for AD0 to AD15, A0 to A23, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, CLK)
- Input Level : High 2.4 V / Low 0.45 V (AD0 to AD15)
  High 0.8 Vcc / Low 0.2 Vcc(Except for AD0 to AD15)

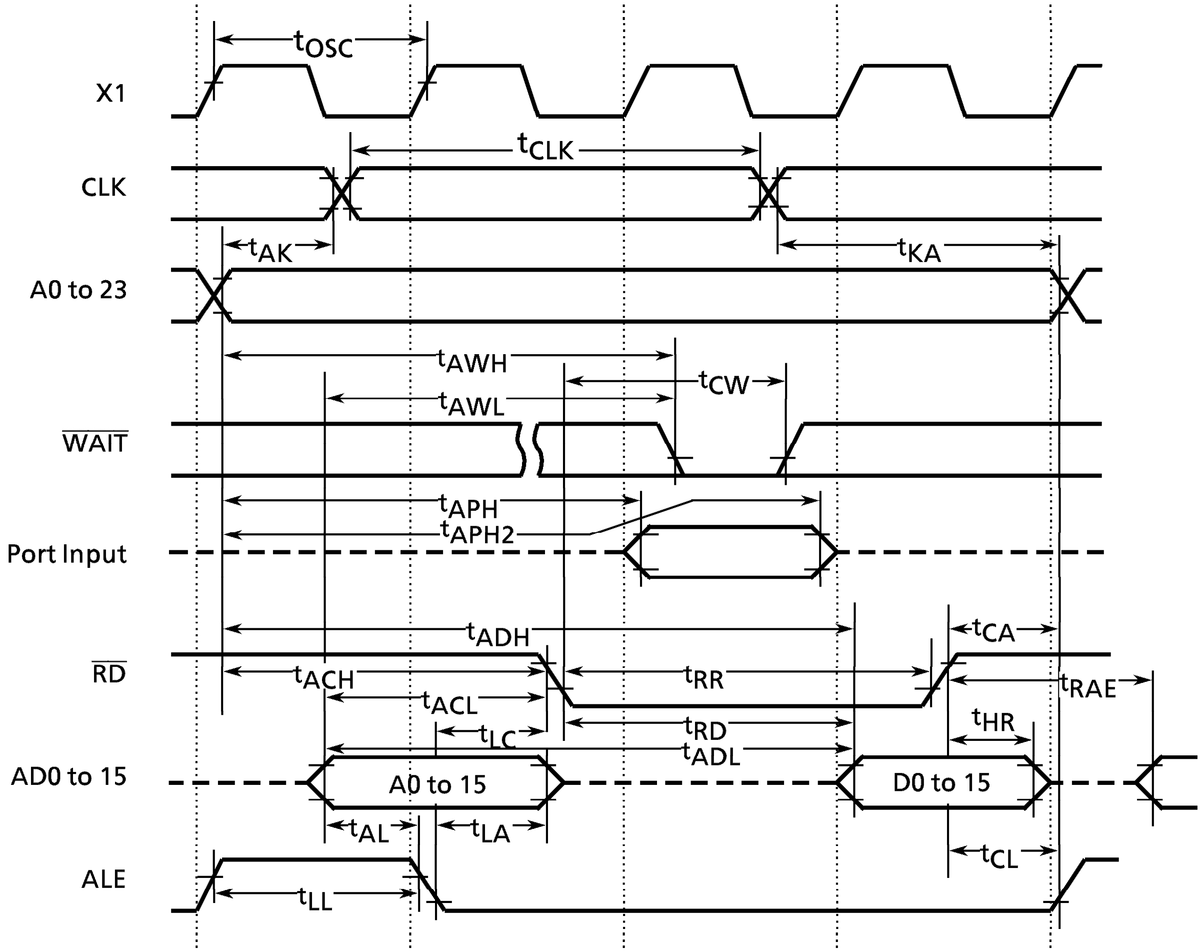
(2) Vcc = 3 V ± 10 %

No.	Symbol	Parameter	Variable		12.5 MHz		Unit
			Min	Max	Min	Max	
1	t_{OSC}	Osc. Period (= x)	80	250	80		ns
2	t_{CLK}	CLK width	2x – 40		120		ns
3	t_{AK}	A0 to 23 Valid→ CLK Hold	0.5x – 30		10		ns
4	t_{KA}	CLK Valid→ A0 to 23 Hold	1.5x – 80		40		ns
5	t_{AL}	A0 to 15 Valid→ ALE fall	0.5x – 35		5		ns
6	t_{LA}	ALE fall→ A0 to 15 Hold	0.5x – 35		5		ns
7	t_{LL}	ALE High width	x – 60		20		ns
8	t_{LC}	ALE fall→ $\overline{RD}/\overline{WR}$ fall	0.5x – 35		5		ns
9	t_{CL}	$\overline{RD}/\overline{WR}$ rise→ ALE rise	0.5x – 40		0		ns
10	t_{ACL}	A0 to 15 Valid→ $\overline{RD}/\overline{WR}$ fall	x – 50		30		ns
11	t_{ACH}	A0 to 23 Valid→ $\overline{RD}/\overline{WR}$ fall	1.5x – 50		70		ns
12	t_{CA}	$\overline{RD}/\overline{WR}$ rise→ A0 to 23 Hold	0.5x – 40		0		ns
13	t_{ADL}	A0 to 15 Valid→ D0 to 15 input		3.0x – 110		130	ns
14	t_{ADH}	A0 to 23 Valid→ D0 to 15 input		3.5x – 125		155	ns
15	t_{RD}	$\overline{RD}$fall → D0 to 15 input		2.0x – 115		45	ns
16	t_{RR}	$\overline{RD}$ Low pulse width	2.0x – 40		120		ns
17	t_{HR}	$\overline{RD}$rise→ D0 to 15 Hold	0		0		ns
18	t_{RAE}	$\overline{RD}$rise→ A0 to 15output	x – 25		55		ns
19	t_{WW}	$\overline{WR}$ Low pulse width	2.0x – 40		120		ns
20	t_{DW}	D0 to 15 Valid→ $\overline{WR}$rise	2.0x – 120		40		ns
21	t_{WD}	$\overline{WR}$ rise →D0 to 15 Hold	0.5x – 40		0		ns
22	t_{AWH}	A0 to 23 Valid→ $\overline{WAIT}$ input (1 WAIT + n mode)		3.5x – 130		150	ns
23	t_{AWL}	A0 to 15 Valid→ $\overline{WAIT}$ input (1 WAIT + n mode)		3.0x – 100		140	ns
24	t_{CW}	$\overline{RD}/\overline{WR}$ fall→ $\overline{WAIT}$ Hold (1 WAIT + n mode)	2.0x + 0		160		ns
25	t_{APH}	A0 to 23 Valid→ PORT input		2.5x – 120		80	ns
26	t_{APH2}	A0 to 23 Valid→ PORT Hold	2.5x + 50		250		ns
27	t_{CP}	$\overline{WR}$ rise→ PORT Valid		200		200	ns

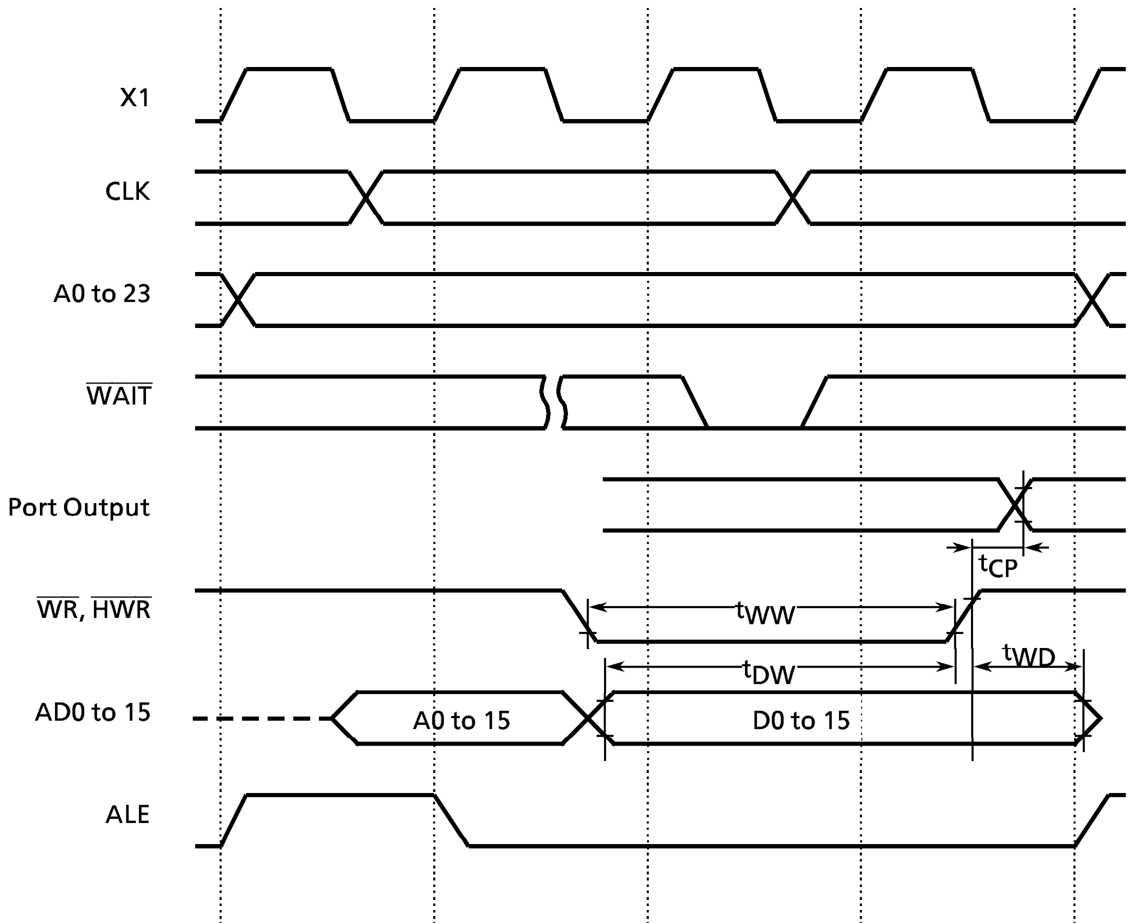
AC Measuring Conditions

- Output Level : High 0.7 × V_{CC} / Low 0.3 × V_{CC} , CL = 50 pF
- Input Level : High 0.9 × V_{CC} / Low 0.1 × V_{CC}

(1) Read Cycle


X1
CLK
A0 to 23
WAIT
Port Input
RD
AD0 to 15
ALE
tOSC
tCLK
tAK
tKA
tAWH
tCW
tAWL
tAPH
tAPH2
tADH
tCA
tACH
tRR
tRAE
tACL
tRD
tHR
tLC
tADL
A0 to 15
D0 to 15
tAL
tLA
tCL
tLL

(2) Write Cycle



4.4 Serial Channel Timing

(1) I/O Interface Mode

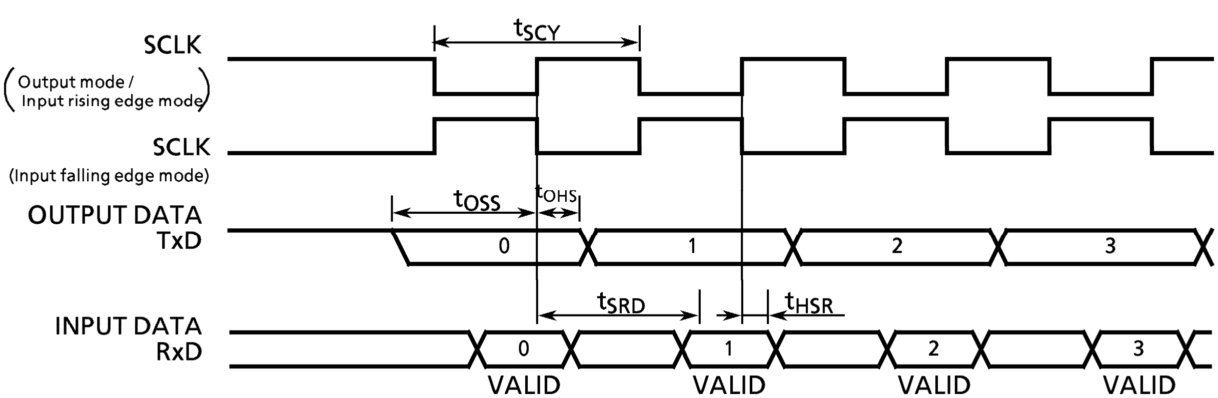
① SCLK Input Mode

Symbol	Parameter	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK cycle	16X		1.28		0.8		μs
t_{OSS}	Output Data → Rising / falling edge of SCLK	t_{SCY}/2 – 5X – 50		190		100		ns
t_{OHS}	SCLK rising / falling edge→ Output Data hold	5X – 100		300		150		ns
t_{HSR}	SCLK rising / falling edge→ Input Data hold	0		0		0		ns
t_{SRD}	SCLK rising / falling edge→ effective data input		t_{SCY} – 5X – 100		780		450	ns

Note : SCLK rising / falling timing ; SCLK rising in the rising mode of SCLK,
SCLK falling in the falling mode of SLCK.

② SCLK Output Mode

Symbol	Parameter	Variable		12.5 MHz		20MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK cycle (programmable)	16X	8192X	1.28	655.36	0.8	409.6	μs
t_{OSS}	Output Data → SCLK rising edge	t_{SCY} – 2X – 150		970		550		ns
t_{OHS}	SCLK rising edge→ Output Data hold	2X – 80		80		20		ns
t_{HSR}	SCLK rising edge→ Input Data hold	0		0		0		ns
t_{SRD}	SCLK rising edge→ effective data input		t_{SCY} – 2X – 150		970		550	ns



(2) UART Mode (SCLK0, 1 are external input)

Symbol	Parameter	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{SCY}	SCLK cycle	4x + 20		340		220		ns
t_{SCYL}	SCLK Low level pulse width	2x + 5		165		105		ns
t_{SCYH}	SCLK High level pulse width	2x + 5		165		105		ns

4.5 A/D Conversion Characteristics

$AV_{CC} = V_{CC}$, $AV_{SS} = V_{SS}$

Symbol	Parameter	Power Supply	Min	Typ	Max	Unit
VREFH	Analog reference voltage (+)	V_{CC} = 5V ± 10 %	V_{CC} – 0.2 V	V_{CC}	V_{CC}	V
		V_{CC} = 3V ± 10 %	V_{CC} – 0.2 V	V_{CC}	V_{CC}	
VREFL	Analog reference voltage (–)	V_{CC} = 5V ± 10 %	V_{SS}	V_{SS}	V_{SS} + 0.2 V	
		V_{CC} = 3V ± 10 %	V_{SS}	V_{SS}	V_{SS} + 0.2 V	
V_{AIN}	Analog input voltage range		VREFL		VREFH	
I_{REF} (V_{REFL} = 0 V)	Analog current for analog reference voltage <VREFON> = 1	V_{CC} = 5V ± 10 %		0.5	1.5	mA
		V_{CC} = 3V ± 10 %		0.3	0.9	
	<VREFON> = 0	V_{CC} = 2.7 to 5.5V		0.02	5.0	μA
–	Error (except quantization errors)	V_{CC} = 5V ± 10 %		± 1.0	± 3.0	LSB
		V_{CC} = 3V ± 10 %		± 1.0	± 5.0	

Note 1: 1LSB = (VREFH – VREFL) / 2^{10} [V]
Note 2: The operation above is guaranteed for $f_{FPH} \geqq 4$ MHz.
Note 3: The value I_{CC} includes the current which flows through the AVCC pin.

4.6 Event Counter Input Clock (external input clock : TI4, TI5, TI6, TI7)

Symbol	Parameter	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{VCK}	Clock Cycle	8X + 100		740		500		ns
t_{VCKL}	Low level clock Pulse width	4X + 40		360		240		ns
t_{VCKH}	High level clock Pulse width	4X + 40		360		240		ns

4.7 Interrupt and Capture Operation

(1) $\overline{\text{NMI}}$, INT0 Interrupts

Symbol	Parameter	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{INTAL}	$\overline{\text{NMI}}$, INT0 Low level Pulse width	4X		320		200		ns
t_{INTAH}	$\overline{\text{NMI}}$, INT0 High level Pulse width	4X		320		200		ns

(2) INT4 to 7 Interrupts and Capture

Symbol	Parameter	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
t_{INTBL}	INT4 to INT7 Low level Pulse width	4X + 100		420		300		ns
t_{INTBH}	INT4 to INT7 High level Pulse width	4X + 100		420		300		ns

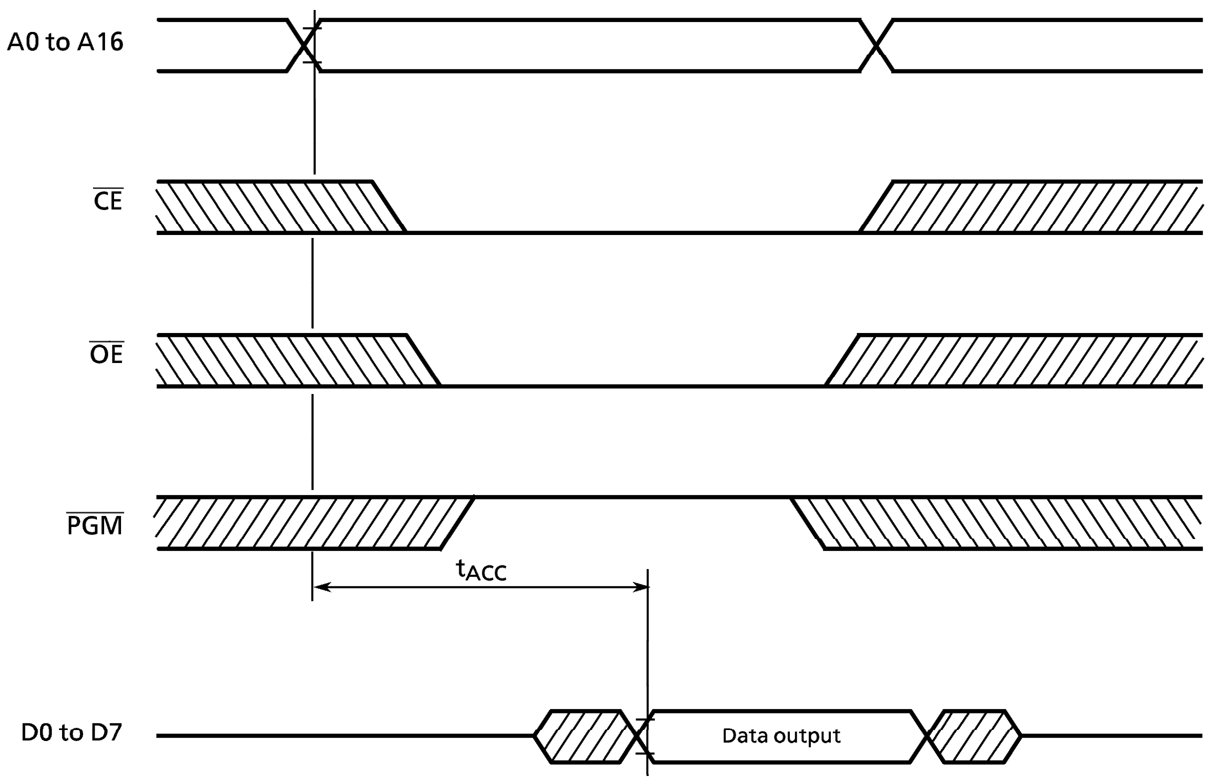
4.8 Read operation in PROM Mode

DC / AC characteristics

Ta = 25 ± 5 °C Vcc = 5 V ± 10 %

Symbol	Parameter	Condition	Min	Max	Unit
V_{PP}	V_{PP} Read Voltage	–	4.5	5.5	V
V_{IH1}	Input High Voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	–	2.2	V_{CC} + 0.3	V
V_{IL1}	Input Low Voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	–	– 0.3	0.8	V
t_{ACC}	Address to Output Delay	C_L = 50 pF	–	2.25TCYC + α	ns

TCYC = 400 ns (10 MHz Clock)
α = 200 ns

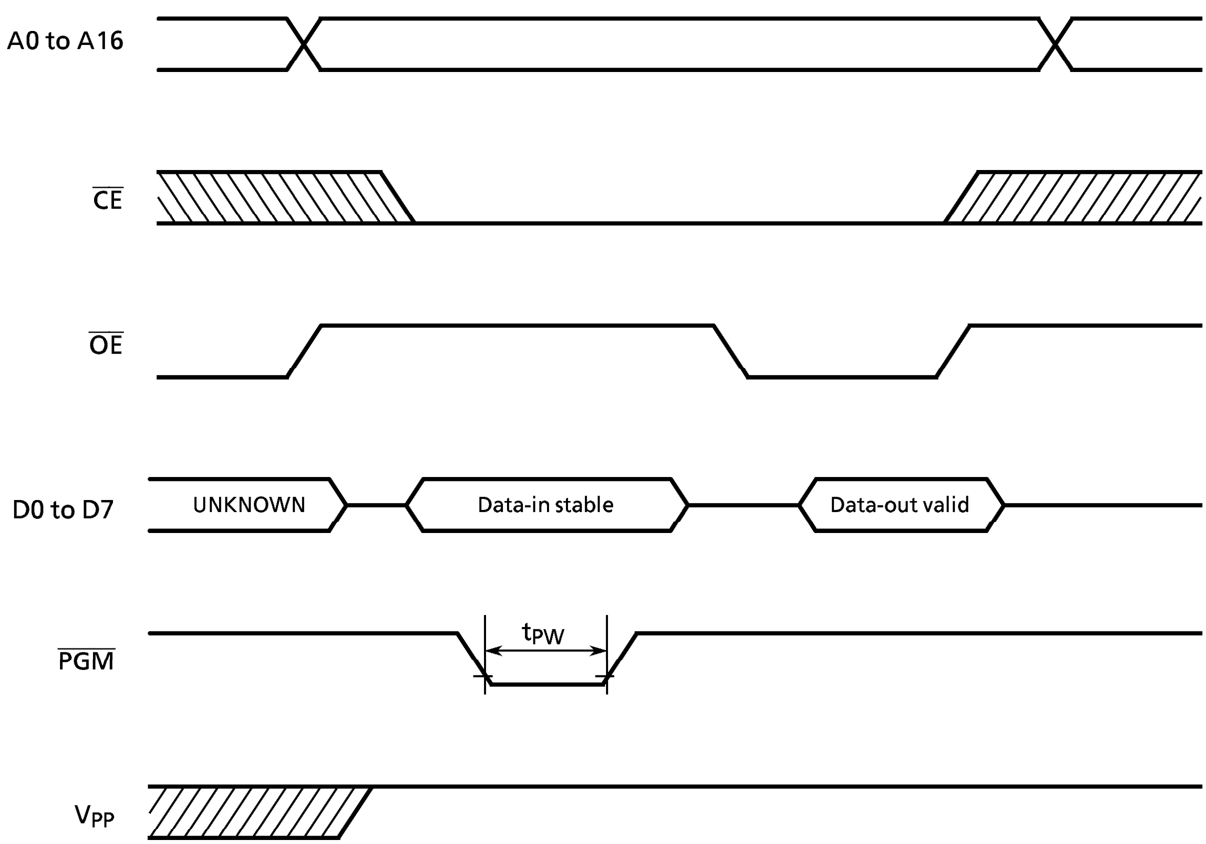


4.9 Program operation in PROM Mode

DC / AC characteristics

Ta = 25 ± 5 °C Vcc = 6.25 V ± 0.25 V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{PP}	Programming Supply Voltage	–	12.50	12.75	13.00	V
V_{IH}	Input High Voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	–	2.6		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	–	– 0.3		0.8	V
I_{CC}	V_{CC} Supply Current	fc = 10 MHz	–		50	mA
I_{PP}	V_{PP} Supply Current	V_{PP} = 13.00 V	–		50	mA
t_{PW}	$\overline{PGM}$ Program Pulse Width	C_L = 50 pF	0.095	0.1	0.105	ms



NOTE

1. The power supply of V_{PP} (12.75 V) must br set power-on at the same time or the later time for a power supply of V_{CC} and must be clear power-on at the same time or early time for a power supply of V_{CC}.
2. The pulling up/down device on condition of V_{PP} = 12.75 V suffer a damage for the device.
3. The maximum spec of V_{PP} pin is 14.0 V. Be carefull a overshoot at the program writing.