

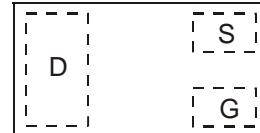
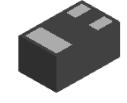
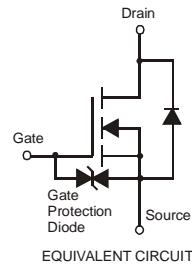
Features

- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Ultra-Small Surface Mount Package
- Ultra-Low Package Profile, 0.4mm Maximum Package Height
- **Lead Free By Design/RoHS Compliant (Note 1)**
- **ESD Protected up to 1.5kV**
- **"Green" Device (Note 2)**
- **Qualified to AEC-Q101 standards for High Reliability**

Mechanical Data

- Case: DFN1006H4-3
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish — NiPdAu over Copper leadframe. Solderable per MIL-STD-202, Method 208
- Weight: 0.001 grams (approximate)

DFN1006H4-3


 TOP VIEW
 Package Pin Configuration


Ordering Information (Note 3)

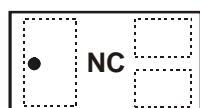
Part Number	Marking	Reel size (inches)	Tape width (mm)	Quantity per reel
DMN2400UFB4-7	NC	7	8	3000
DMN2400UFB4-7B	NC	7	8	10,000

Notes:

1. No purposefully added lead.
2. Diodes Inc.'s "Green" policy can be found on our website at <http://www.diodes.com>.
3. For packaging details, go to our website at <http://www.diodes.com>.

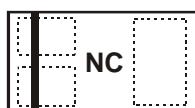
Marking Information

DMN2400UFB4-7



Top View
 Dot Denotes
 Drain Side

DMN2400UFB4-7B



Top View
 Bar Denotes Gate
 and Source Side

NC = Product Type Marking Code

Maximum Ratings @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	20	V
Gate-Source Voltage			V_{GSS}	± 12	V
Continuous Drain Current (Note 4) $V_{GS} = 4.5\text{V}$	Steady State	$T_A = 25^\circ\text{C}$ $T_A = 85^\circ\text{C}$	I_D	0.75 0.55	A
Pulsed Drain Current (Notes 4 & 5)			I_{DM}	3	A

Thermal Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified

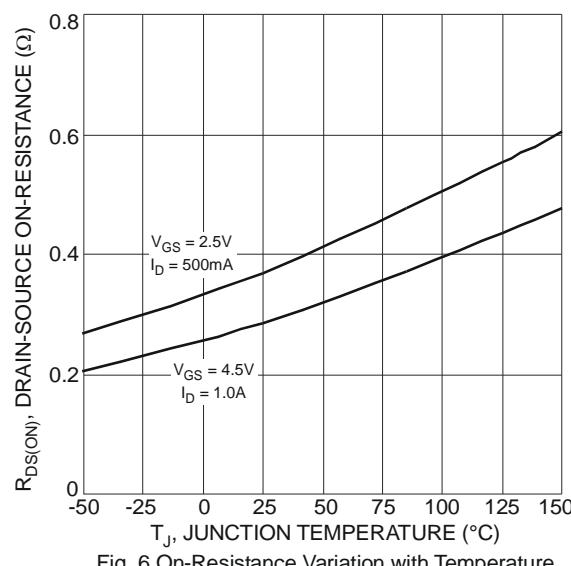
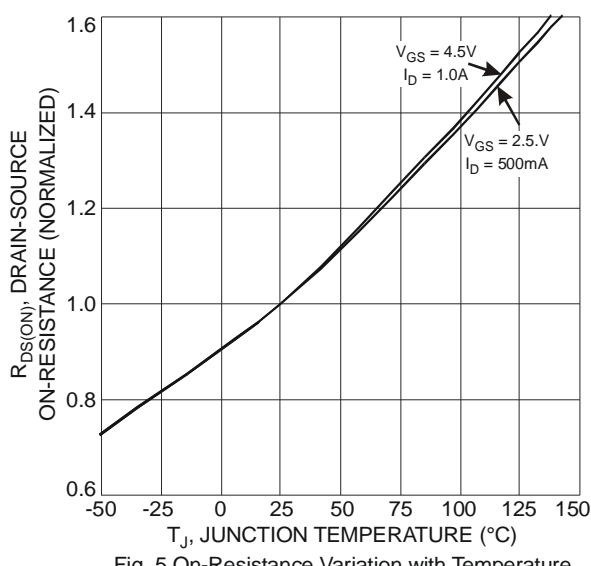
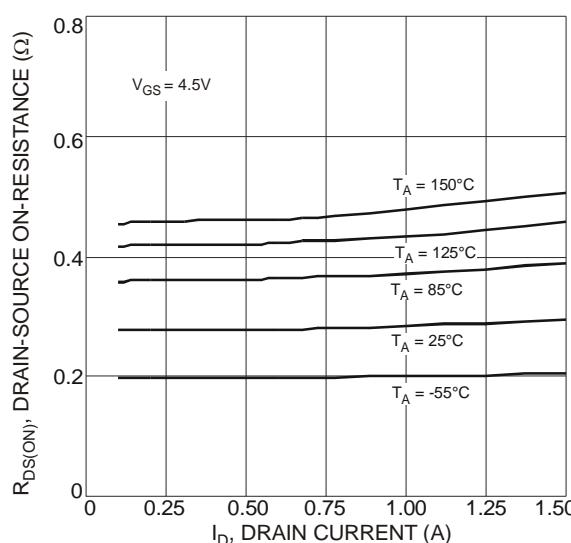
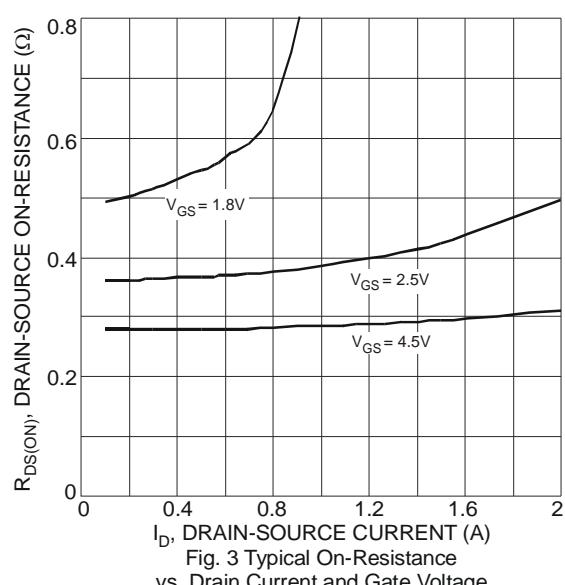
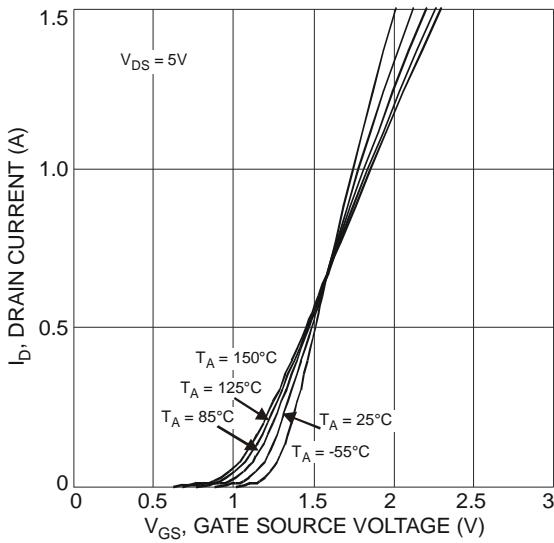
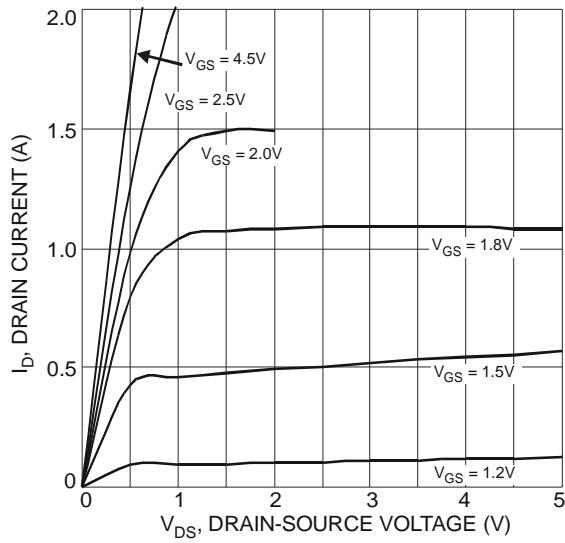
Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 4)	P_D	0.47	mW
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	258	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 6)						
Drain-Source Breakdown Voltage	BV_{DSS}	20	-	-	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current $T_J = 25^\circ\text{C}$	I_{DSS}	-	-	100	nA	$V_{DS} = 20\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	-	-	± 1.0	μA	$V_{GS} = \pm 4.5\text{V}, V_{DS} = 0\text{V}$
Gate-Source Leakage	I_{GS}	-	-	± 50	μA	$V_{GS} = \pm 10\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 6)						
Gate Threshold Voltage	$V_{GS(th)}$	0.5	-	0.9	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(\text{ON})}$	-	-	0.55	Ω	$V_{GS} = 4.5\text{V}, I_D = 600\text{mA}$
		-	-	0.75		$V_{GS} = 2.5\text{V}, I_D = 500\text{mA}$
		-	-	0.9		$V_{GS} = 1.8\text{V}, I_D = 350\text{mA}$
Forward Transfer Admittance	$ Y_{fs} $	-	1.0	-	S	$V_{DS} = 10\text{V}, I_D = 400\text{mA}$
Diode Forward Voltage (Note 6)	V_{SD}	-	0.7	1.2	V	$V_{GS} = 0\text{V}, I_S = 150\text{mA}$
DYNAMIC CHARACTERISTICS (Note 7)						
Input Capacitance	C_{iss}	-	36.0	-	pF	$V_{DS} = 16\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	-	5.7	-	pF	
Reverse Transfer Capacitance	C_{rss}	-	4.2	-	pF	
Total Gate Charge	Q_g	-	0.5	-	nC	$V_{GS} = 4.5\text{V}, V_{DS} = 10\text{V}, I_D = 250\text{mA}$
Gate-Source Charge	Q_{qs}	-	0.07	-	nC	
Gate-Drain Charge	Q_{qd}	-	0.1	-	nC	
Turn-On Delay Time	$t_{D(on)}$	-	4.11	-	ns	$V_{DD} = 10\text{V}, V_{GS} = 4.5\text{V}, R_L = 47\Omega, R_G = 10\Omega, I_D = 200\text{mA}$
Turn-On Rise Time	t_r	-	3.82	-	ns	
Turn-Off Delay Time	$t_{D(off)}$	-	14.8	-	ns	
Turn-Off Fall Time	t_f	-	9.6	-	ns	

Notes:

4. Device mounted on FR-4 PCB, with minimum recommended pad layout, single sided.
5. Device mounted on minimum recommended pad layout test board, 10 μs pulse duty cycle = 1%.
6. Short duration pulse test used to minimize self-heating effect.
7. Guaranteed by design. Not subject to product testing.



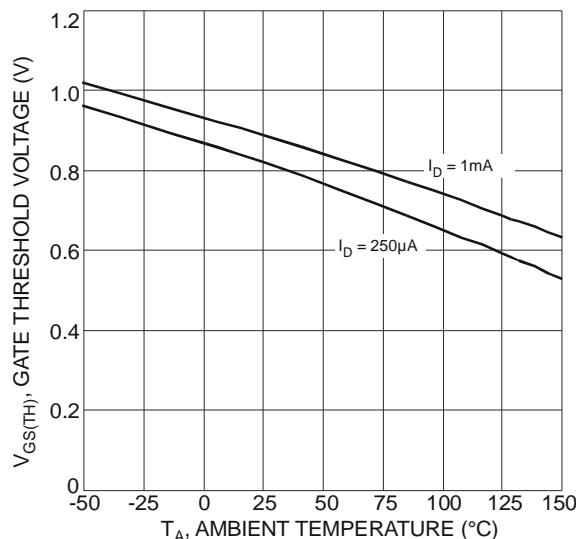


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

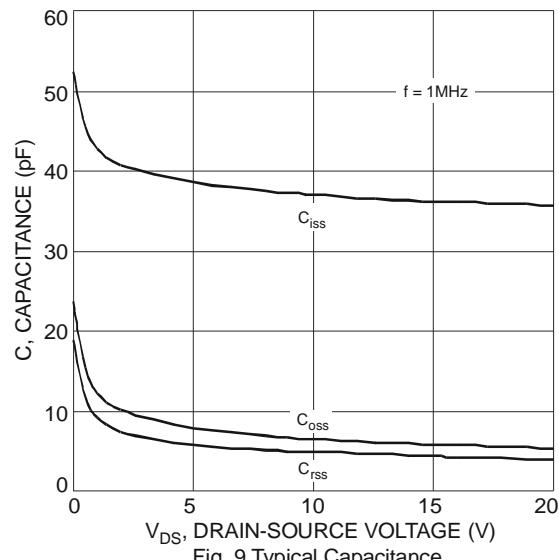


Fig. 9 Typical Capacitance

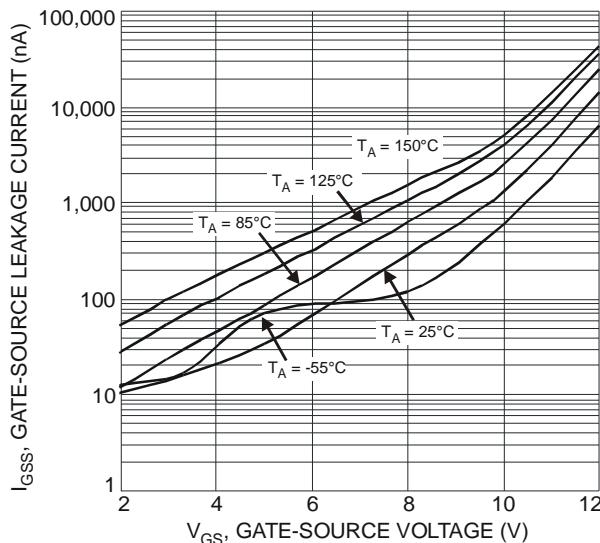


Fig. 11 Typical Gate-Source Leakage Current vs. Gate-Source Voltage

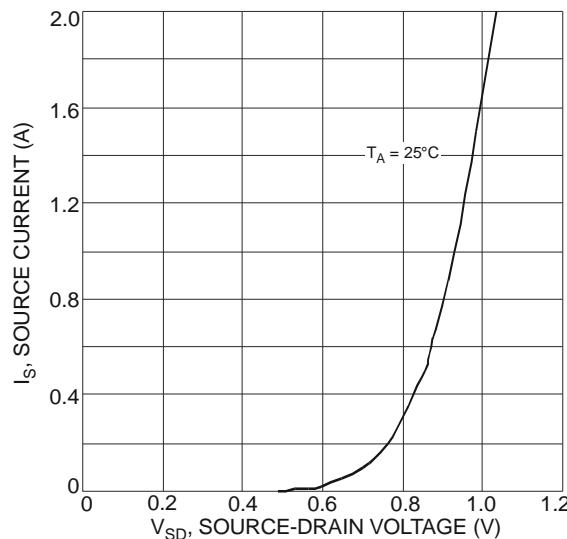


Fig. 8 Diode Forward Voltage vs. Current

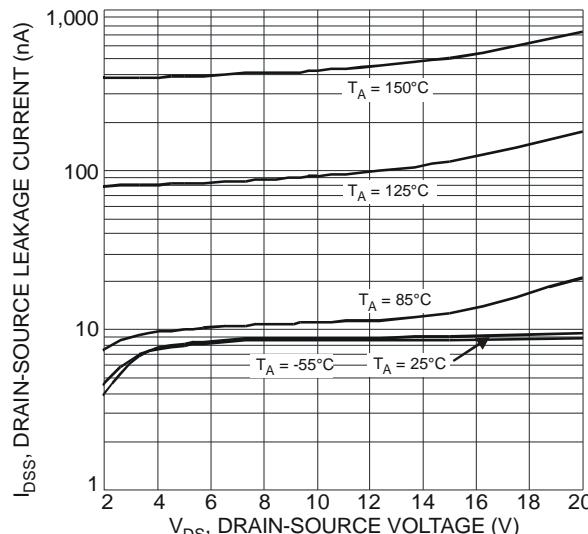


Fig. 10 Typical Drain-Source Leakage Current vs. Drain-Source Voltage

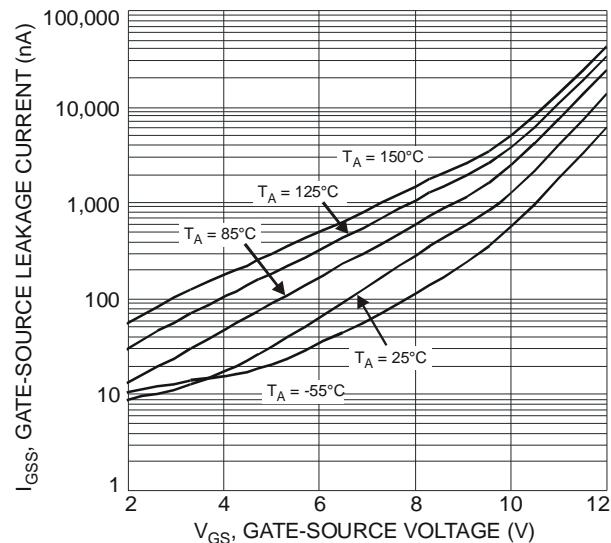


Fig. 12 Typical Gate-Source Leakage Current vs. Gate-Source Voltage

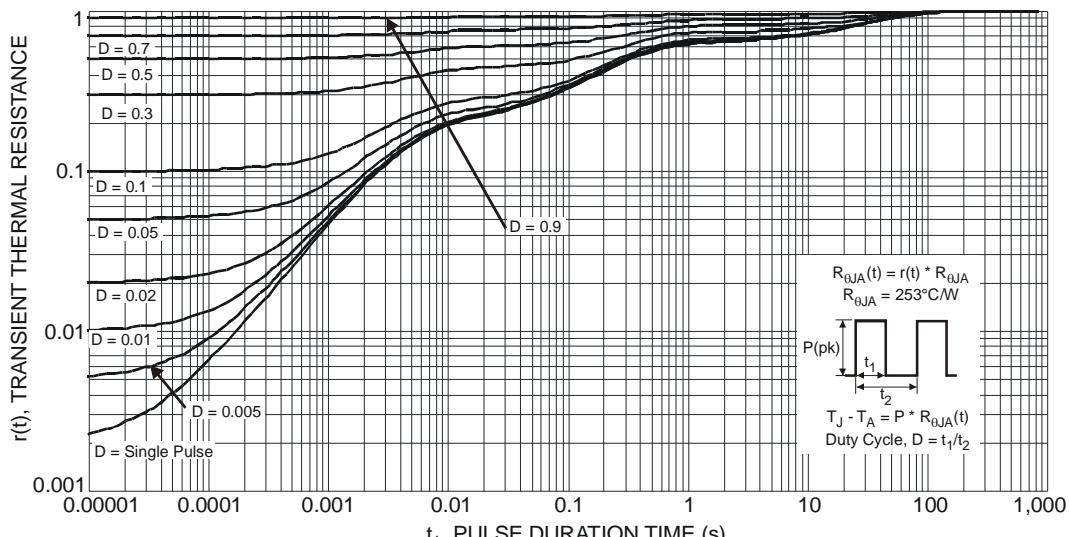
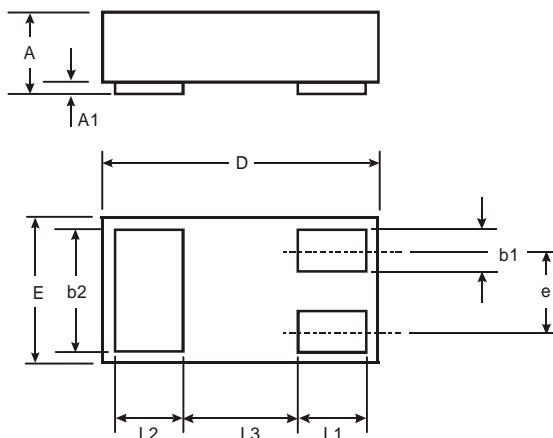


Fig. 13 Transient Thermal Response

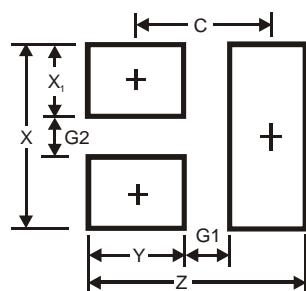
Package Outline Dimensions



DFN1006H4-3			
Dim	Min	Max	Typ
A	—	0.40	—
A1	0	0.05	0.02
b1	0.10	0.20	0.15
b2	0.45	0.55	0.50
D	0.95	1.075	1.00
E	0.55	0.675	0.60
e	—	—	0.35
L1	0.20	0.30	0.25
L2	0.20	0.30	0.25
L3	—	—	0.40

All Dimensions in mm

Suggested Pad Layout



Dimensions	Value (in mm)
Z	1.1
G1	0.3
G2	0.2
X	0.7
X1	0.25
Y	0.4
C	0.7

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