

# SN74ALVC16409

## 9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER

### WITH 3-STATE OUTPUTS

SCAS259A – NOVEMBER 1993 – REVISED JULY 1995

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- Member of the Texas Instruments **Widebus+™** Family
- **UBE™** (Universal Bus Exchanger) Allows Synchronous Data Exchange
- Designed to Facilitate Incident-Wave Switching for Line Impedances of 50  $\Omega$  or Greater
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) > 2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200$  pF,  $R = 0$ )
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages

#### description

The SN74ALVC16409 allows synchronous data exchange between four different buses.

Data flow is controlled by the select (SEL0–SEL4) inputs. A data-flow state is stored on the rising edge of the clock (CLK) input if the select-enable (SELEN) input is low. Once a data-flow state has been established, data is stored in the flip-flop on the rising edge of CLK if SELEN is high.

The data-flow control logic is designed to allow glitch-free data transmission.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16409 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16409 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

DGG OR DL PACKAGE  
(TOP VIEW)

PRE	1	56	CLK
SEL0	2	55	SELEN
1A1	3	54	1B1
GND	4	53	GND
1A2	5	52	1B2
1A3	6	51	1B3
V <sub>CC</sub>	7	50	V <sub>CC</sub>
1A4	8	49	1B4
1A5	9	48	1B5
1A6	10	47	1B6
GND	11	46	GND
1A7	12	45	1B7
1A8	13	44	1B8
1A9	14	43	1B9
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V <sub>CC</sub>	22	35	V <sub>CC</sub>
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2A9	26	31	2B9
SEL1	27	30	SEL4
SEL2	28	29	SEL3



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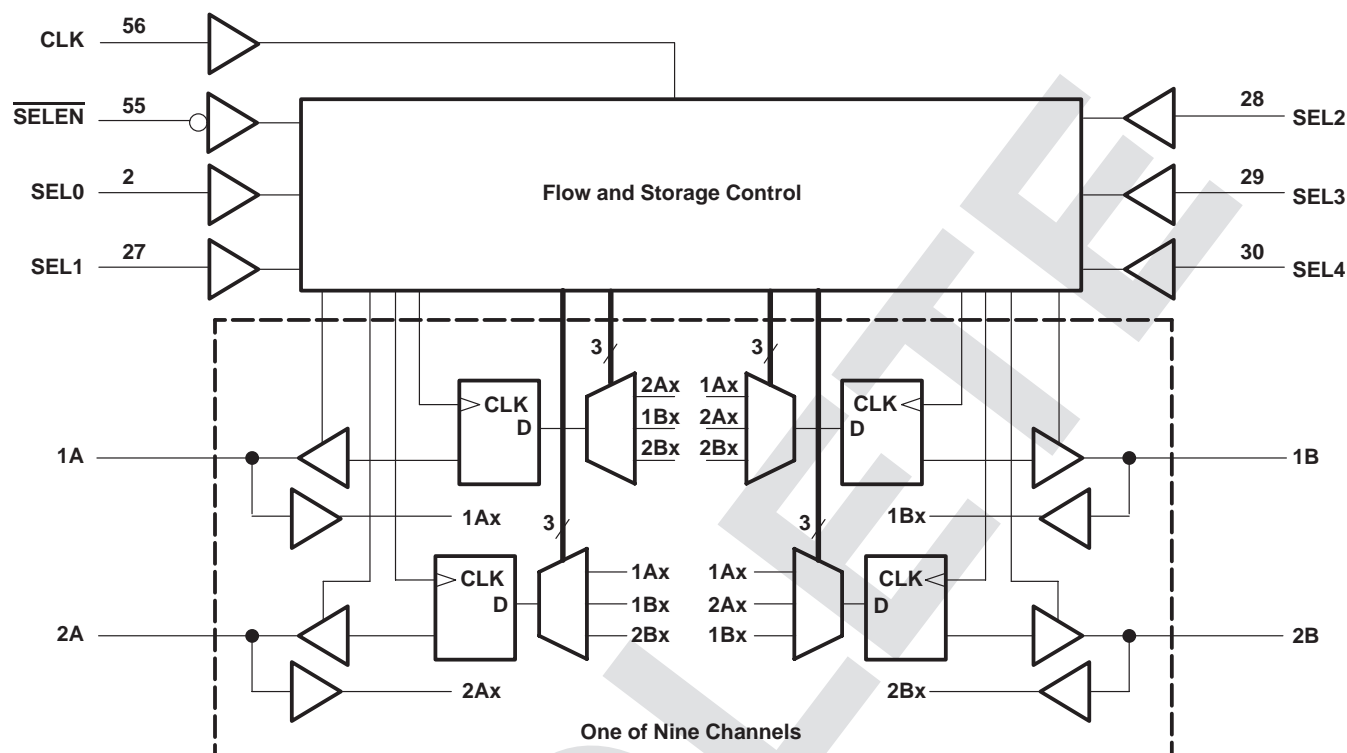
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## 9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER WITH 3-STATE OUTPUTS

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### logic diagram (positive logic)



FUNCTION TABLE

INPUTS		OUTPUT RECEIVE PORT
CLK	SEND PORT	
X	X	$B_0^\dagger$
X	L	L
X	H	H
↑	L	L
↑	H	H
H	X	$B_0^\dagger$
L	X	$B_0^\dagger$

† Output level before the indicated steady-state input conditions were established

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**DATA-FLOW CONTROL FUNCTION TABLE**

INPUTS							DATA FLOW
SELEN	CLK	SEL0	SEL1	SEL2	SEL3	SEL4	
H	↑	X	X	X	X	X	No change
L	↑	0	0	0	0	0	None, all I/Os off
L	↑	0	0	0	0	1	Not used
L	↑	0	0	0	1	0	Not used
L	↑	0	0	0	1	1	Not used
L	↑	0	0	1	0	0	Not used
L	↑	0	0	1	0	1	Not used
L	↑	0	0	1	1	0	Not used
L	↑	0	0	1	1	1	Not used
L	↑	0	1	0	0	0	2A to 1A and 1B to 2B
L	↑	0	1	0	0	1	2A to 1A
L	↑	0	1	0	1	0	2B to 1B
L	↑	0	1	0	1	1	2A to 1A and 2B to 1B
L	↑	0	1	1	0	0	1A to 2A and 1B to 2B
L	↑	0	1	1	0	1	1A to 2A
L	↑	0	1	1	1	0	1B to 2B
L	↑	0	1	1	1	1	1A to 2A and 2B to 1B
L	↑	1	0	0	0	0	1A to 1B and 2B to 2A
L	↑	1	0	0	0	1	1A to 1B
L	↑	1	0	0	1	0	2A to 2B
L	↑	1	0	0	1	1	1A to 1B and 2A to 2B
L	↑	1	0	1	0	0	1B to 1A and 2A to 2B
L	↑	1	0	1	0	1	1B to 1A
L	↑	1	0	1	1	0	2B to 2A
L	↑	1	0	1	1	1	1B to 1A and 2B to 2A
L	↑	1	1	0	0	0	2B to 1A and 2A to 1B
L	↑	1	1	0	0	1	1B to 2A
L	↑	1	1	0	1	0	2B to 1A
L	↑	1	1	0	1	1	2B to 1A and 1B to 2A
L	↑	1	1	1	0	0	1A to 2B and 1B to 2A
L	↑	1	1	1	0	1	1A to 2B
L	↑	1	1	1	1	0	2A to 1B
L	↑	1	1	1	1	1	1A to 2B and 2A to 1B

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## 9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER

### WITH 3-STATE OUTPUTS

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ : Except I/O ports (see Note 1)	–0.5 V to $V_{CC} + 4.6$ V
I/O ports (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through $V_{CC}$ or GND pins	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. This value is limited to 4.6 V maximum.  
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2.7	3.6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V	2		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2.7 V to 3.6 V	0.8		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7		
V <sub>I</sub>	Input voltage		0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2.3 V	−12		mA
		V <sub>CC</sub> = 2.7 V	−12		
		V <sub>CC</sub> = 3 V	−24		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2.3 V	12		mA
		V <sub>CC</sub> = 2.7 V	12		
		V <sub>CC</sub> = 3 V	24		
Δt/Δv	Input transition rise or fall rate		0	10	ns/V
T <sub>A</sub>	Operating free-air temperature		−40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		V <sub>CC</sub> <sup>†</sup>	T <sub>A</sub> = –40°C to 85°C			UNIT
				MIN	TYP <sup>‡</sup>	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –100 μA		MIN to MAX	V <sub>CC</sub> – 0.2			V
	I <sub>OH</sub> = –6 mA	V <sub>IH</sub> = 1.7 V	2.3 V	2			
	I <sub>OH</sub> = –12 mA	V <sub>IH</sub> = 1.7 V	2.3 V	1.7			
		V <sub>IH</sub> = 2 V	2.7 V	2.2			
		V <sub>IH</sub> = 2 V	3 V	2.4			
	I <sub>OH</sub> = –24 mA	V <sub>IH</sub> = 2 V	3 V	2			
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA		MIN to MAX	0.2			V
	I <sub>OL</sub> = 6 mA	V <sub>IL</sub> = 0.7 V	2.3 V	0.4			
	I <sub>OL</sub> = 12 mA	V <sub>IL</sub> = 0.7 V	2.3 V	0.7			
		V <sub>IL</sub> = 0.8 V	2.7 V	0.4			
	I <sub>OL</sub> = 24 mA	V <sub>IL</sub> = 0.8 V	3 V	0.55			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		3.6 V	±5			μA
I <sub>I</sub> (hold)	V <sub>I</sub> = 0.7 V		2.3 V	45			μA
	V <sub>I</sub> = 1.7 V			–45			
	V <sub>I</sub> = 0.8 V		3 V	75			
	V <sub>I</sub> = 2 V			–75			
	V <sub>I</sub> = 0 to 3.6 V		3.6 V	±500			
I <sub>OZ</sub> <sup>§</sup>	V <sub>O</sub> = V <sub>CC</sub> or GND		3.6 V	±10			μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0		3.6 V	40			μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND		3 V to 3.6 V	500			μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		3.3 V	4			pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND		3.3 V	8			pF

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

<sup>‡</sup> All typical values are measured at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

<sup>§</sup> For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

			V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V	V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MIN	MAX	
f <sub>clock</sub>	Clock frequency		0	120		0	120	MHz
t <sub>w</sub>	Pulse duration, CLK high or low		4.2		4.2	3		ns
t <sub>su</sub>	Setup time	A or B before CLK↑	1.9		1.9	1.4		ns
		S before CLK↑	5.1		4.2	3.5		
		SELEN before CLK↑	2.5		2.5	1.8		
		PRE before CLK↑	1		1	0.7		
t <sub>h</sub>	Hold time	A or B after CLK↑	0.8		0.8	1		ns
		S after CLK↑	0		0	0		
		SELEN after CLK↑	0.5		0.5	0.8		



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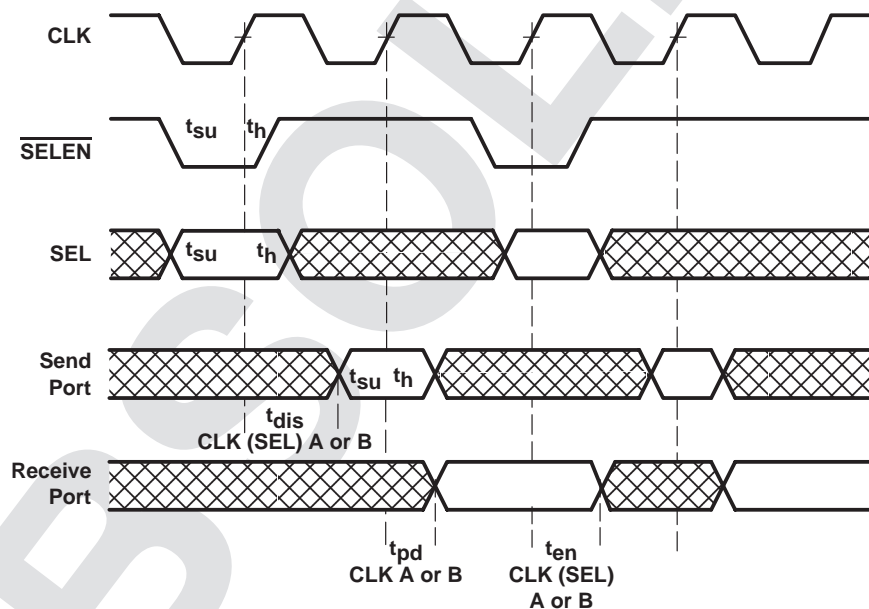
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$			$V_{CC} = 2.7\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			UNIT
			MIN	TYP	MAX	MAX	MIN	TYP	MAX	
$f_{\max}$			120				120			MHz
$t_{pd}$	CLK (A or B)	B or A	2	4.2	6.6	5.7	1.5	3.3	5.1	ns
$t_{en}$	CLK (SEL)	A or B	2.5	4.8	7.4	6.3	2	3.8	5.7	ns
$t_{dis}$	CLK (SEL)	A or B	3	5.1	7.3	6	2	4	5.7	ns
$t_{dis}$	$\overline{\text{PRE}}$	A or B	3.5	5.5	7.7	6.5	2.5	4.2	6.1	ns

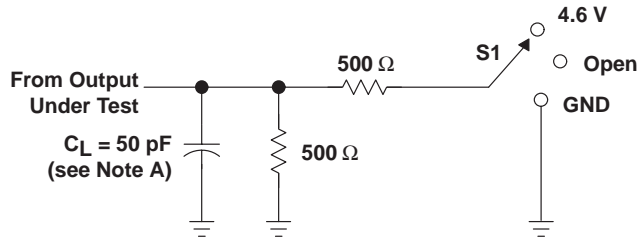
operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	UNIT
			TYP	TYP	
$C_{pd}$ Power dissipation capacitance	Outputs enabled	$C_L = 50$ pF, $f = 10$ MHz	60	60	pF
	Outputs disabled				

timing diagram

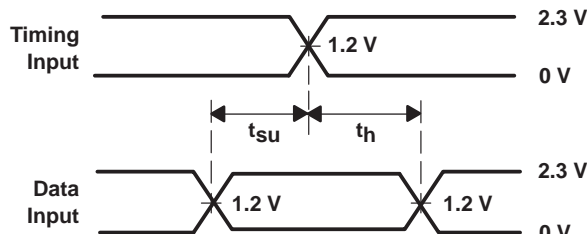


**PARAMETER MEASUREMENT INFORMATION**  
 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

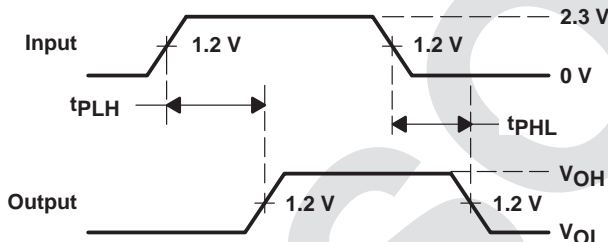


**LOAD CIRCUIT**

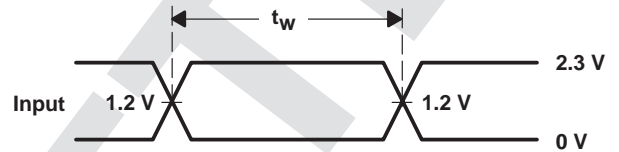
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	4.6 V
$t_{PHZ}/t_{PZH}$	GND



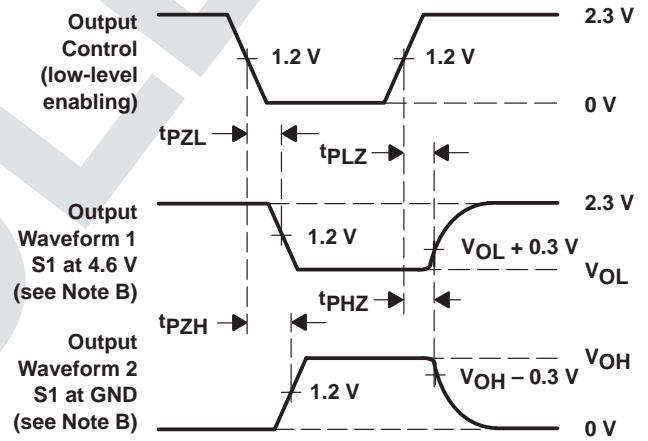
**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS  
PULSE DURATION**



**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

# SN74ALVC16409

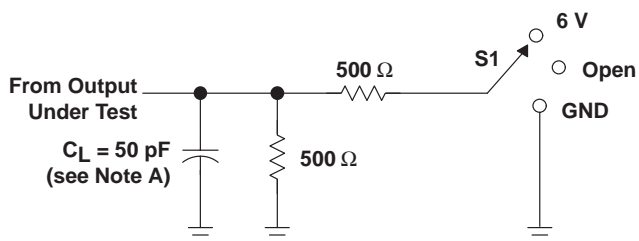
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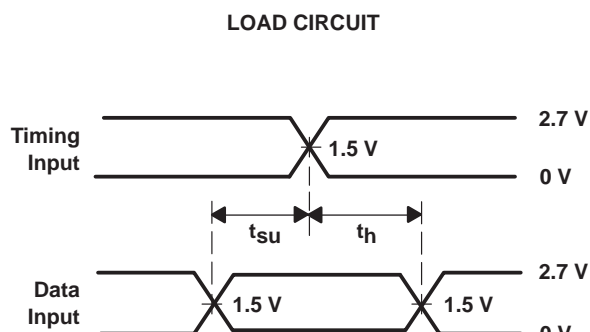
#### PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.7\text{ V AND } 3.3\text{ V} \pm 0.3\text{ V}$

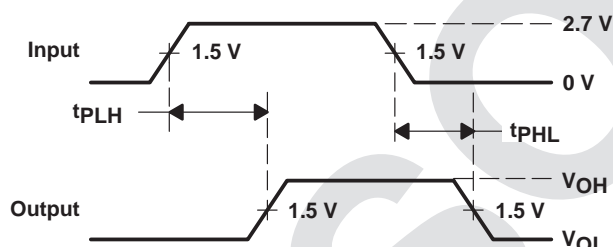


LOAD CIRCUIT

TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



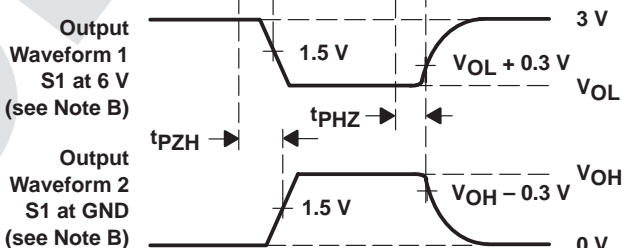
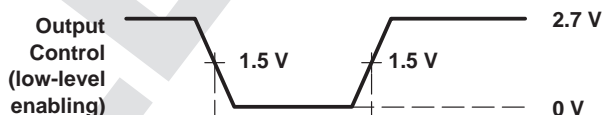
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
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  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\text{ }\Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 2. Load Circuit and Voltage Waveforms

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