

# 20V<sub>P-P</sub> CHARGE PUMP CERAMIC SPEAKER DRIVER

**July 2013** 

#### **GENERAL DESCRIPTION**

The IS31AP4915A features a mono power amplifier with an integrated charge-pump power supply specifically designed to drive the high capacitance of a ceramic loudspeaker.

The IS31AP4915A maximizes battery life by offering high performance efficiency.

The IS31AP4915A is ideally suited to deliver the high output-voltage swing required to drive ceramic/piezoelectric speakers.

The device utilizes comprehensive click-and-pop suppression and shutdown control. The IS31AP4915A is fully specified over the -40°C to +85°C extended temperature range and is available in small lead-free 16-pin QFN (4mm × 4mm) packages.

#### **FEATURES**

- Integrated charge-pump power supply no inductor required
- Thermal protection
- Pop reduction circuitry
- 20V<sub>P-P</sub> voltage swing into piezoelectric speaker
- QFN-16, 4mm × 4mm
- ESD (HBM): 2kV
   ESD (MM): 200V

#### **APPLICATIONS**

- CD/MP3 players
- Smart phones
- Cellular phones
- PDAs
- Handheld gaming

#### TYPICAL APPLICATION CIRCUIT

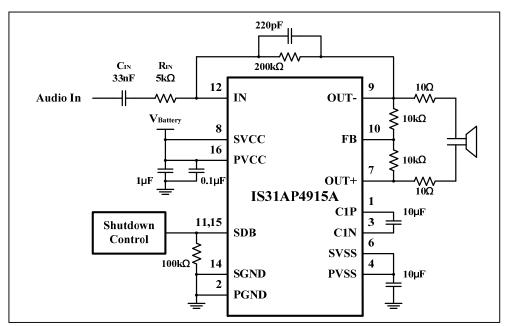


Figure 1 Typical Application Circuit

# IS31AP4915A



# **PIN CONFIGURATION**

Package	Pin Configuration (Top View)	
QFN-16	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	

# **PIN DESCRIPTION**

No.	Pin	Description		
1	C1P	Charge pump flying capacitor positive terminal.		
2	PGND	Power ground, connect to ground.		
3	C1N	Charge pump flying capacitor negative terminal.		
4	PVSS	Output from charge pump.		
5, 13	NC	No connection.		
6	SVSS	Amplifier negative supply, connect to PVSS.		
7	OUT+	Positive output signal.		
8	SVCC	Amplifier positive supply, connect to PVCC.		
9	OUT-	Negative output signal.		
10	FB	Feed back.		
11, 15	SDB	Shutdown, active low logic.		
12	IN	Audio input signal.		
14	SGND	Signal ground, connect to ground.		
16	PVCC	Charge pump supply voltage, connect to positive supply.		
	Thermal Pad	Connect to GND.		





ORDERING INFORMATION Industrial Range: -40°C to +85°C

Order Part No.	Package	QTY/Reel
IS31AP4915A-QFLS2-TR	QFN-16, Lead-free	3000

Copyright © 2013 Integrated Silicon Solution, Inc. All rights reserved. ISSI reserves the right to make changes to this specification and its products at any time without notice. ISSI assumes no liability arising out of the application or use of any information, products or services described herein. Customers are advised to obtain the latest version of this device specification before relying on any published information and before placing orders for products. Integrated Silicon Solution, Inc. does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless Integrated Silicon Solution, Inc. receives written assurance to its satisfaction, that:

a.) the risk of injury or damage has been minimized;

b.) the user assume all such risks; and

c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

# IS31AP4915A



# **ABSOLUTE MAXIMUM RATINGS**

Supply voltage, V <sub>CC</sub>	−0.3V ~ +7.0V
Voltage at any input pin	$-0.3V \sim V_{CC} + 0.3V$
Maximum junction temperature, T <sub>JMAX</sub>	150°C
Storage temperature range, T <sub>STG</sub>	−65°C ~ +150°C
Operating temperature range, T <sub>A</sub>	−40°C ~ +85°C

#### Note:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# **ELECTRICAL CHARACTERISTICS**

 $T_A$ =25°C,  $V_{CC}$  = 2.5V ~ 5.5V (unless otherwise noted). (Note 1)

Symbol	Parameter	Condition	Min.	Тур.	Max.	Unit
$SV_{CC}$ , $PV_{CC}$	Supply voltage		2.5		5.5	V
$V_{IH}$	High level input voltage		1.5			V
$V_{IL}$	Low level input voltage				0.5	V
V <sub>os</sub>	Output offset voltage			6		mV
I <sub>cc</sub>	Supply current	$V_{CC} = 3V, V_{SDB} = V_{CC}$		6.0	8.0	- mA
		$V_{CC}$ = 5V, $V_{SDB}$ = $V_{CC}$		8.5	10.5	
I <sub>SD</sub>	Shutdown current	$V_{SDB} = 0V$			1	μΑ

#### **ELECTRICAL CHARACTERISTICS**

 $V_{CC}$  = 3.6V,  $T_A$  = 25°C (unless otherwise noted). (Note 2)

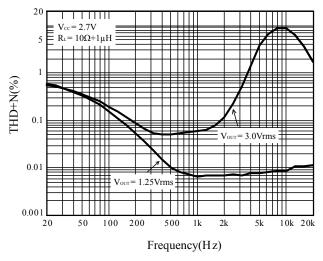
Symbol	Parameter	Condition		Min.	Тур.	Max.	Unit
V <sub>OUT</sub>	Output voltage	$f = 1kHz$ $THD+N = 10\%$ $R_L = 1\mu F + 10\Omega$	V <sub>CC</sub> = 5.0V		7.8		
			V <sub>CC</sub> = 3.6V		5.6		$V_{RMS}$
			V <sub>CC</sub> = 2.7V		4.3		
THEAN	Total harmonic distortion plus	R <sub>L</sub> = 1μF+10Ω,V <sub>OU1</sub>	= 1kHz/2V <sub>RMS</sub>		0.004		%
IUD+N	THD+N noise R <sub>L</sub> :		$R_L$ = 1 $\mu$ F+10 $\Omega$ , $V_{OUT}$ = 1 $k$ Hz/4 $V_{RMS}$		0.014		%
$V_{NO}$	Noise output voltage				10		$\mu V_{RMS}$
f <sub>osc</sub>	Charge pump switching frequency				320		kHz
t <sub>ON</sub>	Start-up time from shutdown				450		μs
SNR	Signal-to-noise ratio				100		dB
T <sub>OVP</sub>	Thermal shutdown threshold				160		°C
T <sub>HY</sub>	Thermal shutdown hysteresis				15		°C

**Note 1:** Production testing of the device is performed at 25°C. Functional operation of the device and parameters specified over other temperature range, are guaranteed by design, characterization and process control.

Note 2: Guaranteed by design.



#### TYPICAL OPERATING CHARACTERISTICS



0.01 0.0

20

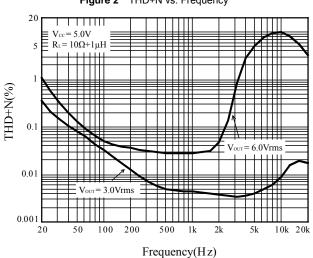
 $V_{\rm cc}\!=3.6V$ 

 $R_L = 10\Omega + 1\mu H$ 

Figure 2 THD+N vs. Frequency

Figure 3 THD+N vs. Frequency

Frequency(Hz)



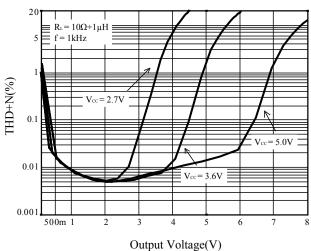
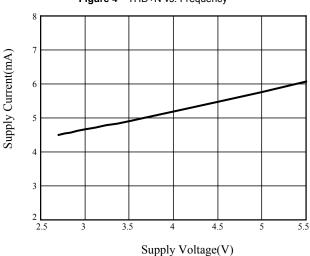


Figure 4 THD+N vs. Frequency

Figure 5 THD+N vs. Output Voltage



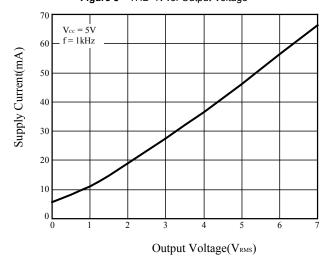
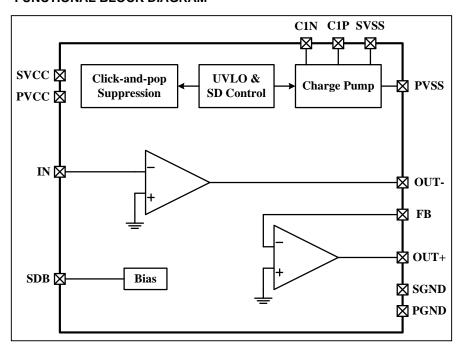


Figure 6 Supply Current vs. Supply Voltage

Figure 7 Supply Current vs. Output Voltage



# **FUNCTIONAL BLOCK DIAGRAM**





#### **APPLICATION INFORMATION**

#### **INPUT-BLOCKING CAPACITORS**

DC input-blocking capacitors are required to be added in series with the audio signal into the input pin of the IS31AP4915A. This capacitor block the DC portion of the audio source and allow the IS31AP4915A inputs to be properly biased to provide maximum performance.

These capacitors form a high-pass filter with the input impedance of the IS31AP4915A. The cutoff frequency is calculated using Equation 1. For this calculation, the capacitance used is the input-blocking capacitor and the resistance is the input impedance of the IS31AP4915A. Because the gains of both the IS31AP4915A is fixed, the input impedance remains a constant value. Using the input impedance value from the operating characteristics table, the frequency and/or capacitance can be determined when one of the two values is given.

$$f_{CIN} = \frac{1}{2\pi R_{IN}C_{IN}} \qquad (1)$$
 or 
$$C_{IN} = \frac{1}{2\pi f_{CIN}R_{IN}}$$

# CHARGE PUMP FLYING CAPACITOR AND PVSS CAPACITOR

The charge pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The PVSS capacitor must be at least equal to the charge pump capacitor in order to allow maximum charge transfer. Low ESR capacitors are an ideal selection, and a value of  $10\mu F$  is typical. Capacitor values that are smaller than  $10\mu F$  can be used, but the maximum output power is reduced and the device may not operate to specifications

#### **DECOUPLING CAPACITORS**

The IS31AP4915A require adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1µF, placed as close as possible to the device  $V_{CC}$  lead works best. Placing this decoupling capacitor close to the IS31AP4915A is important for the performance of the amplifier. For filtering lower frequency noise signals, a 10µF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

#### LAYOUT RECOMMENDATIONS

The SGND and PGND pins of the IS31AP4915A must be routed separately back to the decoupling capacitor in order to provide proper device operation. If the SGND and PGND pins are connected directly to each other, the part functions without risk of failure, but the noise and THD performance do not meet the specifications.



# **CLASSIFICATION REFLOW PROFILES**

Profile Feature	Pb-Free Assembly	
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds	
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds	
Peak package body temperature (Tp)*	Max 260°C	
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds	
Average ramp-down rate (Tp to Tsmax)	6°C/second max.	
Time 25°C to peak temperature	8 minutes max.	

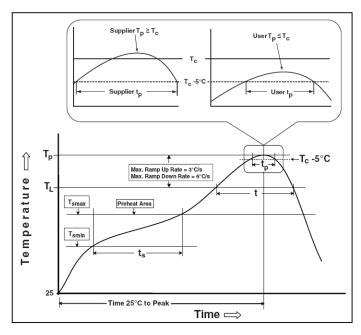
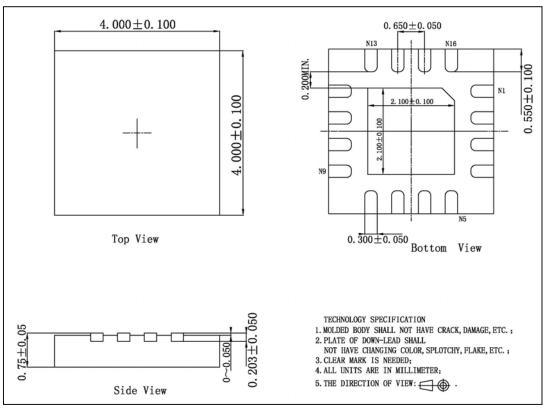


Figure 8 Classification Profile



# **PACKAGE INFORMATION**

#### QFN-16



Note: All dimensions in millimeters unless otherwise stated.