DS2174
EBERT

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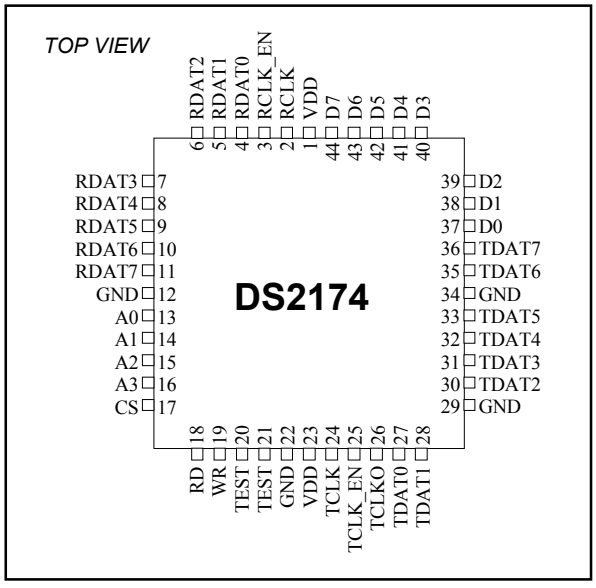
GENERAL DESCRIPTION

The DS2174 enhanced bit error-rate tester (EBERT) is a software-programmable test-pattern generator, receiver, and analyzer capable of meeting the most stringent error-performance requirements of digital transmission facilities. It features bit-serial, nibble-parallel, and byte-parallel data interfaces, and generates and uniquely synchronizes to pseudorandom patterns of the form 2^n - 1, where n can take on values from 1 to 32, and user-defined repetitive patterns of any length up to 512 octets.

APPLICATIONS

- Routers
- Channel Service Units (CSUs)
- Data Service Units (DSUs)
- Muxes
- Switches
- Digital-to-Analog Converters (DACs)
- CPE Equipment
- Bridges
- Smart Jack

PIN CONFIGURATION



FEATURES

- Generates and detects digital patterns for analyzing and trouble-shooting digital communications systems
- Programmable polynomial length and feedback taps for generation of any pseudorandom patterns up to 2^{32} - 1; up to 32 taps can be used in the feedback path
- Programmable, user-defined pattern registers for long repetitive patterns up to 512 bytes in length
- Large 48-bit count and bit error count registers
- Software-programmable bit error insertion
- Fully independent transmit and receive paths
- 8-bit parallel-control port
- Detects polynomial test patterns in the presence of bit error rates up to 10^{-2}
- Programmable for serial, 4-bit parallel, or 8-bit parallel data interfaces
- Serial mode clock rate is 155MHz; byte mode is 80MHz for a net 622Mbps; OC-3
- Available in 44-pin PLCC

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS2174Q	0°C to +70°C	44 PLCC
DS2174QN	-40°C to +85°C	44 PLCC

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

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1. GENERAL OPERATION

1.1 Pattern Generation

1.1.1 Polynomial Generation

The DS2174 has a tap select register that can be used as a mask to tap up to 32 bits in the feedback path of the polynomial generator. It also features a seed register that can be used to preload the polynomial generator with a seed value. This is done on the rising edge of TL in Control Register 1.

The DS2174 generates polynomial patterns of any length up to and including 2^{32} - 1. All of the industry-standard polynomials can be programmed using the control registers. The polynomial is generated using a shift register of programmable length and programmable feedback tap positions. The user has access to all combinations of pattern length and pattern tap location to generate industry-standard polynomials or other combinations as well. In addition, the QRSS pattern described in T1.403 is described by the polynomial 2^{20} – 1. This pattern has the additional requirement that "an output bit is forced to a 1 whenever the next 14 bits are 0." Setting the QRSS bit in Control Register 1 causes the pattern generator to enforce this rule.

1.1.2 Repetitive Pattern Generation

In addition to polynomial patterns, the DS2174 generates repetitive patterns of considerable length. The programmer has access to 512 bytes of memory for storing pattern. The pattern length bits PL0 through PL8, located at addresses 02h and 03h, are used to program the length of the repetitive pattern. Memory is addressed indirectly and is used to store the pattern. Data can be sent MSB or LSB first as it appears in the memory.

Repetitive patterns can include simple patterns such as 3 in 24, but the additional memory can be used to store patterns such as DDS-n patterns or T1-n patterns. Repetitive patterns are stored in increments of 8 bits. To generate a repetitive pattern that is 12 bits long (3 nibbles), the pattern is written twice such that the pattern is 24 bits long (3 bytes), and repeats twice in memory. The same is true when the device is used in serial mode: a 5-bit pattern is written to memory 5 times. For example,

To generate a 00001 pattern at the serial output, write these bytes to memory:

RAM ADDRESS	BINARY CODE	HEX CODE
00h	00010000	10h
01h	01000010	42h
02h	00001000	08h
03h	00100001	21h
04h	10000100	84h

1.2 Pattern Synchronization

1.2.1 Synchronization

The receiver synchronizes to the same pattern that is being transmitted. The pattern must be error free when the synchronizer is online. Once synchronized, an error density of 6 bits in 64 causes the receiver to declare loss-of-pattern sync, set the RLOS bit, and the synchronizer comes back online.

1.2.2 Polynomial Synchronization

Synchronization to polynomial patterns take 50 + n clock cycles (14 + n in nibble mode, 8 + n in byte mode), where n is the exponent in the polynomial that describes the pattern. Once synchronized, any bit that does not match the polynomial is counted as a bit error.

1.2.3 Repetitive Pattern Synchronization

Synchronization to repetitive patterns can take several complete repetitions of the entire pattern. The actual sync time depends on the nature of the pattern and the location of the synchronization pointer. Errors that occur during synchronization could affect the sync time; at least one complete error-free repetition must be received before synchronization is declared. Once synchronized, any bit that does not match the pattern that is programmed in the on-board RAM is counted as a bit error.

1.3 Bit Error Rate (BER) Calculation

1.3.1 Counters

The bit counter is active at all times. Once synchronized, the error counters come online. The receiver has large 48-bit count registers. These counters accumulate for 50,640 hours at the T1 line rate, 1.544MHz, and 38,170 hours at the E1 line rate, 2.048MHz. At higher clock rates, the counters saturate quicker, but at the T3 line rate, the counter still runs for almost 1500 hours, and at 155MHz it runs for 504 hours.

To accumulate BER data, the user toggles the LC bit at T = 0. This clears the accumulators and loads the contents into the count registers. At T = 0, these results should be ignored. At this point, the device is counting bits and bit errors. At the end of the specified time interval, the user toggles the LC bit again and reads the count registers. These are the valid results used to calculate a bit error rate. Remember, the bit counter is really counting clocks, so in nibble and byte modes the bit counter value needs to be multiplied by 4 or 8 to get the correct bit count. For longer integration periods, the results of multiple read cycles have to be accumulated in software.

1.4 Generating Errors

Through Control Register 2, the user can intentionally inject a particular error rate into the transmitted data stream. Injecting errors allows users to stress communication links and to check the functionality of error monitoring equipment along the path.

1.5 Clock Discussion

There are two methods for moving test patterns through a telecom network.

1) The clock applied to TCLK and RCLK can be gapped by other devices on the target system. The gapped clock would be applied to TCLK and RCLK only during the appropriate times. TDATn outputs remain active during clock gaps.
2) The clock applied to TCLK and RCLK can be continuous at the applicable line rate and the TCLK_EN and RCLK_EN pins can be asserted and deasserted during the appropriate time slots. TDATn outputs remain active even when TCLK_EN is pulled low. The output level remains static at the level of the last bit transmitted (output high for a 1, output low for a 0).

1.6 Power-Up Sequence

On power-up, the registers in the DS2174 are in a random state. The user must program all the internal registers to a known state before proper operation can be ensured.

Figure 1-1. Block Diagram

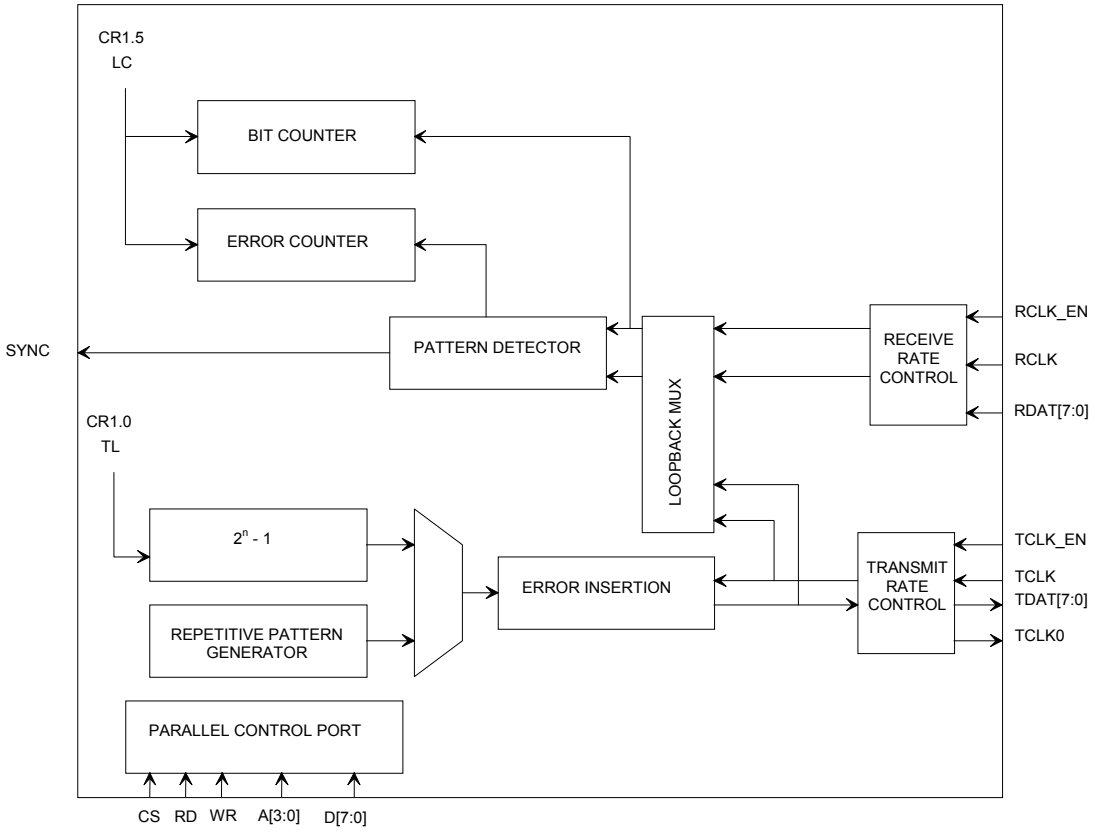


Table 1-A. Pin Assignment

PIN	SYMBOL	I/O	FUNCTION
1, 23	VDD	—	Supply
2	RCLK	I	Receive Clock
3	RCLK_EN	I	Receive Clock Enable
4	RDAT0	I	Receive Serial Data or LSB of Receive Nibble or Byte Data
5	RDAT1	I	Receive Data Nibble or Byte
6	RDAT2	I	Receive Data Nibble or Byte
7	RDAT3	I	Receive Data Nibble or Byte
8	RDAT4	I	Receive Data Byte
9	RDAT5	I	Receive Data Byte
10	RDAT6	I	Receive Data Byte
11	RDAT7	I	Receive Data Byte
12, 22, 29, 34	GND	—	Ground
13	A0	I	Address 0
14	A1	I	Address 1
15	A2	I	Address 2
16	A3	I	Address 3
17	CS	I	Chip Select
18	RD	I	Read
19	WR	I	Write
20, 21	TEST	I	Test Input
24	TCLK	I	Transmit Clock Input
25	TCLK_EN	I	Transmit Clock Enable
26	TCLKO	O	Transmit Clock Output. This is active only when data is being transmitted. This clock has gapped periods corresponding to the times when the transmit enable signal is low.
27	TDAT0	O	Transmit Serial Data or LSB of Transmit Nibble or Byte Data
28	TDAT1	O	Transmit Data Nibble or Byte
30	TDAT2	O	Transmit Data Nibble or Byte
31	TDAT3	O	Transmit Data Nibble or Byte
32	TDAT4	O	Transmit Data Byte
33	TDAT5	O	Transmit Data Byte
35	TDAT6	O	Transmit Data Byte
36	TDAT7	O	Transmit Data Byte
37	D0	I/O	Data I/O
38	D1	I/O	Data I/O
39	D2	I/O	Data I/O
40	D3	I/O	Data I/O
41	D4	I/O	Data I/O
42	D5	I/O	Data I/O
43	D6	I/O	Data I/O
44	D7	I/O	Data I/O

1.7 Detailed Pin Description

Signal Name: **RCLK**
Signal Description: **Receive Clock**
Signal Type: **Input**
Receive clock input. Up to a 155MHz clock to operate the receive circuit. Input data at RDATn is sampled on the rising edge of RCLK.

Signal Name: **RCLK_EN**
Signal Description: **Receive Clock Enable**
Signal Type: **Input**
Gaps the RCLK input to the receive circuit.

Signal Name: **RDAT0 to RDAT7**
Signal Description: **Receive Data Inputs**
Signal Type: **Input**
RDAT0. Receive serial data/receive data bit 0 in nibble and byte mode
RDAT1. Receive data bit 1 in nibble and byte mode
RDAT2. Receive data bit 2 in nibble and byte mode
RDAT3. Receive data bit 3 in nibble and byte mode
RDAT4. Receive data bit 4 in byte mode
RDAT5. Receive data bit 5 in byte mode
RDAT6. Receive data bit 6 in byte mode
RDAT7. Receive data bit 7 in byte mode

Signal Name: **A0 to A3**
Signal Description: **Address Inputs**
Signal Type: **Input**
Address bus for addressing the control registers.

Signal Name: **CS**
Signal Description: **Chip Select**
Signal Type: **Input**
Active-low signal. Must be low to read or write to the part.

Signal Name: **RD**
Signal Description: **Read Strobe**
Signal Type: **Input**
Active-low signal. Must be low to read from the part.

Signal Name: **WR**
Signal Description: **Write Strobe**
Signal Type: **Input**
Active-low signal. Must be low to write to the part.

Signal Name: **TEST**
Signal Description: **TEST Input**
Signal Type: **Input (with internal 10kΩ pullup)**
Test Input. Should be left floating or held high.

Signal Name: **TEST**
Signal Description: **TEST Input**
Signal Type: **Input (with internal 10kΩ pullup)**
Test Input. Should be left floating or held high.

Signal Name: **TCLK**
Signal Description: **Transmit Clock**
Signal Type: **Input**
Transmit Clock Input. Up to a 155MHz clock to operate the transmit circuit. Data is output at TDATn and is updated on the rising edge of TCLK.

Signal Name: **TCLK_EN**
Signal Description: **Transmit Clock Enable**
Signal Type: **Input**
Gaps the TCLK input to the transmit circuit.

Signal Name: **TCLKO**
Signal Description: **TCLK Output**
Signal Type: **Output**
Output of the TCLK gapping circuit. Gapped by TCLK_EN.

Signal Name: **TDAT0 to TDAT7**
Signal Description: **Transmit Data Outputs**
Signal Type: **Output**
TDAT0. Transmit serial data/receive data bit 0 in nibble and byte mode
TDAT1.Transmit data bit 1 in nibble and byte mode
TDAT2. Transmit data bit 2 in nibble and byte mode
TDAT3. Transmit data bit 3 in nibble and byte mode
TDAT4. Transmit data bit 4 in byte mode
TDAT5. Transmit data bit 5 in byte mode
TDAT6. Transmit data bit 6 in byte mode
TDAT7. Transmit data bit 7 in byte mode

Signal Name: **D0 to D7**
Signal Description: **Data I/O**
Signal Type: **I/O**
Parallel data pins.

2. PARALLEL CONTROL INTERFACE

Access to the registers is provided through a nonmultiplexed parallel port. The data bus is 8 bits wide; the address bus is 4 bits wide. Control registers are accessed directly; memory for long repetitive patterns is accessed indirectly. RCLK and TCLK are used to update counters and for all rising edge bits in the register map (RSYNC, LC, TL, SBE). At slow clock rates, sufficient time must be allowed for these port operations.

Table 2-A. Register Map

ADDRESS	R/W	REGISTER NAME
00	R/W	Control Register 1
01	R/W	Control Register 2
02	R/W	Control Register 3
03	R/W	Control Register 4
04	R	Status Register
05	R/W	Tap/Seed Register 0
06	R/W	Tap/Seed Register 1
07	R/W	Tap/Seed Register 2
08	R/W	Tap/Seed Register 3
09	R/W	TEST Register
0A	R	Count Register 0
0B	R	Count Register 1
0C	R	Count Register 2
0D	R	Count Register 3
0E	R	Count Register 4
0F	R	Count Register 5

3. CONTROL REGISTERS

Control Register 1 (Address = 0h)

(MSB) (LSB)

SYNCE	RSYNC	LC	LPBK	QRSS	PS	LSB	TL

SYMBOL	FUNCTION
SYNCE	**SYNC Enable** 0 = Auto resync enabled 1 = Auto resync disabled
RSYNC	**Initiate Manual Resync Process.** A rising edge causes the device to go out of sync and begin resynchronization process.
LC	**Latch Count Registers.** A rising edge copies the bit count and bit error count accumulators to the appropriate registers. The accumulators are then cleared.
LPBK	**Transmit/Receive Loopback Select** 0 = Loopback disabled 1 = Loopback enabled
QRSS	**Zero Suppression Select.** Forces a 1 into the pattern whenever the next 14 bit positions are all 0's. Should only be set when using the QRSS pattern. 0 = Disable 14 zero suppression 1 = Enable 14 zero suppression per T1.403
PS	**Pattern Select** 0 = Pseudorandom pattern 1 = Repetitive pattern
LSB	**LSB/MSB** 0 = Repetitive pattern data is transmitted/received MSB first 1 = Repetitive pattern data is transmitted/received LSB first
TL	**Transmit Load.** A rising edge causes the transmit shift register to be loaded with the seed value.

Control Register 2 (Address = 1h)

(MSB) (LSB)

MODE1	MODE0	TINV	RINV	SBE	EIR2	EIR1	EIR0

SYMBOL	FUNCTION
MODE1	**Mode Select Bit 1** (Table 3-A)
MODE0	**Mode Select Bit 0** (Table 3-A)
TINV	**Transmit Data Inversion Select** 0 = Do not invert outbound data 1 = Invert outbound data
RINV	**Receive Data Inversion Select** 0 = Do not invert inbound data 1 = Invert inbound data
SBE	**Single Bit Error Insert.** A rising edge causes the device to insert a single error in the outbound data. Must be cleared by the user.
EIR2	**Error Insert Bit 2** (Table 3-B)
EIR1	**Error Insert Bit 1** (Table 3-B)
EIR0	**Error Insert Bit 0** (Table 3-B)

3.1 Mode Select

The DS2174 is configured to operate in bit, nibble, or byte mode by using the MODE1/MODE0 bits in Control Register 2.

Table 3-A. Mode Select

MODE1	MODE0	OPERATION MODE
0	0	Bit
0	1	Nibble
1	0	Byte
1	1	Invalid

3.1.1 Error Insertion

The DS2174 inserts bit errors at a particular rate by setting the error insertion bits in Control Register 2 (Table 3-B). In addition, the device inserts errors on command by setting the SBE bit in Control Register 2. The bit that occurs after the rising edge of the SBE insert bit is inverted. In the case of the QRSS pattern, this could result in a string of 0's longer than 14 bits; the DS2174 delays the erred bit by 1 clock cycle.

Data in the nibble and byte modes is presented 4 or 8 bits at a time. When in nibble or byte mode and selecting 10^{-1} error rate, the device actually produces an error rate of 8^{-1}. When in byte mode and selecting an error rate of 10^{-2}, the device produces an error rate of 8^{-2}.

Table 3-B. Error Bit Insertion

EIR2	EIR1	EIR0	ERROR RATE	SERIAL	NIBBLE	BYTE
0	0	0	None	✓	✓	✓
0	0	1	10^{-1}	✓	8^{-1}	8^{-1}
0	1	0	10^{-2}	✓	✓	8^{-2}
0	1	1	10^{-3}	✓	✓	✓
1	0	0	10^{-4}	✓	✓	✓
1	0	1	10^{-5}	✓	✓	✓
1	1	0	10^{-6}	✓	✓	✓
1	1	1	10^{-7}	✓	✓	✓

Control Register 3 (Address = 2h)

(MSB) (LSB)

PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0

SYMBOL	FUNCTION
PL7	**Pattern Length Bit 7.** Bit 7 of [8:0] end address of repetitive pattern data.
PL6	**Pattern Length Bit 6.** Bit 6 of [8:0] end address of repetitive pattern data.
PL5	**Pattern Length Bit 5.** Bit 5 of [8:0] end address of repetitive pattern data.
PL4	**Pattern Length Bit 4.** Bit 4 of [8:0] end address of repetitive pattern data.
PL3	**Pattern Length Bit 3.** Bit 3 of [8:0] end address of repetitive pattern data.
PL2	**Pattern Length Bit 2.** Bit 2 of [8:0] end address of repetitive pattern data.
PL1	**Pattern Length Bit 1.** Bit 1 of [8:0] end address of repetitive pattern data.
PL0	**Pattern Length Bit 0.** Bit 0 of [8:0] end address of repetitive pattern data.

Control Register 4 (Address = 3h)

(MSB) (LSB)

TEST	TEST	CLK_INV	R/W	RAM	COUNT	SEED	PL8

SYMBOL	FUNCTION
TEST	**Factory Use.** Must be set to 0 for proper operation.
TEST	**Factory Use.** Must be set to 0 for proper operation.
CLK_INV	**TCLKO Invert.** 0 = TCLKO polarity is normal 1 = TCLKO polarity is inverted
R/W	**Read/Write Select.** This bit is used with the RAM bit to read or write the RAM. 0 = Write to the RAM 1 = Read from the RAM
RAM	**RAM Select.** This bit should be set when repetitive pattern data is being loaded into the RAM. See flowchart in Section 4 for a description of this process. 0 = BERT state machine has control of the RAM 1 = Parallel port has read and write access to the RAM
COUNT	**Select Bit for Registers Ah–Fh.** 0 = Registers Ah–Fh refer to bit count registers. 1 = Registers Ah–Fh refer to error count registers.
SEED	**Select Bit for Registers 5h–8h.** 0 = Registers 5h–8h refer to tap select registers. 1 = Registers 5h–8h refer to preload seed registers.
PL8	**Pattern Length Bit 8.** Bit 8 of [8:0] End Address of Repetitive Pattern Data.

3.2 Status Register

The status register contains information about the real-time status of the DS2174. When a particular event has occurred, the appropriate bit in the register is set to a 1. All of the bits in this register (except for SYNC) operate in a latched fashion, which means that if an event occurs and a bit is set to a 1, it remains set until the user reads the register. For the BED, BCOF, and BECOF bits, they are cleared when read and are not set again until the event has occurred again. For RLOS, RA0, and RA1 bits, they are cleared when read if the condition no longer persists.

Status Register (Address = 4h)

(MSB) (LSB)

—	RA1	RA0	BED	BECOF	BCOF	RLOS	SYNC

SYMBOL	FUNCTION
—	**Not Assigned.** Could be any value.
RA1	**Receive All 1s.** Set when 40 consecutive 1s are received in pseudorandom mode. Allowed to be cleared when a 0 is received.
RA0	**Receive All 0s.** Set when 40 consecutive 0s are received in pseudorandom mode. Allowed to be cleared when a 1 is received.
BED	**Bit Error Detection.** Set when bit error count is non-zero. Cleared when read.
BECOF	**Bit Error Count Overflow.** Set when the bit error counter overflows. Cleared when read.
BCOF	**Bit Counter Overflow.** Set when the bit counter overflows. Cleared when read.
RLOS	**Receive Loss-of-Sync.** Set when the receiver is searching for synchronization. Remains set until read once sync is achieved. This bit is latched.
SYNC	**Sync.** Real-time status of the synchronizer. This bit is not latched.

3.3 Pseudorandom Pattern Registers

Note: *Bit 1 of Control Register 4 determines if the addresses point to the tap select or seed registers.*

The tap select register is used to select the length and tap positions for pseudorandom generation/reception. Each bit that is set to a 1 denotes a tap at that location for the feedback path. The highest bit location set to a 1 is the length of the shift register. All pattern lengths are available in bit mode, patterns $2^4 - 1$ and greater are available in nibble mode, and patterns $2^8 - 1$ and greater are available in byte mode. The pattern generator generates all 1's if the exponent in the polynomial is less than 4 (nibble mode) or 8 (byte mode).

For example, to transmit/receive $2^{15} - 1$ (O.151) Bit14 and Bit13 would be set to a 1. All other bits would be 0. Table 3-C gives tap select and seed values for many pseudorandom patterns. The seed value is loaded into the transmit shift register on the rising edge of TL (CR1.0).

Tap Select/Seed Value Registers (Address = 5h–8h)

(MSB) (LSB)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT9	BIT8
BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16
BIT31	BIT30	BIT29	BIT28	BIT27	BIT26	BIT25	BIT24

Table 3-C. Pseudorandom Pattern Generation

PATTERN TYPE	TAP0	TAP1	TAP2	TAP3	SEED0/1/2/3	TINV	RINV
$2^3 - 1$ (Notes 1 and 2)	05	00	00	00	FF	0	0
$2^4 - 1$ (Note 1)	09	00	00	00	FF	0	0
$2^5 - 1$ (Note 1)	12	00	00	00	FF	0	0
$2^6 - 1$ (Note 1)	30	00	00	00	FF	0	0
$2^7 - 1$ Fractional T1 LB Activate (Note 1)	48	00	00	00	FF	0	0
$2^7 - 1$ Fractional T1 LB Deactivate (Note 1)	48	00	00	00	FF	1	1
$2^7 - 1$ (Note 1)	41	00	00	00	FF	0	0
$2^8 - 1$ Maximal Length	B8	00	00	00	FF	0	0
$2^9 - 1$ O.153 (511 Type)	10	01	00	00	FF	0	0
$2^{10} - 1$	40	02	00	00	FF	0	0
$2^{11} - 1$ O.152 and O.153 (2047 Type)	00	05	00	00	FF	0	0
$2^{12} - 1$ Maximal Length	29	08	00	00	FF	0	0
$2^{13} - 1$ Maximal Length	0D	10	00	00	FF	0	0
$2^{14} - 1$ Maximal Length	15	20	00	00	FF	0	0
$2^{15} - 1$ O.151	00	60	00	00	FF	1	1
$2^{16} - 1$ Maximal Length	08	D0	00	00	FF	0	0
$2^{17} - 1$	04	00	01	00	FF	0	0
$2^{18} - 1$	40	00	02	00	FF	0	0
$2^{19} - 1$ Maximal Length	23	00	04	00	FF	0	0
$2^{20} - 1$ O.153	04	00	08	00	FF	0	0
$2^{20} - 1$ O.151 QRSS (CR1.3 = 1)	00	00	09	00	FF	0	0
$2^{21} - 1$	02	00	10	00	FF	0	0
$2^{22} - 1$	01	00	20	00	FF	0	0
$2^{23} - 1$ O.151	00	00	42	00	FF	1	1
$2^{24} - 1$ Maximal Length	00	00	E1	00	FF	0	0
$2^{25} - 1$	04	00	00	01	FF	0	0
$2^{26} - 1$ Maximal Length	23	00	00	02	FF	0	0
$2^{27} - 1$ Maximal Length	13	00	00	04	FF	0	0
$2^{28} - 1$	04	00	00	08	FF	0	0
$2^{29} - 1$	02	00	00	10	FF	0	0
$2^{30} - 1$ Maximal Length	29	00	00	20	FF	0	0
$2^{31} - 1$	04	00	00	40	FF	0	0
$2^{32} - 1$ Maximal Length	03	00	20	80	FF	0	0

Note 1: These pattern types do not work in byte mode.
Note 2: These pattern types do not work in nibble mode.

3.4 Test Register

Test register used for factory test. All bits must be set to 0 for proper operation.

Test Register (Address = 9h)

(MSB)							(LSB)
TEST	TEST	TEST	TEST	TEST	TEST	TEST	TEST

SYMBOL	FUNCTION
TEST	**Factory Use.** Must be set to 0 for proper operation.
TEST	**Factory Use.** Must be set to 0 for proper operation.
TEST	**Factory Use.** Must be set to 0 for proper operation.
TEST	**Factory Use.** Must be set to 0 for proper operation.
TEST	**Factory Use.** Must be set to 0 for proper operation.
TEST	**Factory Use.** Must be set to 0 for proper operation.
TEST	**Factory Use.** Must be set to 0 for proper operation.
TEST	**Factory Use.** Must be set to 0 for proper operation.

3.5 Count Registers

Note: *Bit 2 of Control Register 4 determines if the addresses point to the bit count or error count registers.*

The bit count registers comprise a 48-bit count of bits (actually RCLK cycles) received at RDAT. C47 is the MSB of the 48-bit count. The bit counter increments for each cycle of RCLK when RCLK_EN is high. The bit counter is enabled regardless of synchronization. The status register bit BCOF is set when this 48-bit register overflows. The counter rolls over upon an overflow condition. The DS2174 latches the bit count into the bit count registers and clears the internal bit count when the LC bit in Control Register 1 is toggled from low to high.

The error count registers comprise a 48-bit count of bits received in error at RDAT. The bit error counter is disabled during loss-of-sync. C47 is the MSB of the 48-bit count. The status register bit BECOF is set when this 48-bit register overflows. The counter rolls over upon an overflow condition. The DS2174 latches the bit count into the bit error count registers and clears the internal bit error count when the LC bit in Control Register 1 is toggled from low to high.

The bit count and bit error count registers are used by an external processor to compute the BER performance on a loop or channel basis.

Count Registers (Address = Ah–Fh)

(MSB)							(LSB)
C7	C6	C5	C4	C3	C2	C1	C0
C15	C14	C13	C12	C11	C10	C9	C8
C23	C22	C21	C20	C19	C18	C17	C16
C31	C30	C29	C28	C27	C26	C25	C24
C39	C38	C37	C36	C35	C34	C33	C32
C47	C46	C45	C44	C43	C42	C41	C40

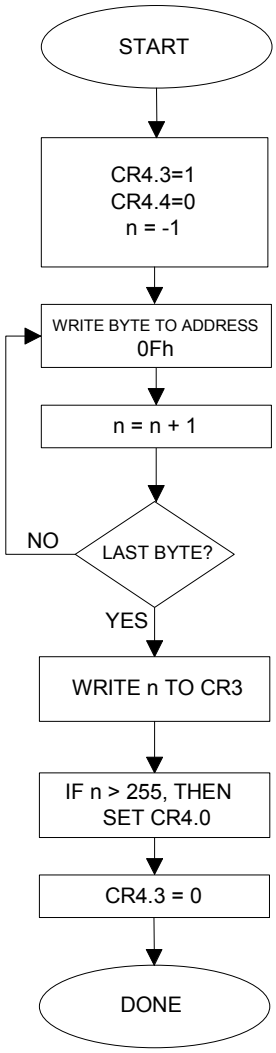
4. RAM ACCESS

4.1 Indirect Addressing

512 bytes of memory, which is addressed indirectly, are available for repetitive patterns. Data bytes are loaded one at a time into the indirect address register at address 0Fh. The RAM mode control bit, CR4.3, determines the access to the RAM. If CR4.3 = 0, the RAM is under control of the BERT state machine. If CR4.3 = 1, the RAM is under the control of the parallel port. This section discusses CR4.3 = 1.

The accompanying flow chart describes the algorithm used to write repetitive patterns to the RAM. The programmer initializes a counter (n) to -1 in software, then sets CR4.3 and clears CR4.4. The rising edge of CR4.3 resets the RAM address pointer to address 00h. Address 0Fh becomes the indirect access port to the RAM. A write cycle on the parallel port to address 0Fh writes to the address in RAM pointed to by the address pointer. The end of the write cycle, rising edge of WR, increments the address pointer. The programmer then increments the counter (n) by 1 and loops until the pattern load is complete. Clear CR4.3 to return control of the RAM to the BERT state machine. Finally, write the value in the counter (n) back to address 04h and 05h to mark the last address of the pattern in memory.

The RAM contents can be verified by executing the same algorithm, replacing the parallel-port write with a read, and setting CR4.4. CR4.3 must remain set for the entire algorithm to properly increment the address pointer.



5. DC OPERATION

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground	-1.0V to +5.5V
Operating Temperature Range for DS2174QN	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Soldering Temperature Range	See IPC/JEDEC J-STD-020A

This a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operation sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect reliability.

Table 5-A. RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to +70°C for DS2174Q; T_A = -40°C to +85°C for DS2174QN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.2		5.5	V	
Logic 0	V_{IL}	-0.3		+0.8	V	
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	
ESD Voltage, Any Pin			1500		V	1

NOTES:

1) Human body model.

Table 5-B. DC CHARACTERISTICS

(V_{DD} = 3.0V to 3.6V, T_A = 0°C to +70°C for DS2174Q; V_{DD} = 3.0V to 3.6V, T_A = -40°C to +85°C for DS2174QN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}		50	60	mA	1
Lead Capacitance	C_{IO}		7		pF	
Input Leakage	I_{IL}	-10		+10	µA	2
Input Leakage (with pullups)	I_{ILP}	-500		+500	µA	2
Output Leakage	I_{LO}	-10		+10	µA	3
Output Current at 2.4V	I_{OH}	-4.0			mA	
Output Current at 2.4V	I_{OH8}	-8.0			mA	4
Output Current at 0.4V	I_{OL}	+4.0			mA	
Output Current at 0.4V	I_{OL8}	+8.0			mA	4

NOTES:

1) TCLK = RCLK = 155MHz serial mode; outputs open-circuited or 80MHz byte mode.
2) $0V < V_{IN} < V_{DD}$.
3) Applies to TDAT when tri-stated.
4) Applies to TDAT[0] and TCLKO.

6. AC TIMING CHARACTERISTICS

6.1 Parallel Port

Figure 6-1. Read Timing

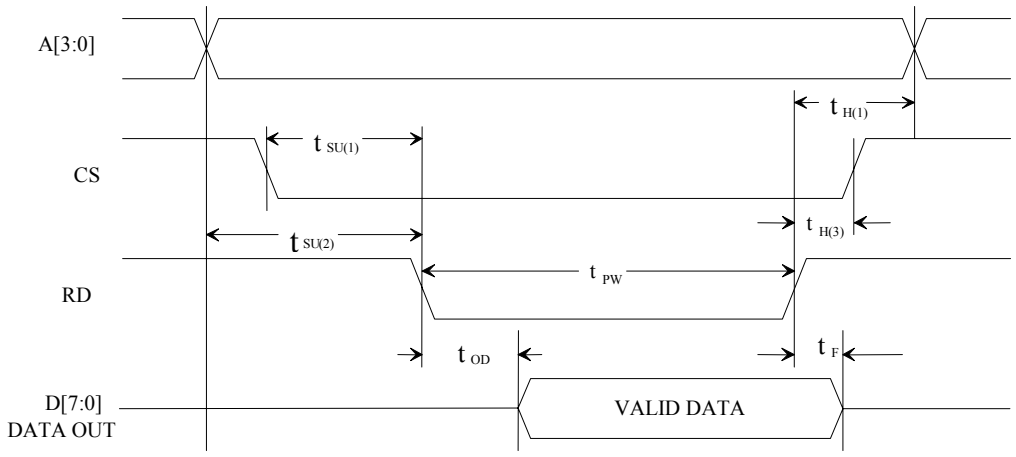


Table 6-A. PARALLEL PORT READ TIMING

(V_{DD} = 3.0V to 3.6V, T_A = 0°C to +70°C for DS2174Q; V_{DD} = 3.0V to 3.6V, T_A = -40°C to +85°C for DS2174QN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CS Setup Time Before RD↓	$t_{SU(1)}$	5.0			ns	
A(3:0) Setup Time Before RD↓	$t_{SU(2)}$	10.0			ns	
A(3:0) Hold Time After RD↑	$t_{H(1)}$	10.0			ns	
RD Pulse Width	t_{PW}	38			ns	
DATA Output Delay After RD↓	t_{OD}			8.0	ns	1
DATA Float Time After RD↑	t_F			2.0	ns	1
CS Hold Time After RD↑	$t_{H(3)}$	5.0			ns	

↑ = Rising Edge
↓ = Falling Edge

NOTES:

1) 50pF load.

Figure 6-2. Write Timing

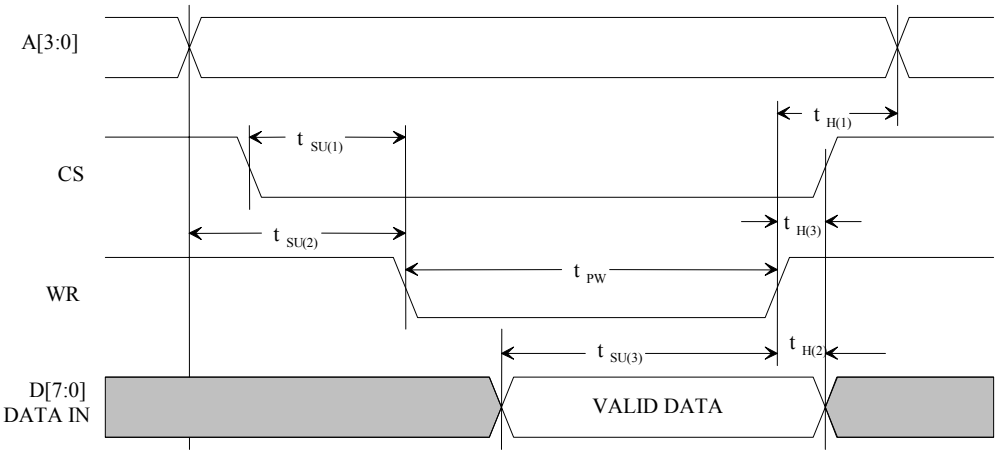


Table 6-B. PARALLEL PORT WRITE TIMING

(V_{DD} = 3.0V to 3.6V, T_A = 0°C to +70°C for DS2174Q; V_{DD} = 3.0V to 3.6V, T_A = -40°C to +85°C for DS2174QN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CS Setup Time Before WR↓	$t_{SU(1)}$	5.0			ns	
A(3:0) Setup Time Before WR↓	$t_{SU(2)}$	10.0			ns	
A(3:0) Hold Time After WR↑	$t_{H(1)}$	10.0			ns	
WR Pulse Width	t_{PW}	38			ns	
DATA Setup Time Before WR↑	$t_{SU(3)}$	10.0			ns	
DATA Hold Time After WR↑	$t_{H(2)}$	5.0			ns	
CS Hold Time After WR↑	$t_{H(3)}$	5.0			ns	

6.2 Data Interface

Figure 6-3. Transmit Interface Timing

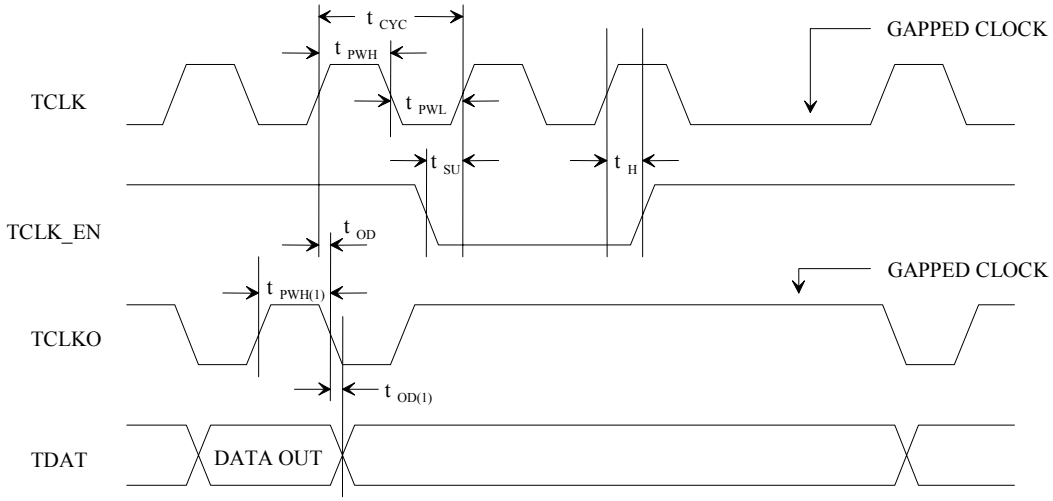


Table 6-C. TRANSMIT DATA TIMING

(V_{DD} = 3.0V to 3.6V, T_A = 0°C to +70°C for DS2174Q; V_{DD} = 3.0V to 3.6V, T_A = -40°C to +85°C for DS2174QN)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TCLK Clock Period (Nibble/Byte Mode)	t_{CYC}	12.5			ns	
TCLK High Time (Nibble/Byte Mode)	t_{PWH}	5.0	½ t_{CYC}		ns	
TCLK Low Time (Nibble/Byte Mode)	t_{PWL}	5.0	½ t_{CYC}		ns	
TCLK Clock Period (Bit Mode)	t_{CYC}	6.45			ns	3
TCLK High Time (Bit Mode)	t_{PWH}	2.0	½ t_{CYC}		ns	3
TCLK Low Time (Bit Mode)	t_{PWL}	2.0	½ t_{CYC}		ns	3
TCLK_EN Setup Time Before TCLK↑	t_{SU}	2.5			ns	
TCLK_EN Hold Time After TCLK↑	t_H	2.5			ns	
TCLKO Output Delay After TCLK↑	t_{OD}			6.0	ns	1
TCLKO High Time (Nibble/Byte Mode)	$t_{PWH(1)}$	5.0			ns	1
TCLKO High Time (Bit Mode)	$t_{PWH(1)}$	2.0			ns	1, 3
TDAT Output Delay After TCLKO↓	$t_{OD(1)}$			5.0	ns	1, 2

NOTES:

1) 20pF load.
2) TDAT follows falling edge of TCLKO if CR4.5 = 0, rising edge if CR4.5 = 1.
3) Guaranteed by design.

Figure 6-4. Receive Interface Timing

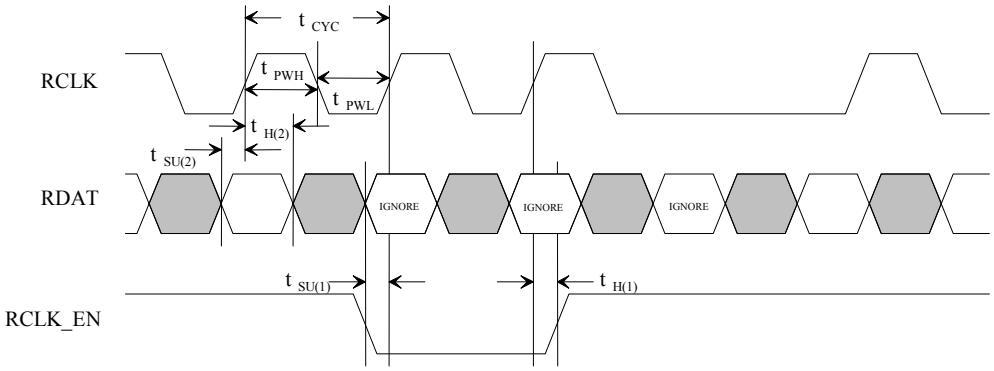


Table 6-D. RECEIVE DATA TIMING

(V_{DD} = 3.0V to 3.6V, T_A = 0°C to +70°C for DS2174Q; V_{DD} = 3.0V to 3.6V, T_A = -40°C to +85°C for DS2174QN)

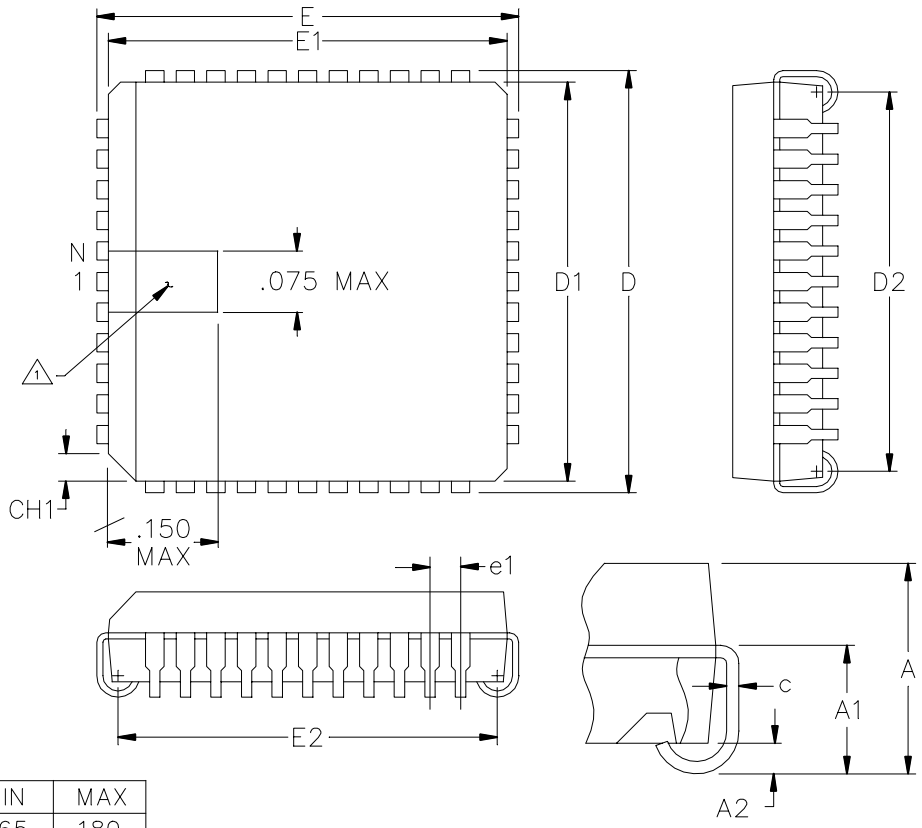
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLK Clock Period (Nibble/Byte Mode)	t_{CYC}	12.5			ns	
RCLK High Time (Nibble/Byte Mode)	t_{PWH}	5.0	½ t_{CYC}		ns	
RCLK Low Time (Nibble/Byte Mode)	t_{PWL}	5.0	½ t_{CYC}		ns	
RCLK Clock Period (Bit Mode)	t_{CYC}	6.45			ns	1
RCLK High Time (Bit Mode)	t_{PWH}	2.0	½ t_{CYC}		ns	1
RCLK Low Time (Bit Mode)	t_{PWL}	2.0	½ t_{CYC}		ns	1
RCLK_EN Setup Time Before RCLK↑	$t_{SU(1)}$	2.5			ns	
RCLK_EN Hold Time After RCLK↑	$t_{H(1)}$	2.5			ns	
RDAT(7:0) Setup Time Before RCLK↑	$t_{SU(2)}$	2.5			ns	
RDAT(7:0) Hold Time After RCLK↑	$t_{H(2)}$	2.5			ns	

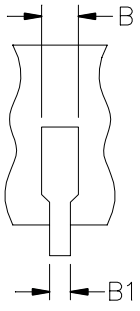
NOTES:

1) Guaranteed by design.

7. MECHANICAL DIMENSIONS

NOTE:
1. PIN–1 IDENTIFIER TO BE LOCATED IN ZONE INDICATED.
2. CONTROLLING DIMENSIONS ARE IN INCHS





LTR	MIN	MAX
A	.165	.180
A1	.090	.120
A2	.020	–
B	.026	.033
B1	.013	.021
c	.009	.012
CH1	.042	.048
D	.685	.695
D1	.650	.656
D2	.590	.630
E	.685	.695
E1	.650	.656
E2	.590	.630
e1	.050 BSC	
N	44	–