

FEATURES:

- Typical $t_{sk(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model ($C = 200\text{pF}$, $R = 0$)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, Normal Range
- $V_{CC} = 2.7\text{V}$ to 3.6V , Extended Range
- CMOS power levels ($0.4\mu\text{W}$ typ. static)
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVC16501A:

- High Output Drivers: $\pm 24\text{mA}$
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

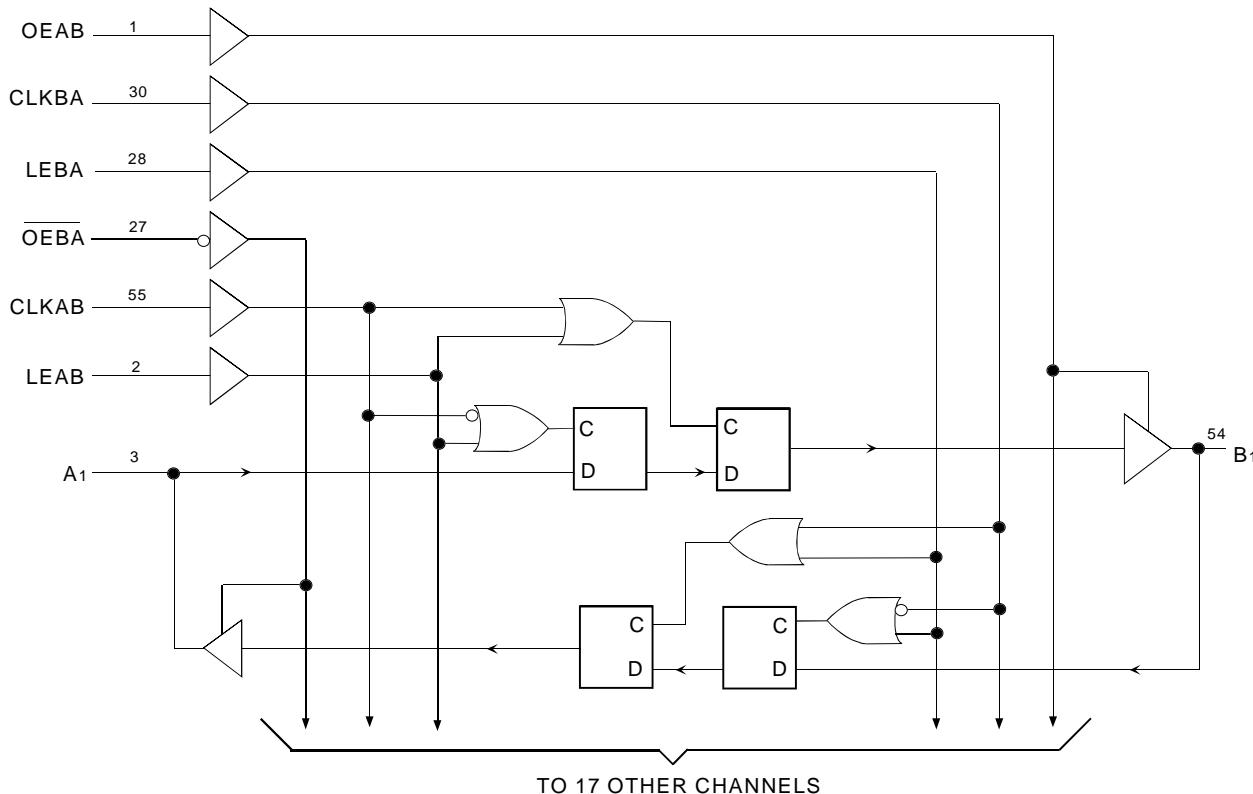
DESCRIPTION:

The LVC16501A is built using advanced dual metal CMOS technology. This high-speed, low power 18-bit registered bus transceiver combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes. Data flow in each direction is controlled by output-enable ($OEAB$ and \overline{OEBA}), latch enable ($LEAB$ and $LEBA$) and clock ($CLKAB$ and $CLKBA$) inputs. For A-to-B data flow, the device operates in transparent mode when $LEAB$ is high. When $LEAB$ is low, the A data is latched if $CLKAB$ is held at a high or low logic level. If $LEAB$ is low, the A bus data is stored in the latch/flip-flop on the low-to-high transition of $CLKAB$. $OEAB$ performs the output enable function on the B port. Data flow from B port to A port is similar but requires using \overline{OEBA} , $LEBA$ and $CLKBA$. Flow-through organization of signal pins simplifies layout. All inputs are designed with hysteresis for improved noise margin.

The LVC16501A has been designed with a $\pm 24\text{mA}$ output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

Functional Block Diagram



PIN CONFIGURATION

OEAB	1	56	GND
LEAB	2	55	CLKAB
A ₁	3	54	B ₁
GND	4	53	GND
A ₂	5	52	B ₂
A ₃	6	51	B ₃
V _{CC}	7	50	V _{CC}
A ₄	8	49	B ₄
A ₅	9	48	B ₅
A ₆	10	47	B ₆
GND	11	46	GND
A ₇	12	45	B ₇
A ₈	13	44	B ₈
A ₉	14	SO56-1	SO56-2
A ₁₀	15	SO56-2	SO56-3
A ₁₁	16	41	B ₉
A ₁₂	17	40	B ₁₀
GND	18	39	GND
A ₁₃	19	38	B ₁₁
A ₁₄	20	37	B ₁₂
A ₁₅	21	36	B ₁₃
V _{CC}	22	35	B ₁₄
A ₁₆	23	34	B ₁₅
A ₁₇	24	33	B ₁₆
GND	25	32	GND
A ₁₈	26	31	B ₁₇
OEBA	27	30	CLKBA
LEBA	28	29	GND

SSOP/TSSOP/TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	- 0.5 to +6.5	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	- 0.5 to +6.5	V
T _{STG}	Storage Temperature	- 65 to +150	°C
I _{OUT}	DC Output Current	- 50 to +50	mA
I _{IK}	Continuous Clamp Current, V _I < 0 or V _O < 0	- 50	mA
I _{CC}	Continuous Current through each V _{CC} or GND	±100	mA
I _{SS}			

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NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	6.5	8	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	6.5	8	pF

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NOTE:

1. As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
OEAB	A-to-B Output Enable Input (Active HIGH)
OEBA	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
A _x	A-to-B Data Inputs or B-to-A 3-State Outputs
B _x	B-to-A Data Inputs or A-to-B 3-State Outputs

FUNCTION TABLE (1, 2)

Inputs				Outputs
OEAB	LEAB	CLKAB	Ax	Bx
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	L	X	B ⁽³⁾
H	L	H	X	B ⁽⁴⁾

NOTES:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance
↑ = LOW-to-HIGH Transition
2. A-to-B data flow is shown. B-to-A data flow is similar but uses \overline{OEBA} , \overline{LEBA} , and \overline{CLKBA} .
3. Output level before the indicated steady-state input conditions were established.
4. Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = -40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
VIH	Input HIGH Voltage Level	V _{CC} = 2.3V to 2.7V		1.7	—	—	V
		V _{CC} = 2.7V to 3.6V		2	—	—	
VIL	Input LOW Voltage Level	V _{CC} = 2.3V to 2.7V		—	—	0.7	V
		V _{CC} = 2.7V to 3.6V		—	—	0.8	
I _{IH} I _{IL}	Input Leakage Current	V _{CC} = 3.6V	V _I = 0 to 5.5V	—	—	±5	µA
I _{OZH} I _{OZL}	High Impedance Output Current (3-State Output pins)	V _{CC} = 3.6V	V _O = 0 to 5.5V	—	—	±10	µA
I _{OFF}	Input/Output Power Off Leakage	V _{CC} = 0V, V _{IN} or V _O ≤ 5.5V		—	—	±50	µA
V _{IK}	Clamp Diode Voltage	V _{CC} = 2.3V, I _{IN} = -18mA		—	-0.7	-1.2	V
V _H	Input Hysteresis	V _{CC} = 3.3V		—	100	—	mV
I _{ICL} I _{ICCH} I _{ICCZ}	Quiescent Power Supply Current	V _{CC} = 3.6V	V _{IN} = GND or V _{CC}	—	—	10	µA
			3.6 ≤ V _{IN} ≤ 5.5V ⁽²⁾	—	—	10	
ΔI _{CC}	Quiescent Power Supply Current Variation	One input at V _{CC} - 0.6V other inputs at V _{CC} or GND			—	—	500 µA

NOTES:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient.
2. This applies in the disabled state only.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = 2.3V to 3.6V	I _{OH} = - 0.1mA	V _{CC} - 0.2	—	V
		V _{CC} = 2.3V	I _{OH} = - 6mA	2	—	
		V _{CC} = 2.3V	I _{OH} = - 12mA	1.7	—	
		V _{CC} = 2.7V		2.2	—	
		V _{CC} = 3.0V		2.4	—	
		V _{CC} = 3.0V	I _{OH} = - 24mA	2.2	—	
V _{OL}	Output LOW Voltage	V _{CC} = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		V _{CC} = 2.3V	I _{OL} = 6mA	—	0.4	
		V _{CC} = 2.3V	I _{OL} = 12mA	—	0.7	
		V _{CC} = 2.7V	I _{OL} = 12mA	—	0.4	
		V _{CC} = 3.0V	I _{OL} = 24mA	—	0.55	

NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = - 40°C to +85°C.

OPERATING CHARACTERISTICS, V_{CC} = 3.3V ± 0.3V, T_A = 25°C

Symbol	Parameter	Test Conditions	Typical	Unit
CPD	Power Dissipation Capacitance per transceiver Outputs enabled	C _L = 0pF, f = 10Mhz	—	pF
CPD	Power Dissipation Capacitance per transceiver Outputs disabled		—	pF

SWITCHING CHARACTERISTICS (1)

Symbol	Parameter	V _{CC} = 2.7V		V _{CC} = 3.3V±0.3V		Unit
		Min.	Max.	Min.	Max.	
f _{MAX}		150	—	150	—	MHz
t _{P LH}	Propagation Delay Ax to Bx or Bx to Ax	1.5	5.1	1.5	4.6	ns
t _{P HL}	Propagation Delay LEBA to Ax, LEAB to Bx	1.5	5.6	1.5	5.3	ns
t _{P LH}	Propagation Delay CLKBA to Ax, CLKAB to Bx	1.5	5.6	1.5	5.3	ns
t _{P ZH}	Output Enable Time OEBA to Ax, OEAB to Bx	1.5	6	1.5	5.6	ns
t _{P ZL}	Output Disable Time OEBA to Ax, OEAB to Bx	1.5	5.6	1.5	5.2	ns
t _{SU}	Set-up Time, HIGH or LOW Ax to CLKAB, Bx to CLKBA	3	—	3	—	ns
t _H	Hold Time, HIGH or LOW Ax to CLKAB, Bx to CLKBA	0	—	0	—	ns
t _{SU}	Set-up Time HIGH or LOW	2.5	—	2.5	—	ns
	Ax to LEAB, Bx to LEBA	Clock HIGH	2.5	—	2.5	—
t _H	Hold Time HIGH or LOW Ax to LEAB, Bx to LEBA	1.5	—	1.5	—	ns
t _W	LEAB or LEBA Pulse Width HIGH or LOW	3	—	3	—	ns
t _W	CLKAB or CLKBA Pulse Width HIGH or LOW	3	—	3	—	ns
t _{SK(0)}	Output Skew ⁽²⁾	—	—	—	500	ps

NOTES:

1. See test circuits and waveforms. TA = -40°C to +85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

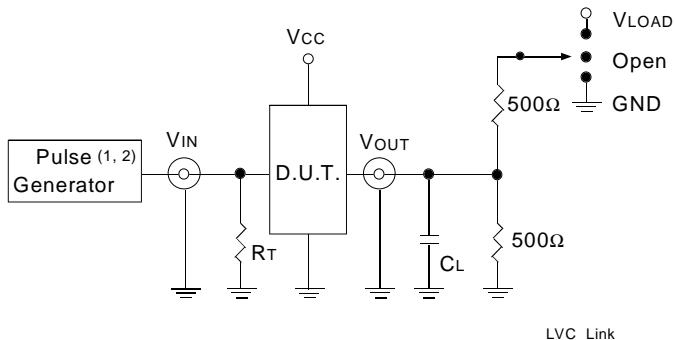
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC(1)} = 3.3V \pm 0.3V$	$V_{CC(1)} = 2.7V$	$V_{CC(2)} = 2.5V \pm 0.2V$	Unit
V_{LOAD}	6	6	$2 \times V_{CC}$	V
V_{IH}	2.7	2.7	V_{CC}	V
V_T	1.5	1.5	$V_{CC}/2$	V
V_{LZ}	300	300	150	mV
V_{HZ}	300	300	150	mV
C_L	50	50	30	pF

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TEST CIRCUITS FOR ALL OUTPUTS



DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
 R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

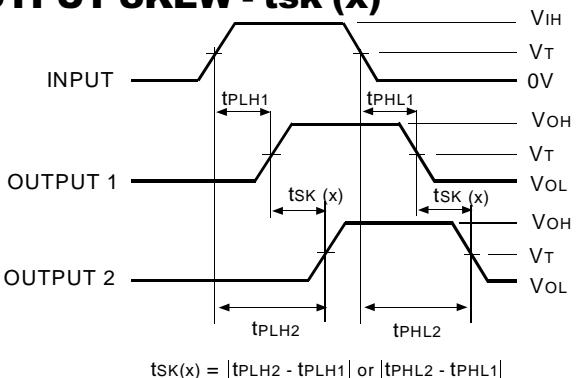
1. Pulse Generator for All Pulses: Rate ≤ 10 MHz; $t_f \leq 2.5$ ns; $t_r \leq 2.5$ ns.
2. Pulse Generator for All Pulses: Rate ≤ 10 MHz; $t_f \leq 2$ ns; $t_r \leq 2$ ns.

SWITCH POSITION

Test	Switch
Open Drain	V_{LOAD}
Disable Low	
Enable Low	
Disable High	GND
Enable High	
All Other tests	Open

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OUTPUT SKEW - $t_{SK}(x)$



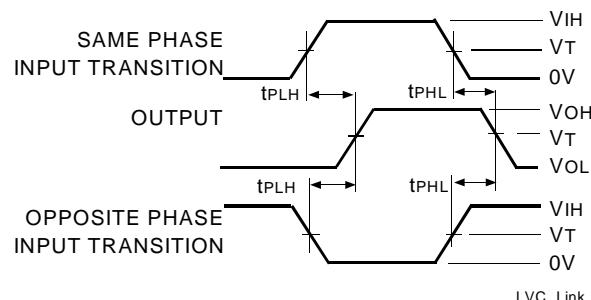
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PLH2} - t_{PLH1}|$$

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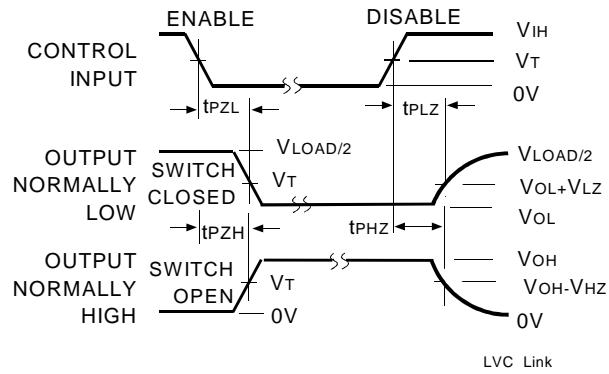
NOTES:

1. For $t_{SK}(o)$ OUTPUT1 and OUTPUT2 are any two outputs.
2. For $t_{SK}(b)$ OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



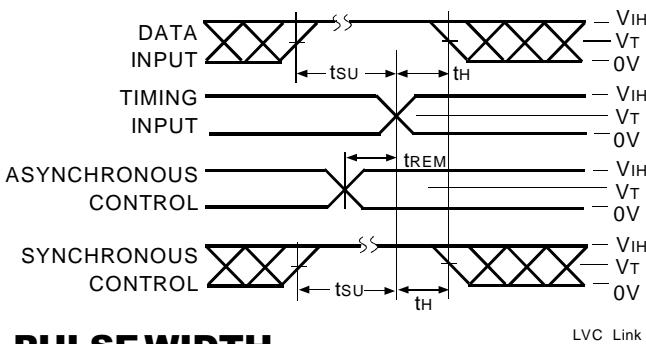
ENABLE AND DISABLE TIMES



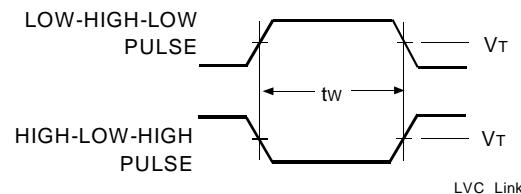
NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

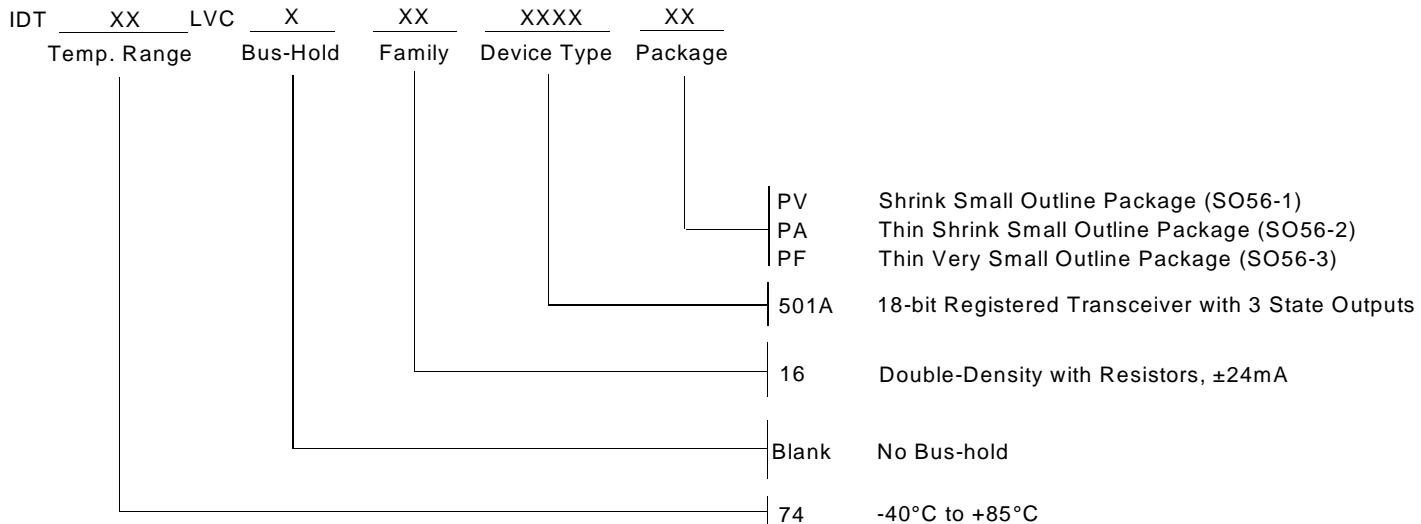
SET-UP, HOLD, AND RELEASE TIMES



PULSE WIDTH



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