FAIRCHILD SEMICONDUCTOR®

December 2012

KA317L
3-Terminal 0.1A Positive Adjustable Regulator

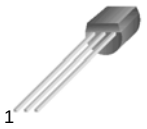
Features

- Output Current in Excess of 100 mA
- Output Adjustable Between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe Area Compensation
- Floating Operation for High-Voltage Applications

Description

The KA317L is a 3-terminal, adjustable, positive-voltage regulator capable of supplying in excess of 100 mA over an output voltage range of 1.2 V to 37 V. This voltage regulator requires only two external resistors to set the output voltage.

TO-92



1. Adj 2. Output 3. Input

Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method
KA317LZTA	0°C to +125°C	KA317LZ	TO-92	Ammo

Block Diagram

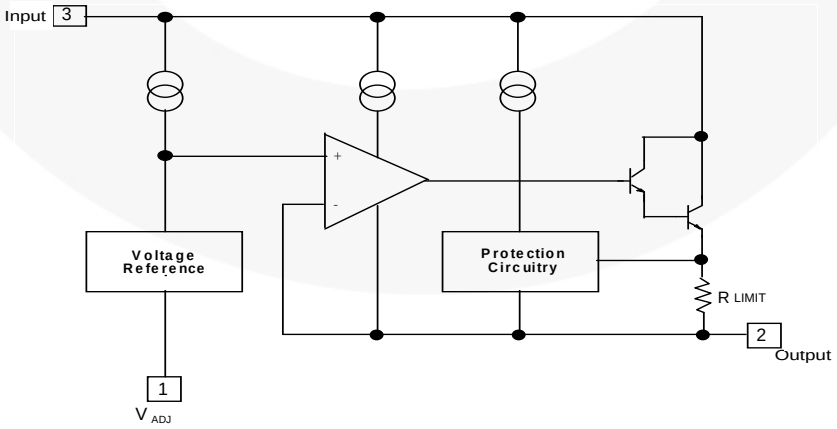


Figure 1. Block Diagram

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Value	Unit
V_I - V_O	Input-Output Voltage Differential	40	V
P_D	Power Dissipation	Internally limited	W
T_J	Operating Junction Temperature Range	0 ~ +125	°C
T_{STG}	Storage Temperature Range	-65 ~ +125	°C

Electrical Characteristics

V_I - V_O = 5 V, I_O = 40 mA, 0°C ≤ T_J ≤ +125°C, $P_{D(MAX)}$ = 625 mW, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
R_{LINE}	Line Regulation(1)	T_A = +25°C, 3 V ≤ V_I − V_O ≤ 40 V		0.01	0.04	%/V
		3 V ≤ V_I − V_O ≤ 40 V		0.02	0.07	%/V
R_{LOAD}	Load Regulation(1)	T_A = +25°C, 10 mA ≤ I_O ≤ 100 mA, V_O ≤ 5 V		5	25	mV
		T_A = +25°C, 10 mA ≤ I_O ≤ 100 mA, V_O ≥ 5 V		0.1	0.5	%/V_O
		10 mA ≤ I_O ≤ 100 mA, V_O ≤ 5 V		20	70	mV
		10 mA ≤ I_O ≤ 100 mA, V_O ≥ 5 V		0.3	1.5	%/V_O
I_{ADJ}	Adjustment Pin Current			50	100	µA
ΔI_{ADJ}	Adjustment Pin Current Change	3 V ≤ V_I - V_O ≤ 40 V, 10 mA ≤ I_O ≤ 100 mA, P_D < P_{DMAX}		0.2	5	µA
V_{REF}	Reference Voltage	3 V < V_I - V_O < 40 V, 10 mA ≤ I_O ≤ 100 mA, P_D ≤ P_{DMAX}	1.20	1.25	1.30	V
ST_T	Temperature Stability			0.7		%
$I_{L(MIN)}$	Minimum Load Current to Maintain Regulation	V_I - V_O = 40 V		3.5	10	mA
$I_{O(MAX)}$	Maximum Output Current	V_I - V_O ≤ 15V, P_D < P_{DMAX}	100	200		mA
		V_I - V_O ≤ 40 V, P_D < P_{DMAX}, T_A = +25°C	25	50		mA
e_N	RMS Noise, %/V_{OUT}	T_A = +25°C, 10 Hz < f < 10 kHz		0.003		%/V_O
RR	Ripple Rejection	V_O = 10 V, f = 120 Hz, without C_{ADJ}		65		dB
		V_O = 10 V, f = 120 Hz, C_{ADJ} = 10 µF	66	80		dB
ST	Long-Term Stability	T_J = +125°C, 1000 Hours		0.3		%

Note:

1. Load and Line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

Typical Application

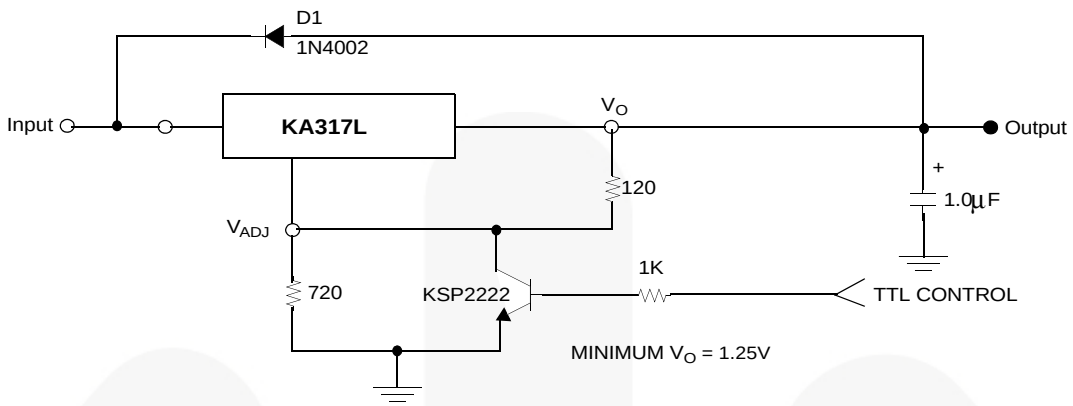


Figure 2. 5V Electronic Shutdown Regulator

D1 protects the device during an input short circuit.

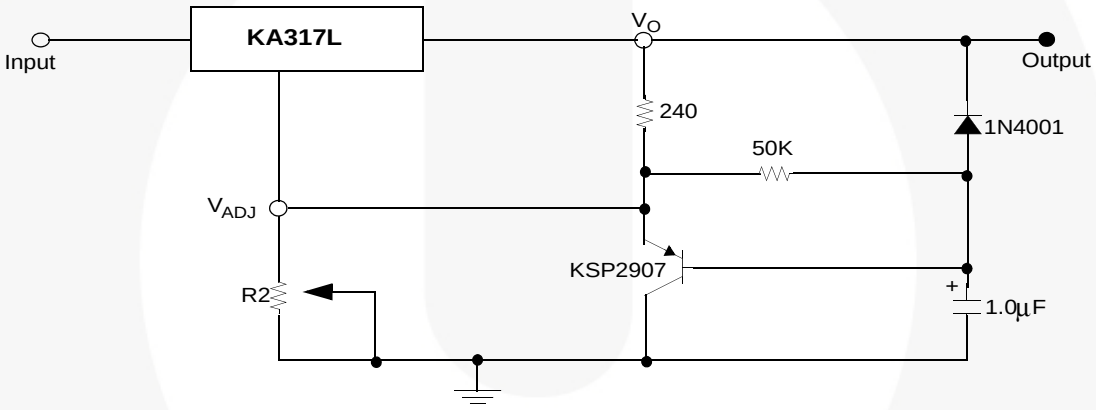


Figure 3. Slow Turn-On Regulator

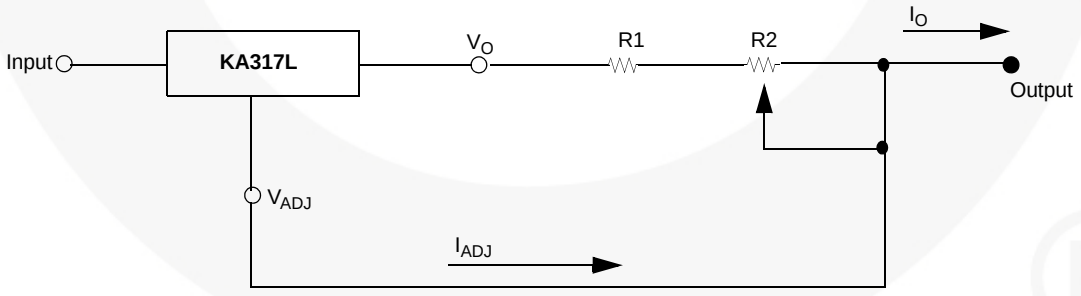


Figure 4. Current Regulator

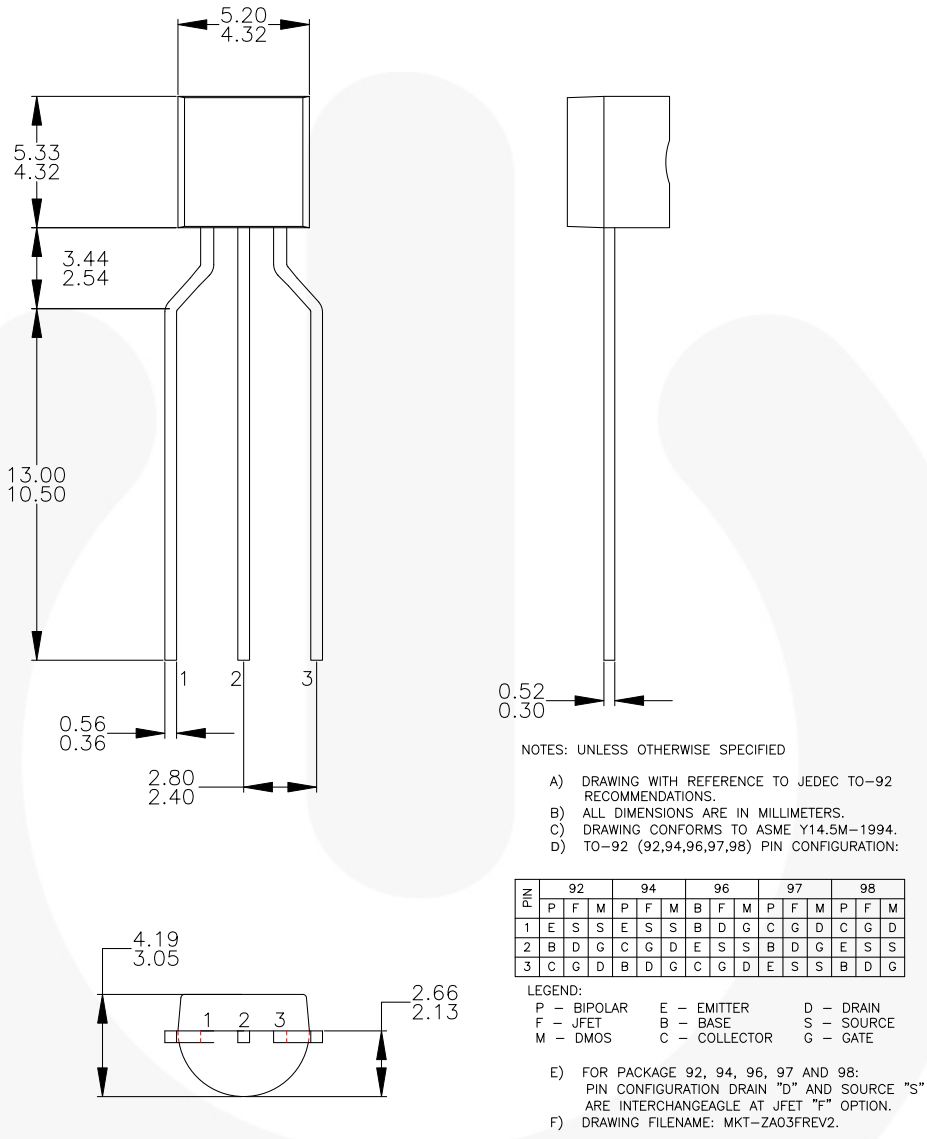
$$I_{OMAX} = \left(\frac{V_{REF}}{R1}\right) + I_{ADJ} @ \frac{1.25V}{R1}$$

$$I_{OMAX} = \left(\frac{V_{REF}}{R1 + R2}\right) + I_{ADJ} @ \frac{1.25V}{R1 + R2}$$

$$5mA < I_O < 500mA$$

Physical Dimensions

TO-92 Ammo Type



NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DRAWING CONFORMS TO ASME Y14.5M-1994.
D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	B	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:
P – BIPOLAR
F – JFET
M – DMOS
E – EMITTER
B – BASE
C – COLLECTOR
D – DRAIN
S – SOURCE
G – GATE

E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEAGLE AT JFET "F" OPTION.
F) DRAWING FILENAME: MKT-ZA03FREV2.

Figure 6. 3-Lead, TO-92, Molded, 0.200 in Line Spacing Lead Form

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