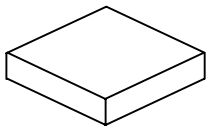
5x10 DUAL BAND ANTENNA SWITCH GaAs MMIC

■GENERAL DESCRIPTION

NJG1540JA3 is a 5x10 antenna switch IC for 800MHz and 1.5GHz dual band digital cellular phone. The 7 bits parallel control signal controls RF paths between 800MHz T/R or 1.5GHz T/R circuits and internal two antennas or external two antennas. The termination ports to improve interference between diversity antennas with external matching circuits are equipped. The ultra small and thin BCC32-A3 package is applied.

■PACKAGE OUTLINE



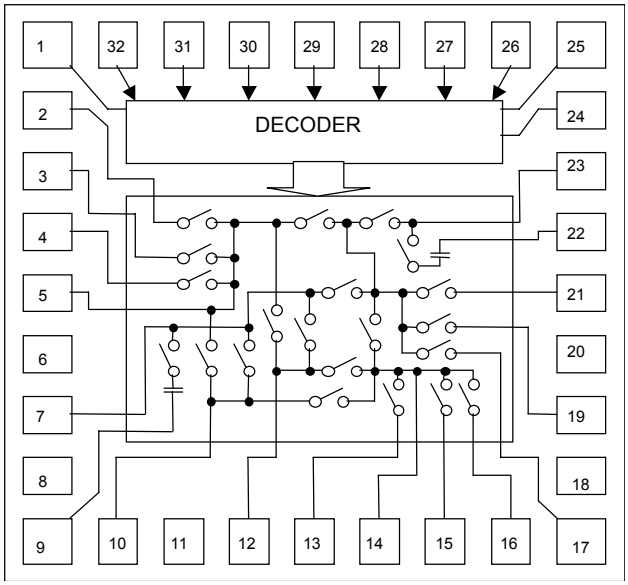
NJG1540JA3

■FEATURES

●Low voltage operation	+3.3V and -2.5V (Tx only)
●Low current consumption	30uA typ. (Transmit, P_{IN}=30dBm)
	15uA typ. (Receiving, No RF signal)
●Low insertion loss	0.35dB typ. @TX1-ANT1,ANT2,EXT1, f_{in}=960MHz, P_{in}=30dBm
	0.55dB typ. @TX2-ANT1,ANT2,EXT1, f_{in}=1453MHz, P_{in}=30dBm
●Ultra small & thin package	BCC32 (Mount Size: 5.0x5.0x0.8mm)

■PIN CONFIGURATION

BCC32 type
(Top View)



Pin Connection

1. VDD	17. RX3(1.5GHz)
2. TERM5(1.5GHz)	18. GND
3. TERM4(800MHz RX)	19. RX2(800MHz A Band)
4. TERM3(800MHz TX)	20. GND
5. ANT2	21. RX1(800MHz D/C Band)
6. GND	22. GND
7. EXT1	23. EXT2
8. GND	24. GND
9. GND	25. VSS
10. TX1(800MHz)	26. CTL7
11. GND	27. CTL6
12. TX2(1.5GHz)	28. CTL5
13. TERM6(800MHz TX)	29. CTL4
14. ANT1	30. CTL3
15. TERM2(1.5GHz)	31. CTL2
16. TERM1(800MHz RX)	32. CTL1

■ABSOLUTE MAXIMUM RATINGS

(T_a=+25°C)

PARAMETER	SYMBOL	CONDTIONS	RATINGS	UNITS
Supply Voltage 1	V_{DD}	VDD Terminal	6.0	V
Supply Voltage 2	V_{SS}	VSS Terminal	-4.0~+0.3	V
Control Voltage	V_{CTL}	CTL1~7 Terminals	6.0	V
Input Power	P_{IN}	TX1, TX2, ANT1, ANT2, EXT1 Terminals	36	dBm
		RX1, RX2, RX3, EXT2 Terminals	28	dBm
Power Dissipation	P_D		950	mW
Operating Temperature	T_{opr}		-25~+75	°C
Storage Temperature	T_{stg}		-55~+125	°C

■ELECTRICAL CHARACTERISTICS 1 [DC CHARACTERISTICS]

General Conditions: T_a=+25°C, V_{DD}=3.3V, V_{SS}=-2.5V
TX1, TX2, RX1, RX2, RX3, ANT1, ANT2, EXT1, EXT2: terminated (50Ω)
TER1~6: grounded by 5pFcapacitor.

PARAMETER	SYMBOL	CONDTIONS	MIN	TYP	MAX	UNITS
Positive Supply Voltage	V_{DD}	V_{DD} Terminal	2.7	3.3	5.0	V
Negative Supply Voltage	V_{SS}	V_{SS} Terminal	-3.5	-2.5	-2.0	V
Current Consumption 1	I_{DD1}	V_{DD} Terminal RX Mode, No RF Signal	-	15	30	uA
Current Consumption 2	I_{SS1}	V_{SS} Terminal RX Mode, No RF Signal	-0.1	-	0	uA
Current Consumption 3	I_{DD2}	V_{DD} Terminal f_{in}=0.05~2GHz TX Mode, P_{in}=30dBm	-	50	100	uA
Current Consumption 4	I_{SS2}	V_{SS} Terminal, f_{in}=0.05~2GHz TX Mode, P_{in}=30dBm	-100	-50	-	uA
Control Voltage (H)	$V_{CTL(H)}$	CTL1~7 Terminal	2.0	3.0	V_{DD}	V
Control Voltage (L)	$V_{CTL(L)}$	CTL1~7 Terminal	0	0	0.6	V
Control Current	I_{CTL}	CTL1~7 Terminal=V_{DD} or CTL1~7 Terminal=0V	-1.3	-	1.3	uA
Control terminal Input Impedance	R_{in}	CTL1~7 Terminal	4	-	-	MΩ

■ELECTRICAL CHARACTRISTICS 2 [800MHz TX Mode]

General Conditions: T_a=+25°C, V_{DD}=3.3V, V_{SS}=0V, f_{in}=893~960MHz
Tested on PCB circuit as shown below.
Insertion loss of each connectors, striplines, and capacitors are excluded.
TX1, TX2, RX1, RX2, RX3, ANT1, ANT2, EXT1, and EXT2: terminated (50Ω)
TER1~6: grounded by 5pF capacitor

PARAMETER	SYMBOL	CONDTIONS	MIN	TYP	MAX	UNITS
TX1-ANT1 Insertion Loss	LOSS1	P_{in}=30dBm	-	0.35	0.50	dB
TX1-ANT2 Insertion Loss	LOSS2	P_{in}=30dBm	-	0.35	0.50	dB
TX1-EXT1 Insertion Loss	LOSS3	P_{in}=30dBm	-	0.35	0.50	dB
TX1-RX1, RX2, RX3 Isolation	ISL1	P_{in}=30dBm TX1-ANT1, ANT2, EXT1 passing	40	45	-	dB
TX1-EXT1 Isolation	ISL2	P_{in}=30dBm TX1-ANT1, ANT2 passing	23	25	-	dB
TX1-ANT1 Isolation	ISL3	P_{in}=30dBm TX1-ANT2, EXT1 passing	25	30	-	dB
TX1-ANT2 Isolation	ISL4	P_{in}=30dBm TX1-ANT1, EXT1 passing	25	30	-	dB
TX1-EXT2 Isolation	ISL5	P_{in}=30dBm TX1-ANT1, ANT2, EXT1 passing	25	30	-	dB
Input Power at 0.1dB Compression 1	$P_{-0.1dB}$(1)	TX1-ANT1, ANT2, EXT1 passing	33.0	34.5	-	dBm
Adjacent Channel Leakage Power 1	ACP1	PDC Standard, ±50kHz offset P_{in}=30dBm, Load: VSWR=1.5 Input Signal ACP=-70dBc @ 30dBm	-	-65	-63	dBc
Adjacent Channel Leakage Power 2	ACP2	PDC Standard, ±50kHz offset, P_{in}=30dBm, Load: VSWR ≦ 3.0 Input Signal ACP=-70dBc @ 30dBm	-	-65	-55	dBc
Adjacent Channel Leakage Power 3	ACP3	PDC Standard, ±50kHz offset, V_{DD} ≧3.0V P_{in}=30dBm, Load: VSWR ≦ 1.5 Input Signal ACP=-70dBc @ 30dBm	-	-65	-60	dBc
Adjacent Channel Leakage Power 4	ACP4	PDC Standard, ±100kHz offset V_{DD} ≧ 3.0V P_{in}=30dBm, Load: VSWR ≦ 1.5 Input Signal ACP=-76dBc @ 30dBm	-	-73	-65	dBc
2nd Harmonics 1	$2f_0$(1)	P_{in}=30dBm V_{DD}≧ 3.0V, Load: VSWR ≦ 1.5 Input Signal 2nd Harmonics=-70dBc	-	-70	-65	dBc
3rd Harmonics 1	$3f_0$(1)	P_{in}=30dBm V_{DD}≧ 3.0V, Load: VSWR ≦1.5 Input Signal 3rd Harmonics=-100dBc	-	-65	-63	dBc
VSWR 1	VSWR1	TX1-ANT1, ANT2, EXT1 passing	-	1.2	1.4	
Switching Time 1	T_D1	CTL1~7	-	200	500	nsec

■ELECTRICAL CHARACTRISTICS 3 [800MHz RX Mode]

General Conditions: T_a=+25°C, V_{DD}=3.3V, V_{SS}=0V, f_{in}=810~885MHz
Tested on PCB circuit as shown below.
Insertion loss of each connectors, striplines, and capacitors are excluded.
TX1, TX2, RX1, RX2, RX3, ANT1, ANT2, EXT1, and EXT2: terminated (50Ω)
TER1~6: grounded by 5pF capacitor

PARAMETER	SYMBOL	CONDTIONS	MIN	TYP	MAX	UNITS
RX1,2-ANT1 Insertion Loss	LOSS4	P_{in}=10dBm	-	0.85	1.00	dB
RX1,2-ANT2 Insertion Loss	LOSS5	P_{in}=10dBm	-	0.85	1.00	dB
RX1,2-EXT1 Insertion Loss	LOSS6	P_{in}=10dBm	-	0.95	1.10	dB
RX1,2-EXT2 Insertion Loss	LOSS7	P_{in}=10dBm	-	1.05	1.20	dB
RX1-RX2 Isolation	ISL6	P_{in}=10dBm , f=658MHz RX1,2-ANT1,2,EXT1,2 passing	23	25	-	dB
RX1,2-ANT1 Isolation	ISL7	P_{in}=10dBm RX1,2-ANT2,EXT1,EXT2 passing	23	25	-	dB
RX1,2-ANT2 Isolation	ISL8	P_{in}=10dBm RX1,2-ANT1,EXT1,EXT2 passing	25	30	-	dB
RX1,2-EXT1 Isolation	ISL9	P_{in}=10dBm RX1,2-ANT1,ANT2,EXT2 passing	23	27	-	dB
RX1,2-EXT2 Isolation	ISL10	P_{in}=10dBm RX1,2-ANT1,ANT2,EXT1 passing	25	30	-	dB
Input Power at 0.5dB Compression 1	$P_{-0.5}$(1)	RX1,2-ANT1,ANT2,EXT1,EXT2 passing	25	28	-	dBm
VSWR 2	VSWR2	RX1,2-ANT1,ANT2,EXT1,EXT2 passing	-	1.3	1.5	
Switching Time2	T_D2	CTL1~7	-	200	500	nsec

■ELECTRICAL CHARACTRISTICS 4 [1.5GHz TX Mode]

General Conditions: T_a=+25°C, V_{DD}=3.3V, V_{SS}=0V, f_{in}=1429~1453MHz
Tested on PCB circuit as shown below.
Insertion loss of each connectors, striplines, and capacitors are excluded.
TX1, TX2, RX1, RX2, RX3, ANT1, ANT2, EXT1, and EXT2: terminated (50Ω)
TER1~6: grounded by 5pF capacitor

PARAMETER	SYMBOL	CONDTIONS	MIN	TYP	MAX	UNITS
TX2-ANT1 Insertion Loss	LOSS8	P_{in}=30dBm	-	0.55	0.70	dB
TX2-ANT2 Insertion Loss	LOSS9	P_{in}=30dBm	-	0.55	0.70	dB
TX2-EXT1 Insertion Loss	LOSS10	P_{in}=30dBm	-	0.55	0.70	dB
TX2-RX1,RX2,RX3 Isolation	ISL11	P_{in}=30dBm TX2-ANT1, ANT2, EXT1 passing	40	45	-	dB
TX2-EXT1 Isolation	ISL12	P_{in}=30dBm TX2-ANT1 ANT2, passing	23	25	-	dB
TX2-ANT1 Isolation	ISL13	P_{in}=30dBm TX2- ANT2, EXT1 passing	23	25	-	dB
TX2-ANT2 Isolation	ISL14	P_{in}=30dBm TX2-ANT1, EXT1 passing	23	25	-	dB
TX2-EXT2 Isolation	ISL15	P_{in}=30dBm TX2-ANT1, ANT2, EXT1 passing	25	30	-	dB
Input Power at 0.1dB Compression. 2	$P_{-0.1}$(2)	TX2-ANT1, ANT2,EXT1 passing	33.0	34.5	-	dBm
Adjacent Channel Leakage Power 5	ACP5	PDC Standard, ±50kHz offset P_{in}=30dBm, Load: VSWR=1.5 Input Signal ACP=-68dBc @ 30dBm	-	-65	-63	dBc
Adjacent Channel Leakage Power 6	ACP6	PDC Standard, ±50kHz offset, P_{in}=30dBm, Load: VSWR ≦ 3.0 Input Signal ACP=-68dBc @ 30dBm	-	-62	-55	dBc
Adjacent Channel Leakage Power 7	ACP7	PDC Standard, ±50kHz offset, V_{DD} ≧3.0V P_{in}=30dBm, Load: VSWR ≦1.5 Input Signal ACP=-68dBc @ 30dBm	-	-65	-60	dBc
Adjacent Channel Leakage Power 8	ACP8	PDC Standard, ±100kHz offset V_{DD} ≧ 3.0V P_{in}=30dBm, Load: VSWR ≦1.5 Input Signal ACP=-76dBc @ 30dBm	-	-70	-65	dBc
2nd Harmonics 2	$2f_0$(2)	P_{in}=30dBm V_{DD}≧ 3.0V, Load: VSWR ≦ 1.5 Input Signal 2nd Harmonics=-80dBc	-	-68	-65	dBc
3nd Harmonics 2	$3f_0$(2)	P_{in}=30dBm V_{DD}≧ 3.0V, Load: VSWR ≦1.5 Input Signal 3rd Harmonics=-100dBc	-	-60	-57	dBc
VSWR3	VSWR3	TX2-ANT1, ANT2,EXT1 passing	-	1.2	1.4	
Switching Time3	T_D3	CTL1~7	-	200	500	nsec

■ELECTRICAL CHARACTRISTICS 5 [1.5GHz RX Mode]

General Conditions: T_a=+25°C, V_{DD}=3.3V, V_{SS}=0V, f_{in}=1477~1501MHz
Tested on PCB circuit as shown below.
Insertion loss of each connectors, striplines, and capacitors are excluded.
TX1, TX2, RX1, RX2, RX3, ANT1, ANT2, EXT1, and EXT2: terminated (50Ω)
TER1~6: grounded by 5pF capacitor

PARAMETER	SYMBOL	CONDTIONS	MIN	TYP	MAX	UNITS
RX3-ANT1 Insertion Loss	LOSS11	P_{in}=10dBm	-	1.00	1.15	dB
RX3-ANT2 Insertion Loss	LOSS12	P_{in}=10dBm	-	1.10	1.25	dB
RX3-EXT1 Insertion Loss	LOSS13	P_{in}=10dBm	-	1.10	1.25	dB
RX3-EXT2 Insertion Loss	LOSS14	P_{in}=10dBm	-	1.00	1.15	dB
RX3-ANT1 Isolation	ISL16	P_{in}=10dBm RX3-ANT2, EXT1, EXT2 passing	25	30	-	dB
RX3-ANT2 Isolation	ISL17	P_{in}=10dBm RX3-ANT1, EXT1, EXT2 passing	23	25	-	dB
RX3-EXT1 Isolation	ISL18	P_{in}=10dBm RX3-ANT1, ANT2, EXT2 passing	25	28	-	dB
RX3-EXT2 Isolation	ISL19	P_{in}=10dBm RX3-ANT1, ANT2, EXT1 passing	25	30	-	dB
Input Power at 0.5dB Compression 2	$P_{-0.5}$(2)	RX3-ANT1, ANT2, EXT1, EXT2 passing	25	28	-	dBm
VSWR 4	VSWR4	RX3-ANT1, ANT2, EXT1, EXT2 passing	-	1.3	1.5	dBc
Switching Time 4	T_D4	CTL1~7	-	200	500	dBc

■ELECTRICAL CHARACTERISTICS 6 [1.5GHz TX,RX Mode]

General Conditions: T_a=+25°C, V_{DD}=3.3V, V_{SS}=0V, f_{in}(TX)=940~960MHz, , f_{in}(RX)=810~830MHz
Tested on PCB circuit as shown below.
Insertion loss of each connectors, striplines, and capacitors are excluded.
TX1, TX2, RX1, RX2, RX3, ANT1, ANT2, EXT1, and EXT2: terminated (50Ω)
TER1~6: grounded by 5pF capacitor

Condition 1: RX1 Open
Condition 2: TX1 Open

PARAMETER	SYMBOL	CONDTIONS	MIN	TYP	MAX	UNITS
TX1-ANT1 Insertion Loss	LOSS15	Pin=30dBm TX1-RX1-ANT1 passing, Condition 1	-	0.90	1.05	dB
	LOSS16	Pin=30dBm TX1-ANT1, RX1-ANT2 passing, Condition 1	-	0.40	0.55	dB
TX1-ANT2 Insertion Loss	LOSS17	Pin=30dBm TX1-ANT2, RX1-ANT1 passing, Condition 1	-	0.40	0.55	dB
	LOSS18	Pin=30dBm TX1-RX1-ANT2 passing, Condition 1	-	0.95	1.10	dB
TX1-EXT1 Insertion Loss	LOSS19	Pin=30dBm TX1-RX1-EXT1 passing, Condition 1	-	1.00	1.15	dB
	LOSS20	Pin=30dBm TX1-EXT1,RX1-EXT2 passing, Condition 1	-	0.40	0.55	dB
RX1-ANT1 Insertion Loss	LOSS21	Pin=10dBm TX1-RX1-ANT1 passing, Condition 2	-	1.05	1.20	dB
	LOSS22	Pin=10dBm TX1-ANT2, RX1-ANT1 passing, Condition 2	-	0.90	1.05	dB
RX1-ANT2 Insertion Loss	LOSS23	Pin=10dBm TX1-ANT1, RX1-ANT2 passing, Condition 2	-	0.95	1.10	dB
	LOSS24	Pin=10dBm TX1-RX1-ANT2 passing, Condition 2	-	1.10	1.25	dB
RX1-EXT1 Insertion Loss	LOSS25	Pin=10dBm TX1-RX1-EXT1 passing, Condition 2	-	1.10	1.25	dB
RX1-EXT2 Insertion Loss	LOSS26	Pin=10dBm TX1-EXT1, RX1-EXT2 passing, Condition 2	-	1.15	1.30	dB
TX1-RX1 Isolation	ISL20	Pin=30dBm TX1- ANT1, RX1-ANT2 passing	23	28	-	dB
	ISL21	Pin=30dBm TX1- EXT1, RX1-EXT2 passing	30	35	-	dB
	ISL22	Pin=30dBm TX1- ANT2, RX1-ANT1 passing	23	28	-	dB
TX1-RX2 Isolation	ISL23	Pin=30dBm TX1-RX1-ANT1 passing, Condition 1	25	29	-	dB
	ISL24	Pin=30dBm TX1-ANT1, RX1-ANT2 passing, Condition 1	45	50	-	dB
	ISL25	Pin=30dBm TX1-RX1-EXT1 passing, Condition 1	25	30	-	dB
	ISL26	Pin=30dBm TX1-EXT1, RX1-EXT2 passing, Condition 1	45	50	-	dB
	ISL27	Pin=30dBm TX1-ANT1, RX1-ANT1 passing, Condition 1	45	50	-	dB
	ISL28	Pin=30dBm TX1-RX1-ANT2 passing, Condition 1	25	30	-	dB

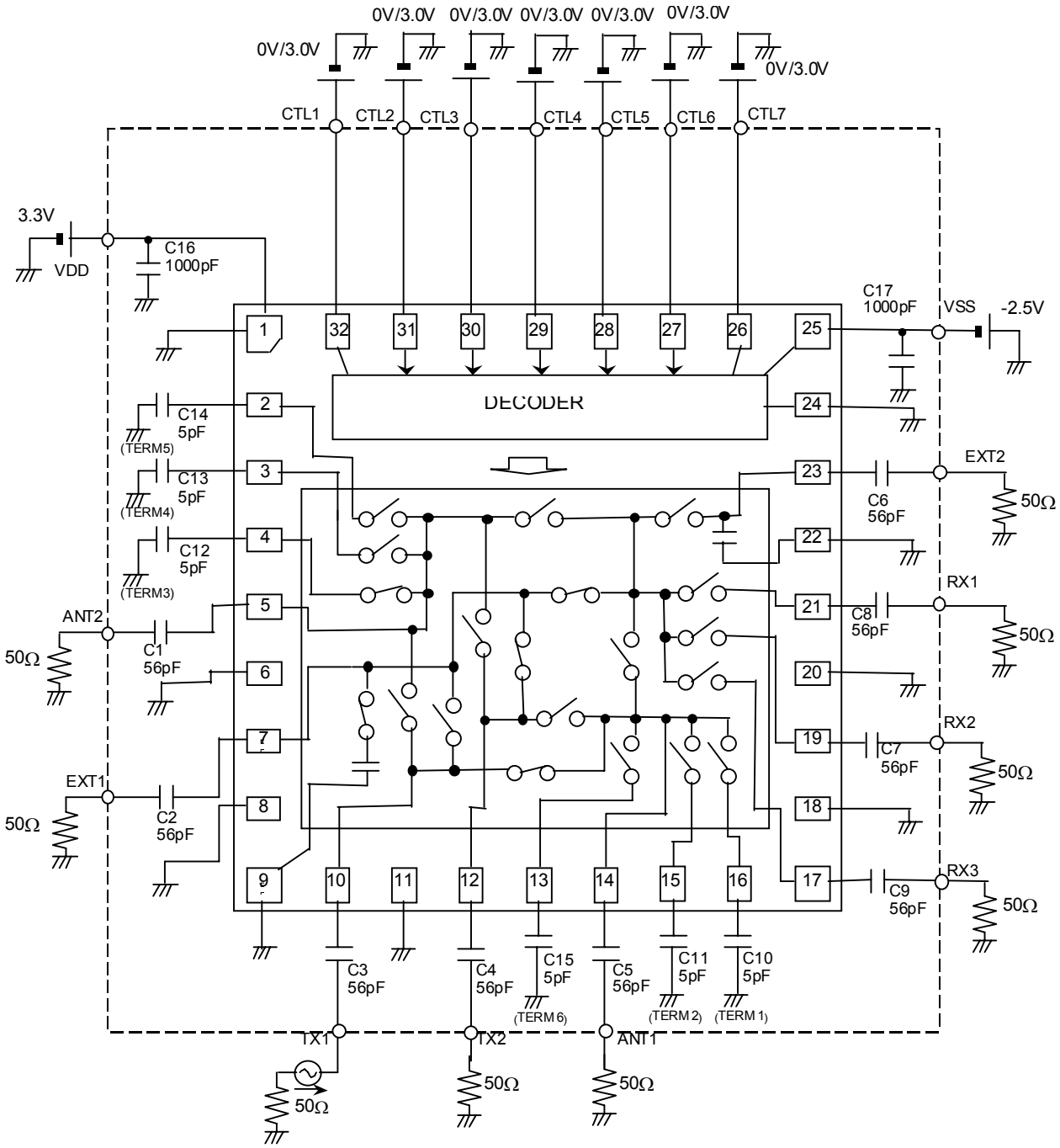
TX1-ANT1 Isolation	ISL29	Pin=30dBm TX1-RX1-EXT1 passing, Condition 1	25	30	-	dB
	ISL30	Pin=30dBm TX1-EXT1,RX1-EXT2 passing, Condition 1	25	30	-	dB
	ISL31	Pin=30dBm TX1-ANT2,RX1-ANT1 passing, Condition 1	17	20	-	dB
	ISL32	Pin=30dBm TX1-RX1-ANT2 passing, Condition 1	17	20	-	dB
TX1-ANT2 Isolation	ISL33	Pin=30dBm TX1-RX1-ANT1 passing, Condition 1	17	20	-	dB
	ISL34	Pin=30dBm TX1-ANT1,RX1-ANT2 passing, Condition 1	17	20	-	dB
	ISL35	Pin=30dBm TX1-RX1-EXT1 passing, Condition 1	28	33	-	dB
	ISL36	Pin=30dBm TX1-EXT1,RX1-EXT2 passing, Condition 1	28	33	-	dB
TX1-EXT1 Isolation	ISL37	Pin=30dBm TX-RX1-ANT1 passing, Condition 1	23	25	-	dB
	ISL38	Pin=30dBm TX1-ANT1,RX1-ANT2 passing, Condition 1	23	27	-	dB
	ISL39	Pin=30dBm TX1-ANT1,RX1-ANT2 passing, Condition 1	25	30	-	dB
	ISL40	Pin=30dBm TX1-RX1-ANT2 passing, Condition 1	23	28	-	dB
TX1-EXT2 Isolation	ISL41	Pin=30dBm TX1-RX1-ANT1 passing, Condition 1	28	33	-	dB
	ISL42	Pin=30dBm TX1-ANT1,RX1-ANT2 passing, Condition 1	50	55	-	dB
	ISL43	Pin=30dBm TX1-RX1-EXT1 passing, Condition 1	28	33	-	dB
	ISL44	Pin=30dBm TX1-EXT1,RX1-EXT2 passing, Condition 1	25	30	-	dB
	ISL45	Pin=30dBm TX1-ANT2,RX1-ANT1 passing, Condition 1	45	50	-	dB
	ISL46	Pin=30dBm TX1-RX1-ANT2 passing, Condition 1	25	32	-	dB
RX1-ANT1 Isolation	ISL47	Pin=10dBm TX1-ANT1,RX1-ANT2 passing, Condition 2	17	21	-	dB
	ISL48	Pin=10dBm TX1-RX1-EXT1 passing, Condition 2	23	27	-	dB
	ISL49	Pin=10dBm TX1-EXT1,RX1-EXT2 passing, Condition 2	30	37	-	dB
	ISL50	Pin=10dBm TX1-RX1-ANT2 passing, Condition 2	17	20	-	dB

RX1-ANT2 Isolation	ISL51	Pin=10dBm TX1-RX1-ANT1 passing, Condition 2	17	20	-	dB
	ISL52	Pin=10dBm TX1-RX1-EXT1 passing, Condition 2	25	30	-	dB
	ISL53	Pin=10dBm TX1-EXT1,RX1-EXT2 passing, Condition 2	30	36	-	dB
	ISL54	Pin=10dBm TX1-ANT2,RX1-ANT1 passing, Condition 2	17	21	-	dB
RX1-EXT1 Isolation	ISL55	Pin=10dBm TX1-RX1-ANT1 passing, Condition 2	23	26	-	dB
	ISL56	Pin=10dBm TX1-ANT1,RX1-ANT2 passing, Condition 2	30	35	-	dB
	ISL57	Pin=10dBm TX1-EXT1,RX1-EXT2 passing, Condition 2	25	30	-	dB
	ISL58	Pin=10dBm TX1-ANT2,RX1-ANT1 passing, Condition 2	23	28	-	dB
	ISL59	Pin=10dBm TX1-RX1-ANT2 passing, Condition 2	28	33	-	dB
RX1-EXT2 Isolation	ISL60	Pin=10dBm TX1-RX1-ANT1 passing, Condition 2	25	30	-	dB
	ISL61	Pin=10dBm TX1-ANT1,RX1-ANT2 passing, Condition 2	25	30	-	dB
	ISL62	Pin=10dBm TX1-RX1-EXT1 passing, Condition 2	25	30	-	dB
	ISL63	Pin=10dBm TX1-ANT2,RX1-ANT1 passing, Condition 2	25	30	-	dB
	ISL64	Pin=10dBm TX1-RX1-ANT2 passing, Condition 2	25	30	-	dB
Adjacent Channel Leakage Power 9	ACP9	PDC Standard, ±50kHz offset P_{in}=30dBm, Load: VSWR=1.5 Input Signal ACP=-64dBc @ 30dBm	-	-65	-63	dBc
Adjacent Channel Leakage Power 10	ACP10	PDC Standard, ±50kHz offset, P_{in}=30dBm, Load: VSWR ≦ 3.0 Input Signal ACP=-64dBc @ 30dBm	-	-65	-60	dBc
Adjacent Channel Leakage Power 11	ACP11	PDC Standard, ±50kHz offset, V_{DD} ≧ 3.0V P_{in}=30dBm, Load: VSWR ≦1.5 Input Signal ACP=-64dBc @ 30dBm	-	-65	-60	dBc
Adjacent Channel Leakage Power 12	ACP12	PDC Standard, ±100kHz offset V_{DD} ≧ 3.0V P_{in}=30dBm, Load: VSWR ≦1.5 Input Signal ACP=-76dBc @ 30dBm	-	-73	-65	dBc
2nd Harmonics 3	2fo(3)	P_{in}=30dBm V_{DD}≧ 3.0V, Load: VSWR ≦ 1.5 Input Signal 2nd Harmonics=-70dBc	-	-68	-65	dBc
3rd Harmonics 3	3fo(3)	P_{in}=30dBm V_{DD}≧ 3.0V, Load: VSWR ≦1.5 Input Signal 3rd Harmonics=-100dBc	-	-60	-57	dBc

■TERMINAL INFORMATION

PIN No.	SYMBOL	DESCRIPTION
1	VDD	Positive voltage supply terminal. The positive voltage (+2.7~+5.0V) have to be supplied. Please connect a bypass capacitor with GND terminal for excellent RF performance.
2	TERM5	ANT2 termination port (1.5GHz band). Please connect this port and GND by appropriate capacitor to suppress the interference of ANT2 port signal to ANT1 port. The capacitor works as DC voltage (V_{DD}) blocking.
3	TERM4	ANT2 termination port (800MHz RX Mode). Please connect this port and GND by appropriate capacitor to suppress the interference of ANT2 port signal to ANT1 port. The capacitor works as DC voltage (V_{DD}) blocking.
4	TERM3	ANT2 termination port (800MHz TX Mode). Please connect this port and GND by appropriate capacitor to suppress the interference of ANT2 port signal to ANT1 port. The capacitor works as DC voltage (V_{DD}) blocking.
5	ANT2	RF transmitting/receiving port. An external capacitor is required to block DC voltage (VDD).
7	EXT1	RF transmitting/receiving port. An external capacitor is required to block DC voltage (VDD).
10	TX1	RF transmitting port (800MHz band). An external capacitor is required to block DC voltage (V_{DD}).
12	TX2	RF transmitting port (1.5GHz band). An external capacitor is required to block DC voltage (V_{DD}).
13	TERM6	ANT1 termination port (800MHz TX Mode). Please connect this port and GND by appropriate capacitor to suppress the interference of ANT1 port signal to ANT2 port. The capacitor works as DC voltage (V_{DD}) blocking.
14	ANT1	RF transmitting/receiving port. An external capacitor is required to block DC voltage (V_{DD}).
15	TERM2	ANT1 termination port (1.5GHz band). Please connect this port and GND by appropriate capacitor to suppress the interference of ANT1 port signal to ANT2 port. The capacitor works as DC voltage (V_{DD}) blocking.
16	TERM1	ANT1 termination port (800MHz TX Mode). Please connect this port and GND by appropriate capacitor to suppress the interference of ANT1 port signal to ANT2 port. The capacitor works as DC voltage (V_{DD}) blocking.
17	RX3	RF transmitting port (1.5GHz band). An external capacitor is required to block DC voltage (V_{DD}).
19	RX2	RF transmitting port (800MHz A band). An external capacitor is required to block DC voltage (V_{DD}).
21	RX3	RF transmitting port (800MHz D/C band). An external capacitor is required to block DC voltage (V_{DD}).
23	EXT2	RF receiving port. An external capacitor of is required to block DC voltage (V_{DD}).
25	VSS	Negative voltage supply terminal. Please supply negative voltage of -3.5~-2.0V on transmitting state. On receiving state, this terminal is internally disconnected, so the voltage of this terminal (negative, short, or open) does not affect to receiving signal quality. The bypass capacitor should be connected between this terminal and GND for excellent RF performance.
26	CTL7	High-impedance C-MOS input terminal. This terminal is set to High-Level (+2V~V_{DD}) or Low-Level (+0.6V~0V). If the voltage level of this terminal is unstable, please connect a resistor (100kΩ) with GND terminal or V_{DD} terminal.
27	CTL6	High-impedance C-MOS input terminal. This terminal is set to High-Level (+2V~V_{DD}) or Low-Level (+0.6V~0V). If the voltage level of this terminal is unstable, please connect a resistor (100kΩ) with GND terminal or V_{DD} terminal.
28	CT5	High-impedance C-MOS input terminal. This terminal is set to High-Level (+2V~V_{DD}) or Low-Level (+0.6V~0V). If the voltage level of this terminal is unstable, please connect a resistor (100kΩ) with GND terminal or V_{DD} terminal.
29	CTL4	High-impedance C-MOS input terminal. This terminal is set to High-Level (+2V~V_{DD}) or Low-Level (+0.6V~0V). If the voltage level of this terminal is unstable, please connect a resistor (100kΩ) with GND terminal or V_{DD} terminal.
30	CTL3	High-impedance C-MOS input terminal. This terminal is set to High-Level (+2V~V_{DD}) or Low-Level (+0.6V~0V). If the voltage level of this terminal is unstable, please connect a resistor (100kΩ) with GND terminal or V_{DD} terminal.
31	CTL2	High-impedance C-MOS input terminal. This terminal is set to High-Level (+2V~V_{DD}) or Low-Level (+0.6V~0V). If the voltage level of this terminal is unstable, please connect a resistor (100kΩ) with GND terminal or V_{DD} terminal.
32	CTL1	High-impedance C-MOS input terminal. This terminal is set to High-Level (+2V~V_{DD}) or Low-Level (+0.6V~0V). If the voltage level of this terminal is unstable, please connect a resistor (100kΩ) with GND terminal or V_{DD} terminal.
6,8,9,11 18,20,22,24	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.

■APPLICATION CIRCUIT

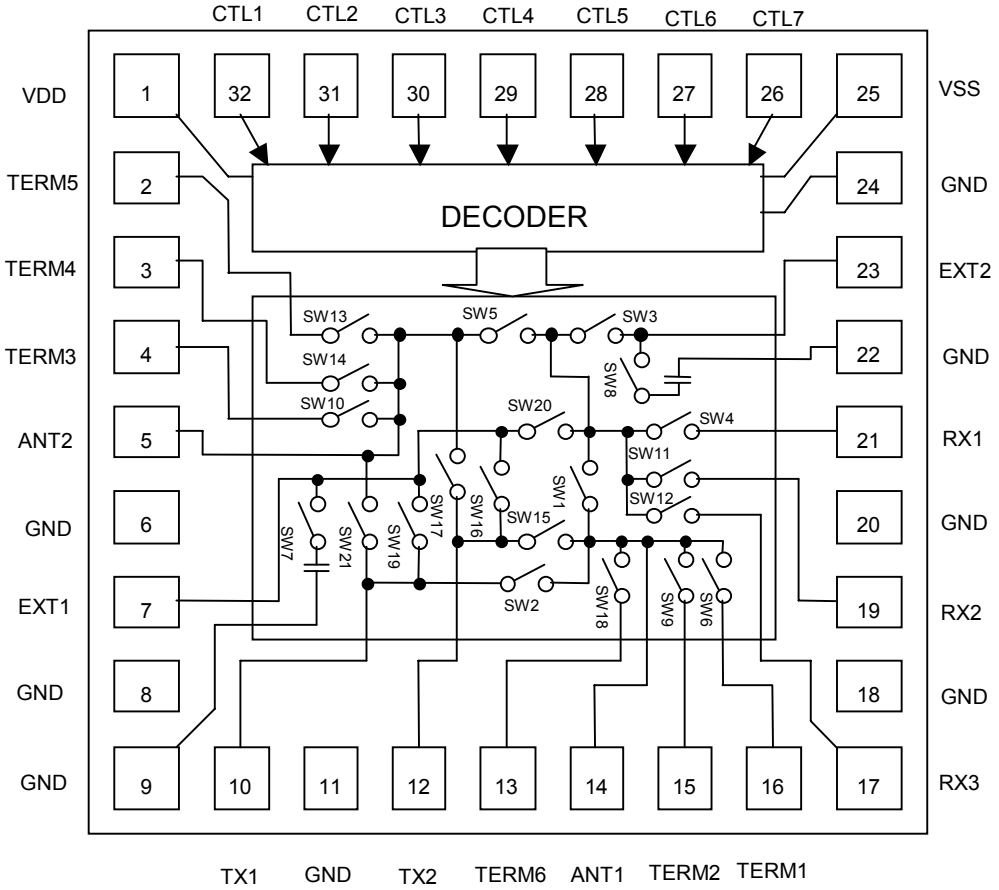


■TRUTH TABLE

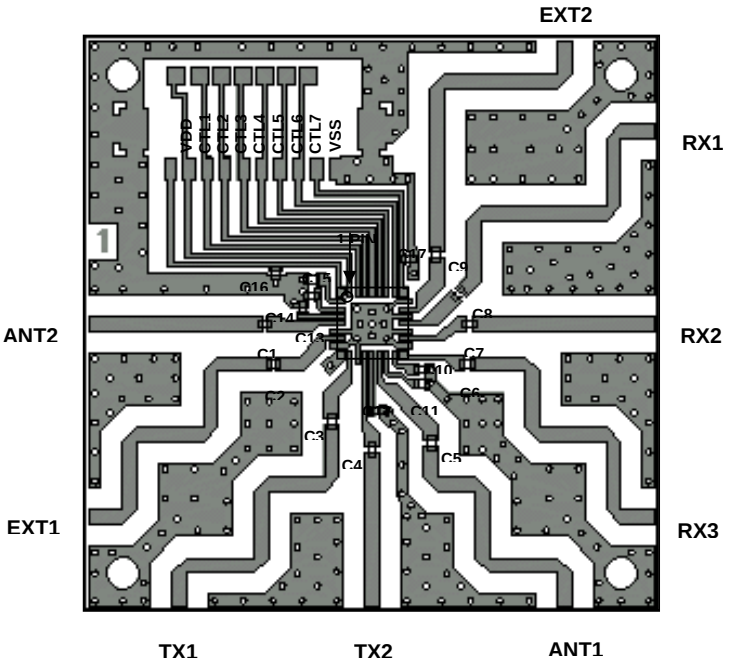
"H"=$V_{CTL\ (H)}$, "L"=$V_{CTL\ (L)}$, "X"=H or L

No.	ROUTE	CONTOROL INPUT							CONTOROL OUTPUT																	
		CTL1	CTL2	CTL3	CTL4	CTL5	CTL6	CTL7	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	SW10	SW11	SW12	SW13	SW14	SW15	SW16	SW17	SW18	SW19	SW20	SW21
1	TX1-ANT1	H	X	H	X	L	L	L	OFF	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF
2	TX1-EXT1	H	X	L	X	L	X	L	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	OFF
3	RX1-ANT1	L	L	H	L	L	X	X	ON	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	OFF
4	RX1-ANT2	L	H	H	L	L	X	X	OFF	OFF	OFF	ON	ON	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF
5	RX1-EXT1	L	L	L	L	L	X	X	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF
6	RX1-EXT2	L	H	L	L	L	X	X	OFF	OFF	ON	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
7	RX2-ANT1	L	L	H	H	L	X	X	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	OFF
8	RX2-ANT2	L	H	H	H	L	X	X	OFF	OFF	OFF	OFF	ON	ON	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF
9	RX2-EXT1	L	L	L	H	L	X	X	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF
10	RX2-EXT2	L	H	L	H	L	X	X	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
11	TX2-ANT1	H	X	H	X	H	L	L	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	ON	OFF
12	TX2-EXT1	H	X	L	X	H	X	L	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
13	RX3-ANT1	L	L	H	X	H	X	X	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF
14	RX3-ANT2	L	H	H	X	H	X	X	OFF	OFF	OFF	OFF	ON	OFF	ON	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF
15	RX3-EXT1	L	L	L	X	H	X	X	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF
16	RX3-EXT2	L	H	L	X	H	X	X	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
17	TX1-ANT2	H	X	H	X	L	H	L	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON
18	TX2-ANT2	H	X	H	X	H	H	L	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF
19	TX1-RX1-ANT1	H	L	H	L	L	L	H	ON	ON	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
20	TX1-ANT1, RX1-ANT2	H	H	H	L	L	L	H	OFF	ON	OFF	ON	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
21	TX1-RX1-EXT1	H	L	L	L	L	L	H	OFF	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	OFF
22	TX1-EXT1, RX1-EXT2	H	H	L	L	L	L	H	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	OFF
23	TX1-ANT2, RX1-ANT1	H	L	H	L	L	H	H	ON	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON
24	TX1-RX1-ANT2	H	H	H	L	L	H	H	OFF	OFF	OFF	ON	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON

■PIN CONFIGRATION (TOP VIEW)



■RECOMMENDED PCB DESIGN



PCB: FR-4, t=0.5mm
Strip line width=1.0mm

Board total Loss (Capacitor, Connector, and PCB)

Pass route	Loss(dB)	Frequency
TX1-ANT1	0.33	800MHz Band
TX1-ANT2	0.28	
TX1-EXT1	0.33	
RX1-ANT1	0.31	
RX1-ANT2	0.28	
RX1-EXT1	0.31	
RX1-EXT2	0.31	
RX2-ANT1	0.28	
RX2-ANT2	0.23	
RX2-EXT1	0.28	
RX2-EXT2	0.28	
TX2-ANT1	0.36	1.5GHz Band
TX2-ANT2	0.29	
TX2-EXT1	0.36	
RX3-ANT1	0.46	
RX3-ANT2	0.37	
RX3-EXT1	0.46	
RX3-EXT2	0.46	

Parts List

Parts number	Value	Comment
C1 – C9	56pF	MURATA(GRM36)
C10 – C15	5pF	
C16, C17	1000pF	

PRECAUTIONS

[1] The bypass capacitors should be connected to the VDD, VSS terminals as close as possible respectively.

[2] For good RF performance, the ground terminals should be directly connected to the ground patterns and through-holes as close as possible by using relativity wide pattern.