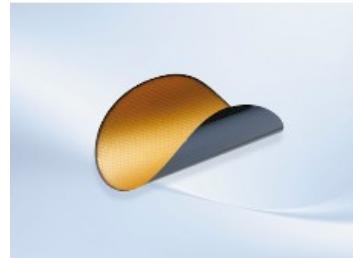


## MOSFET

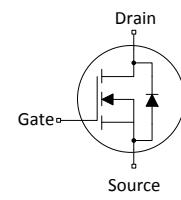
### OptiMOS™3 Power MOS Transistor Chip

- N-channel enhancement mode
- For dynamic characterization refer to the datasheet of IPB011N04N G
- AQL 0.65 for visual inspection according to failure catalogue
- Electrostatic Discharge Sensitive Device according to MIL-STD 883C
- Die bond: soldered or glued
- Backside metallization: NiV system
- Frontside metallization: AlCu system
- Passivation: Nitride + Imide

Power MOS Transistor Chip

**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{(BR)DSS}$	40	V
$R_{DS(on)}$	1.1 <sup>1)</sup>	$\text{m}\Omega$
Die size	5.9 x 3.7	$\text{mm}^2$
Thickness	175	$\mu\text{m}$



Type / Ordering Code	Package	Marking	Related Links
IPC218N04N3	Chip	not defined	-

### 1 Electrical Characteristics on Wafer Level

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(\text{th})}$	2	-	4	V	$V_{DS}=V_{GS}$ , $I_D=200\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1	2	$\mu\text{A}$	$V_{GS}=0\text{ V}$ , $V_{DS}=40\text{ V}$
Gate-source leakage current	$I_{GSS}$	-	2	200	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on- resistance	$R_{DS(\text{on})}$	-	0.9 <sup>2)</sup>	50 <sup>3)</sup>	$\text{m}\Omega$	$V_{GS}=10\text{ V}$ , $I_D=2.0\text{ A}$
Reverse diode forward on-voltage	$V_{SD}$	-	0.86	1.1	V	$V_{GS}=0\text{ V}$ , $I_F=1\text{ A}$
Internal gate resistance	$R_G$	-	1.5	-	$\Omega$	-
Avalanche energy, single pulse	$E_{AS}$	-	-	525 <sup>4)</sup>	mJ	$I_D = 50\text{ A}$ , $R_{GS} = 25\text{ }\Omega$

<sup>1)</sup> packaged in a PG-T0263-7 (see ref. product)

<sup>2)</sup> typical bare die  $R_{DS(\text{on})}$ ;  $V_{GS}=10\text{ V}$  when used with 4\*500 $\mu\text{m}$  Al-wedge double-stitch bonding

<sup>3)</sup> limited by wafer test-equipment

<sup>4)</sup> Wafer tested. For general avalanche capability refer to the datasheet of IPB011N04N G

## 2 Package Outlines

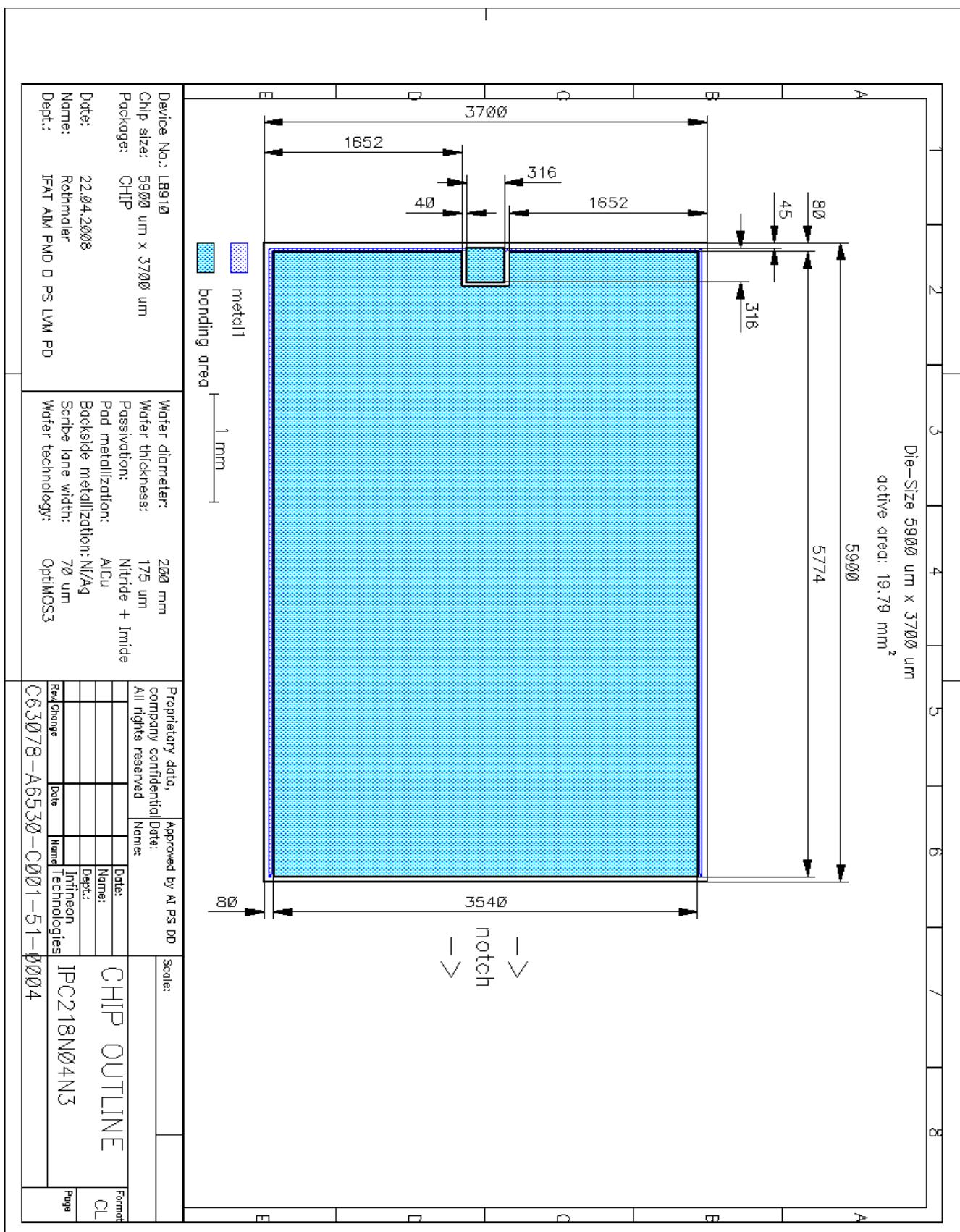


Figure 1 Outline Chip, dimensions in μm

## Revision History

IPC218N04N3

**Revision: 2017-07-17, Rev. 2.6**

### Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.5	2014-07-25	Release Final Version
2.6	2017-07-17	Change typical RDS(on)

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