

July 1996

Features

- 50A, 60V
- $r_{DS(ON)} = 0.022\Omega$
- 2kV ESD Protected
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

Description

The RFG50N06LE, RFP50N06LE, RF1S50N06LE, and RF1S50N06LESM are N-channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

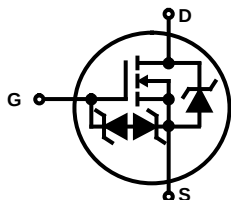
PACKAGE AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RFG50N06LE	TO-247	FG50N06L
RFP50N06LE	TO-220AB	FP50N06L
RF1S50N06LE	TO-262AA	F50N06LE
RF1S50N06LESM	TO-263AB	F50N06LE

Note: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in tape and reel, i.e. RF1S50N06LESM9A.

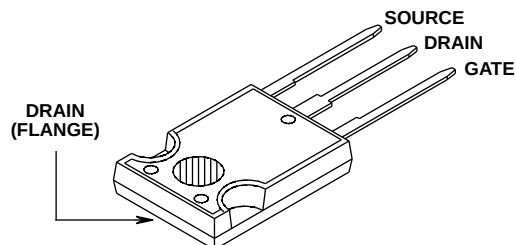
Formerly developmental type TA49164.

Symbol

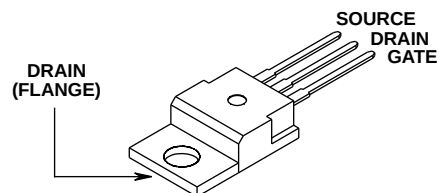


Packages

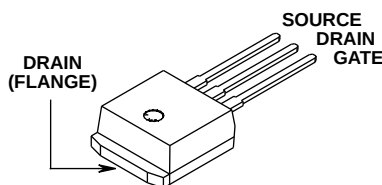
JEDEC STYLE TO-247



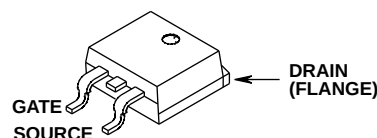
JEDEC TO-220AB



JEDEC TO-262AA



JEDEC TO-263AB



Absolute Maximum Ratings $T_C = +25^\circ\text{C}$

Drain-Source Voltage	V_{DS}
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}
Gate-Source Voltage (Note)	V_{GS}
Drain Current	
Continuous	I_D
Pulsed Drain Current	I_{DM}
Pulsed Avalanche Rating	E_{AS}
Power Dissipation	
$T_C = +25^\circ\text{C}$	P_D
Derate above $+25^\circ\text{C}$	
Operating and Storage Temperature	T_{STG}, T_J
Soldering Temperature of Leads for 10s	T_L
Electrostatic Discharge Rating MIL-STD-883, Category B(2)	ESD

RFG50N06LE, RFP50N06LE, RF1S50N06LE, RF1S50N06LESM	UNITS
60	V
60	V
± 10	V
50	A
Refer to Peak Current Curve Refer to UIS Curve	
142	W
0.95	W/ $^\circ\text{C}$
-55 to +175	$^\circ\text{C}$
260	$^\circ\text{C}$
2	kV

Specifications RFG50N06LE, RFP50N06LE, RF1S50N06LE, RF1S50N06LESM

Electrical Specifications $T_C = +25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A, V_{GS} = 0V$		60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60V, V_{GS} = 0V$	$T_C = +25^{\circ}C$	-	-	1	μA
			$T_C = +150^{\circ}C$	-	-	50	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 10V$		-	-	10	μA
On Resistance	$r_{DS(ON)}$	$I_D = 50A, V_{GS} = 5V$		-	-	0.022	Ω
Turn-On Time	t_{ON}	$V_{DD} = 30V, I_D = 50A, R_L = 0.6\Omega, V_{GS} = 5V, R_{GS} = 2.5\Omega$		-	-	230	ns
Turn-On Delay Time	$t_{D(ON)}$			-	20	-	ns
Rise Time	t_R			-	170	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	48	-	ns
Fall Time	t_F			-	90	-	ns
Turn-Off Time	t_{OFF}			-	-	165	ns
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 0V$ to $10V$	$V_{DD} = 48V, I_D = 50A, R_L = 0.96\Omega$	-	96	120	nC
Gate Charge at 5V	$Q_{G(5)}$	$V_{GS} = 0V$ to $5V$		-	57	70	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0V$ to $1V$		-	2.2	2.7	nC
Input Capacitance	C_{ISS}	$V_{DS} = 25V, V_{GS} = 0V, f = 1MHz$		-	2100	-	pF
Output Capacitance	C_{OSS}			-	600	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	230	-	pF
Thermal Resistance Junction-to-Case	$R_{\theta JC}$			-	-	1.05	$^{\circ}C/W$
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	TO-247		-	-	30	$^{\circ}C/W$
		TO-220, TO-262, and TO-263		-	-	80	$^{\circ}C/W$

Source-Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = 50\text{A}$	-	-	1.5	V
Reverse Recovery Time	t_{RR}	$I_{SD} = 50\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	130	ns

Typical Performance Curves

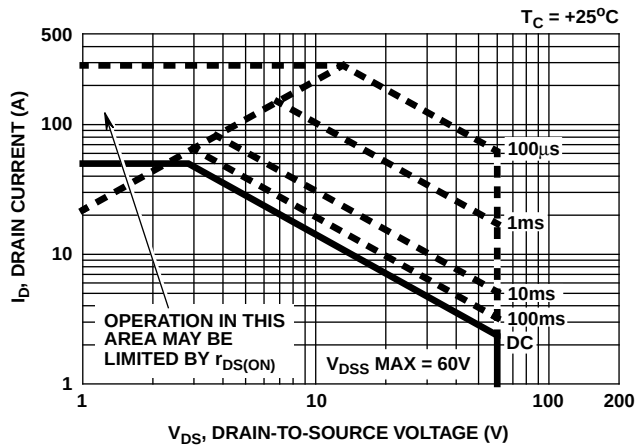


FIGURE 1. SAFE OPERATING AREA CURVE

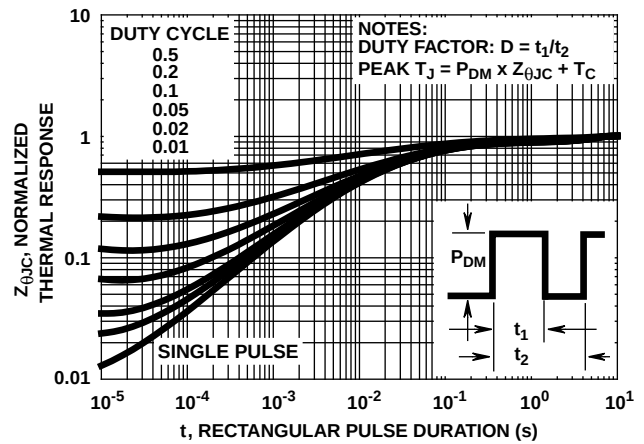


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

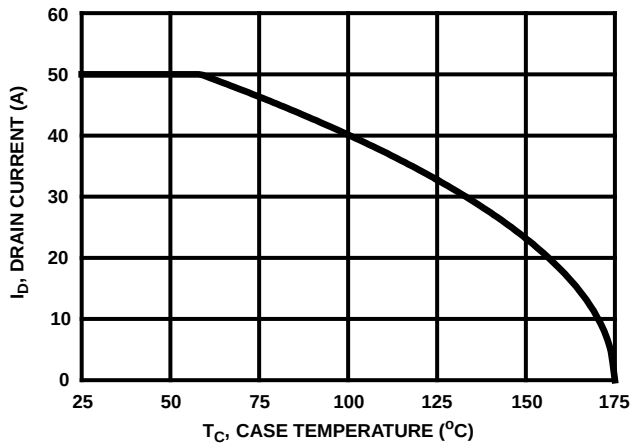


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

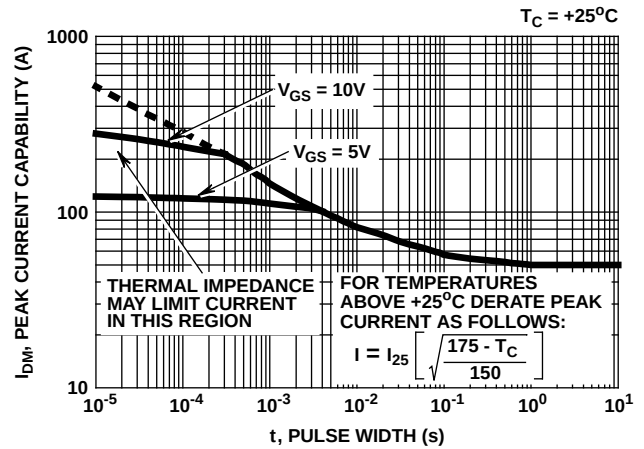


FIGURE 4. PEAK CURRENT CAPABILITY

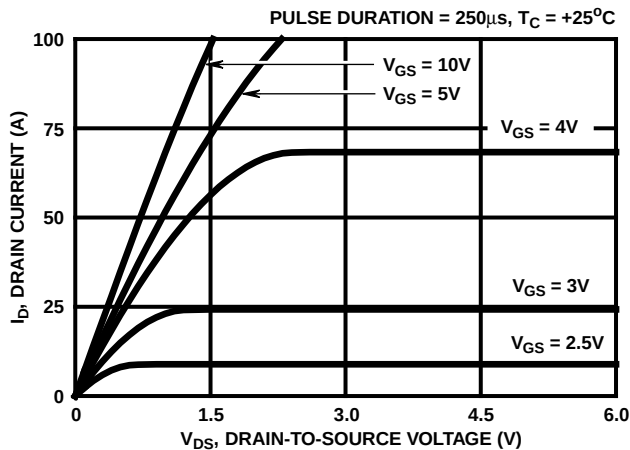


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

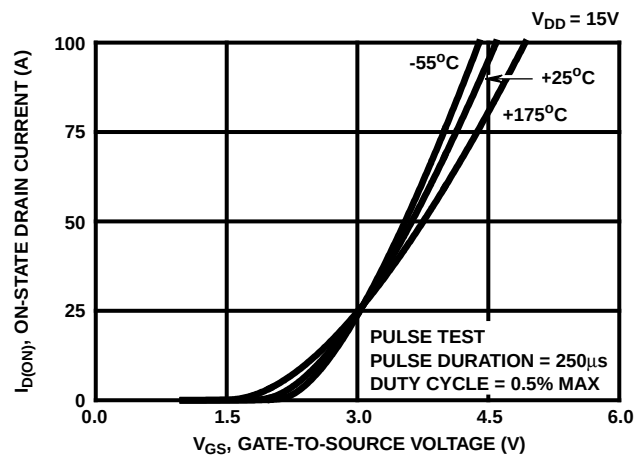


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

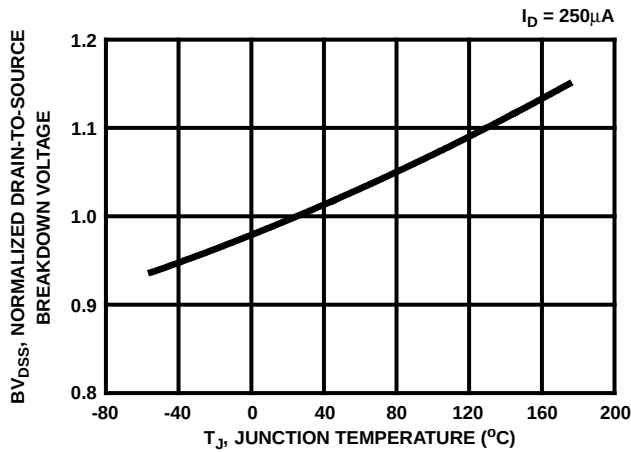


FIGURE 7. NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

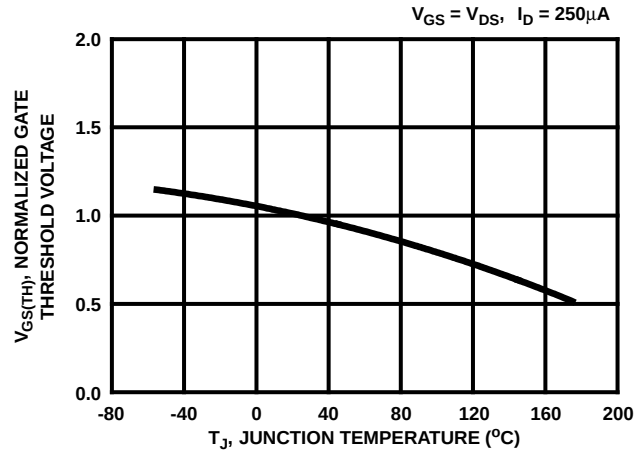


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

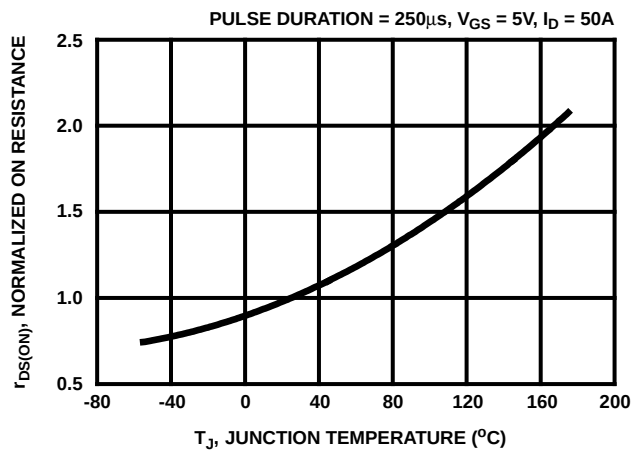


FIGURE 9. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

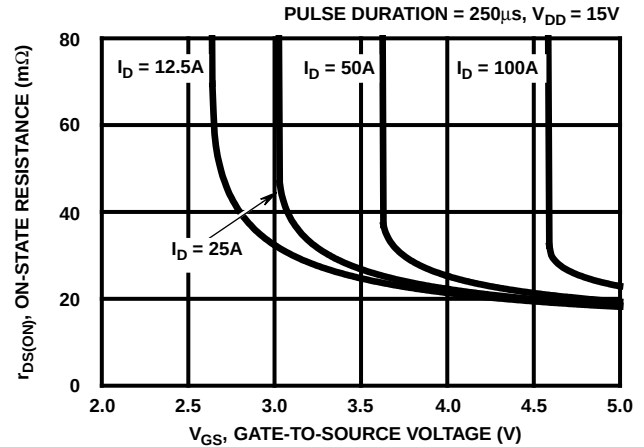


FIGURE 10. $r_{DS(ON)}$ FOR VARYING CONDITIONS OF GATE VOLTAGE AND DRAIN CURRENT

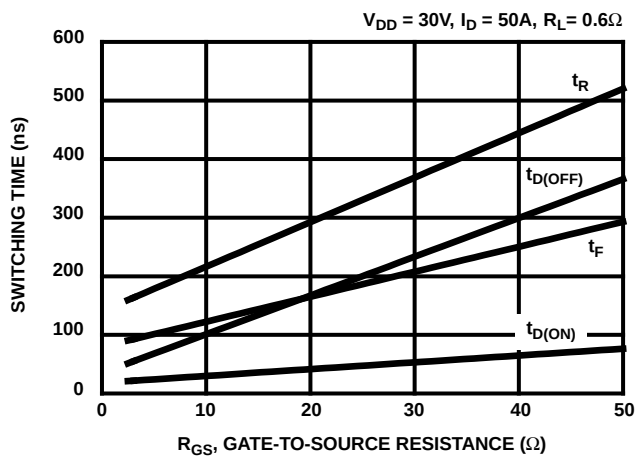


FIGURE 11. SWITCHING TIME AS A FUNCTION OF GATE RESISTANCE

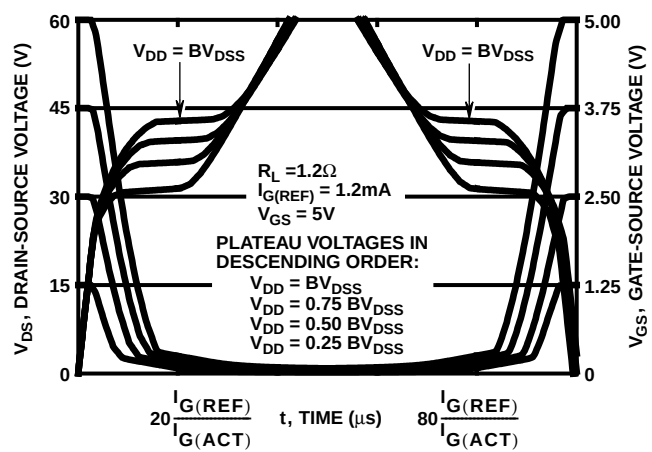


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

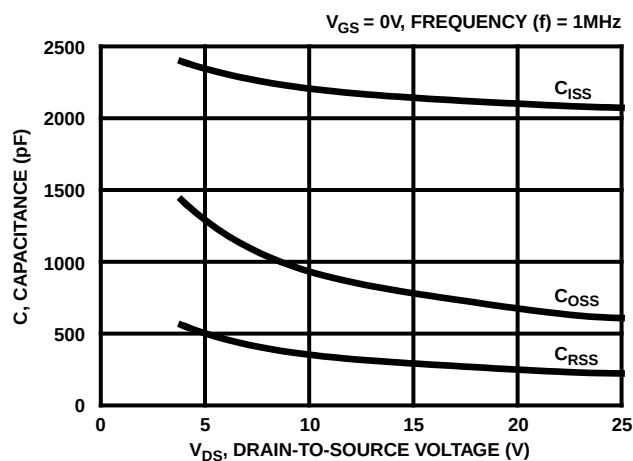


FIGURE 13. TYPICAL CAPACITANCE vs VOLTAGE

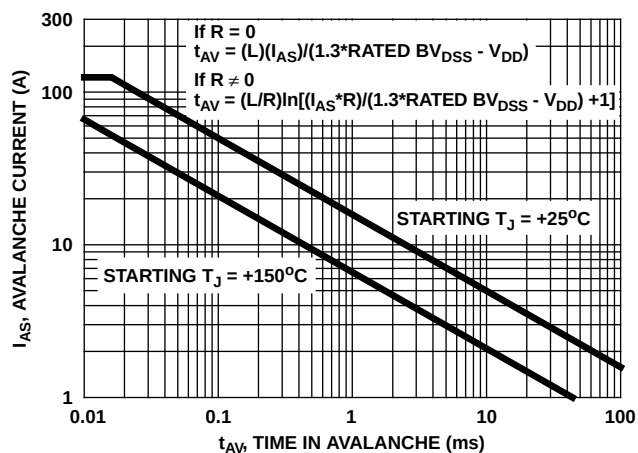


FIGURE 14. UNCLAMPED INDUCTIVE SWITCHING. REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

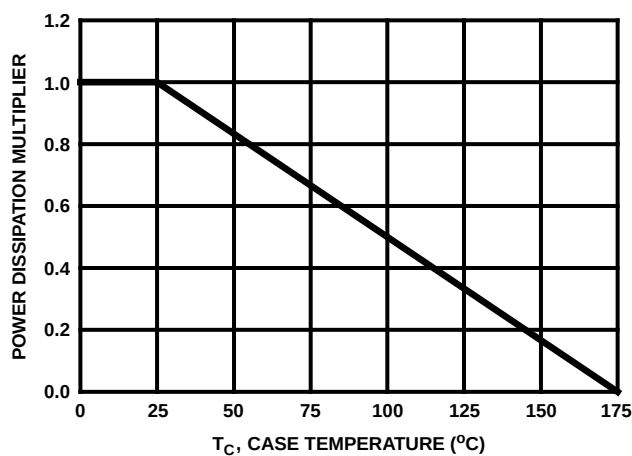


FIGURE 15. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

Test Circuits and Waveforms

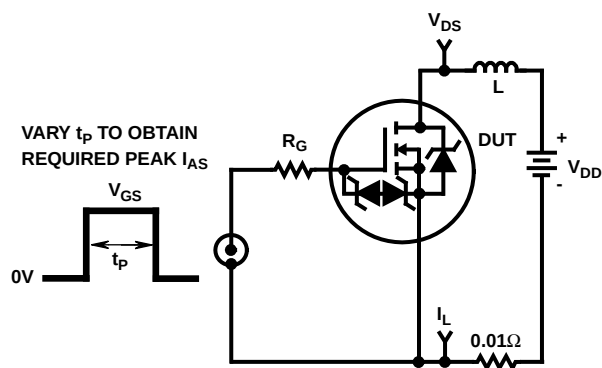


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

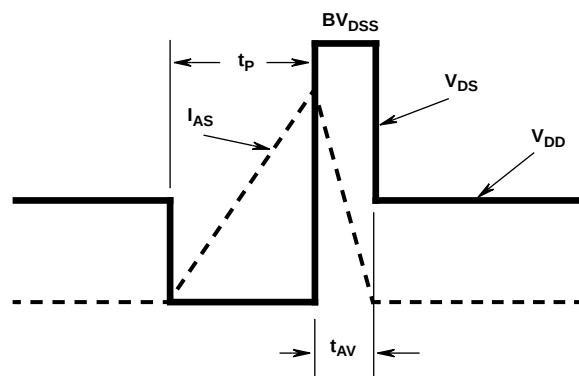


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

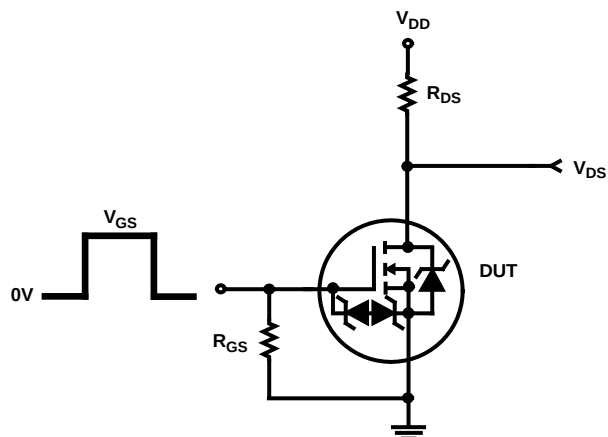


FIGURE 18. RESISTIVE SWITCHING TEST CIRCUIT

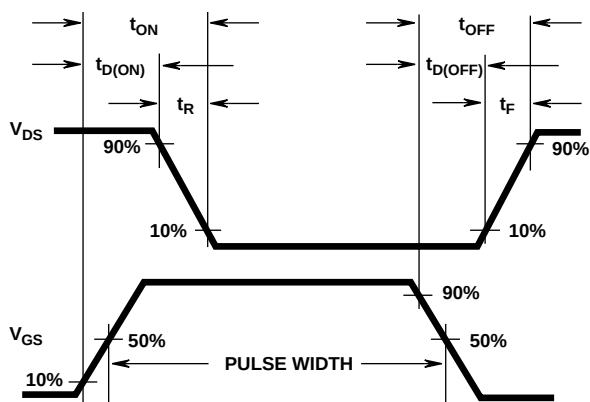


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSpice Model for the RFG50N06LE, RFP50N06LE, RF1S50N06LE, RF1S50N06LESM

CA	12	8	7.0e-9
CB	15	14	7.0e-9
CIN	6	8	1.85e-9

```
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1
```

```
LDRAIN 2 5 1e-9
LGATE 1 9 7.29e-9
LSOURCE 3 7 6.16e-9
```

```
MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD
```

```
RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 3.95e-3
RGATE 9 20 1.18
RLDRAIN 2 5 10
RLGATE 1 9 72.9
RLSOURCE 3 7 61.6
```

```

RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 8.0e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

```

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

ESLC 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*185),4.2))}

```
.MODEL DBODYMOD D (IS = 1.98e-12 RS = 4.90e-3 TRS1 = 2.75e-3 TRS2 = -4.08e-6 CJO = 1.90e-9 TT = 7.15e-8 M = 0.49)
```

```
.MODEL DBREAKMOD D (RS = 1.26e-1 TRS1 = 2.75e-3 TRS2 = -1.17e-5)
```

```
.MODEL DESD1MOD D (BV = 12.75 TBV1 = 0 TBV2 = 0 RS = 0 TRS1 = 0 TRS2 = 0)
```

```
.MODEL DESD2MOD D (BV = 12.75 TBV1 = 0 TBV2 = 0 RS = 54 TRS1 = 0 TRS2 = 0)
```

```
.MODEL DPLCAPMOD D (CJO = 1.36e-9 IS = 1e-30 N = 10 M = 0.56)
```

```
.MODEL MMEDMOD NMOS (VTO = 1.56 KP = 3.50 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 1.18)
```

```
.MODEL MSTROMOD NMOS (VTO = 1.88 KP = 50.00 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
```

```
.MODEL MWEAKMOD NMOS (VTO = 1.34 KP = 0.08 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 11.8 RS = 0.1)
```

```
.MODEL RBREAKMOD RES (TC1 = 9.02e-4 TC2 = 9.18e-7)
```

```
.MODEL RDRAINMOD RES (TC1 = 1.41e-2 TC2 = 7.94e-5)
```

```
.MODEL RSLCMOD RES (TC1 = 3.0e-3 TC2 = 2.0e-6)
```

```
.MODEL RSOURCEMOD RES (TC1 = 0 TC2 = 0)
```

```
.MODEL RVTHRESMOD RES (TC1 = -9.50e-4 TC2 = -9.53e-6)
```

```
.MODEL RVTEMPMOD RES (TC1 = -1.54e-3 TC2 = 1.21e-6)
```

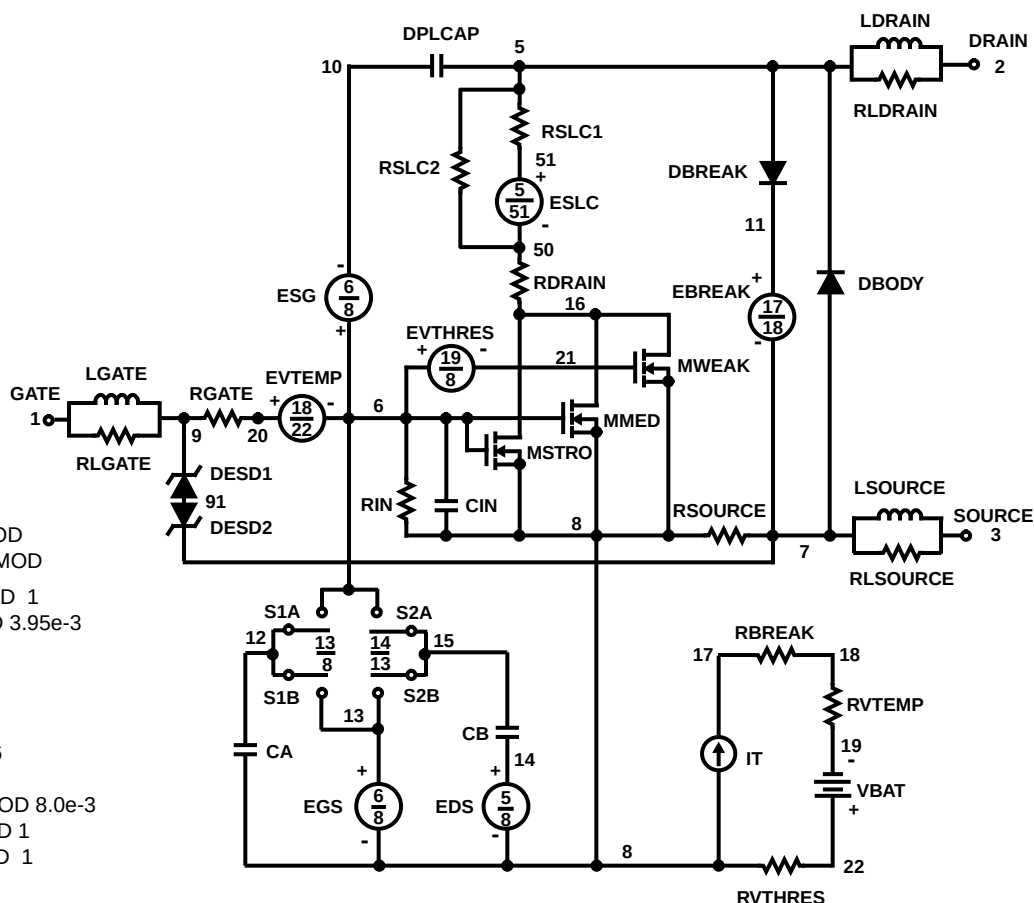
```
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.95 VOFF = -1.95)
```

```
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.95 VOFF = -4.95)
```

```
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.43 VOFF = 1.57)
```

```
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 1.57 VOFF = -1.43)
```

.ENDS

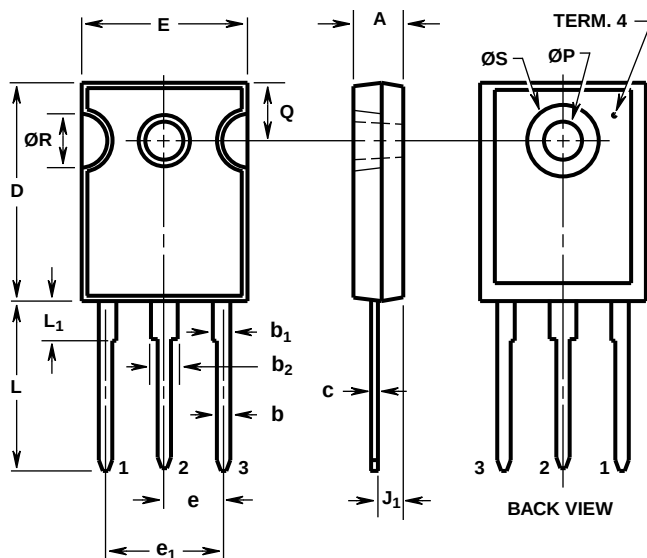


NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records; authors William J. Hepp and C. Frank Wheatley, 1991.

RFG50N06LE, RFP50N06LE, RF1S50N06LE, RF1S50N06LESM

TO-247

3 LEAD JEDEC STYLE TO-247 PLASTIC PACKAGE



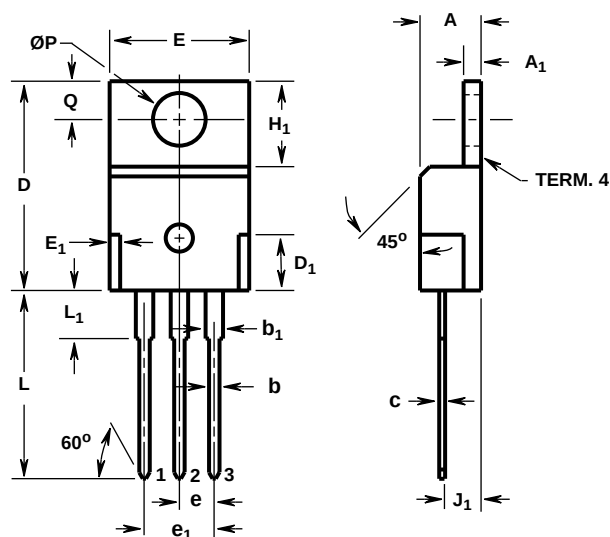
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.180	0.190	4.58	4.82	-
b	0.046	0.051	1.17	1.29	2, 3
b ₁	0.060	0.070	1.53	1.77	1, 2
b ₂	0.095	0.105	2.42	2.66	1, 2
c	0.020	0.026	0.51	0.66	1, 2, 3
D	0.800	0.820	20.32	20.82	-
E	0.605	0.625	15.37	15.87	-
e	0.219 TYP		5.56 TYP		4
e ₁	0.438 BSC		11.12 BSC		4
J ₁	0.090	0.105	2.29	2.66	5
L	0.620	0.640	15.75	16.25	-
L ₁	0.145	0.155	3.69	3.93	1
ØP	0.138	0.144	3.51	3.65	-
Q	0.210	0.220	5.34	5.58	-
ØR	0.195	0.205	4.96	5.20	-
ØS	0.260	0.270	6.61	6.85	-

NOTES:

1. Lead dimension and finish uncontrolled in L₁.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
6. Controlling dimension: Inch.
7. Revision 1 dated 1-93.

TO-220AB

3 LEAD JEDEC TO-220AB PLASTIC PACKAGE



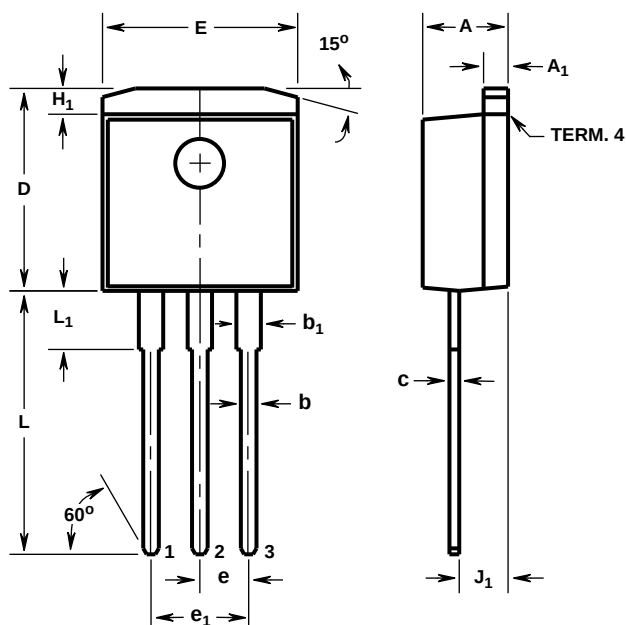
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A ₁	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b ₁	0.045	0.055	1.15	1.39	2, 3
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D ₁	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E ₁	-	0.030	-	0.76	-
e	0.100 TYP		2.54 TYP		5
e ₁	0.200 BSC		5.08 BSC		5
H ₁	0.235	0.255	5.97	6.47	-
J ₁	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
L ₁	0.130	0.150	3.31	3.81	2
ØP	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in L₁.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 1 dated 1-93.

TO-262AA

3 LEAD JEDEC TO-262AA PLASTIC PACKAGE



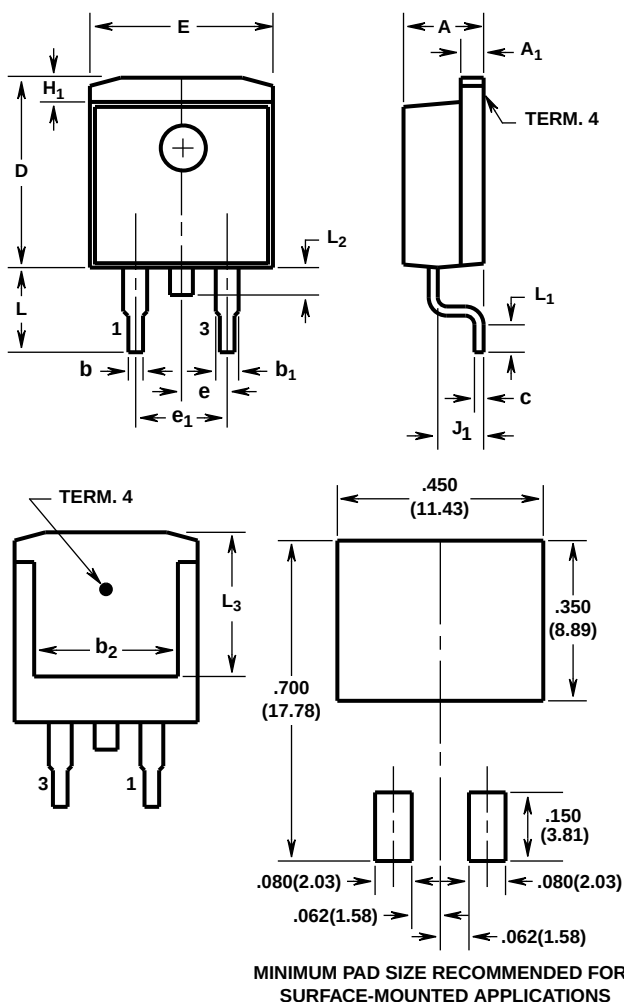
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A ₁	0.048	0.052	1.22	1.32	3, 4
b	0.030	0.034	0.77	0.86	3, 4
b ₁	0.045	0.055	1.15	1.39	3, 4
c	0.018	0.022	0.46	0.55	3, 4
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		5
e ₁	0.200 BSC		5.08 BSC		5
H ₁	0.045	0.055	1.15	1.39	-
J ₁	0.095	0.105	2.42	2.66	6
L	0.530	0.550	13.47	13.97	-
L ₁	0.110	0.130	2.80	3.30	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. A of JEDEC TO-262AA outline dated 6-90.
2. Solder finish uncontrolled in this area.
3. Dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder plating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 4 dated 10-95.

TO-263AB

SURFACE MOUNT JEDEC TO-263AB PLASTIC PACKAGE



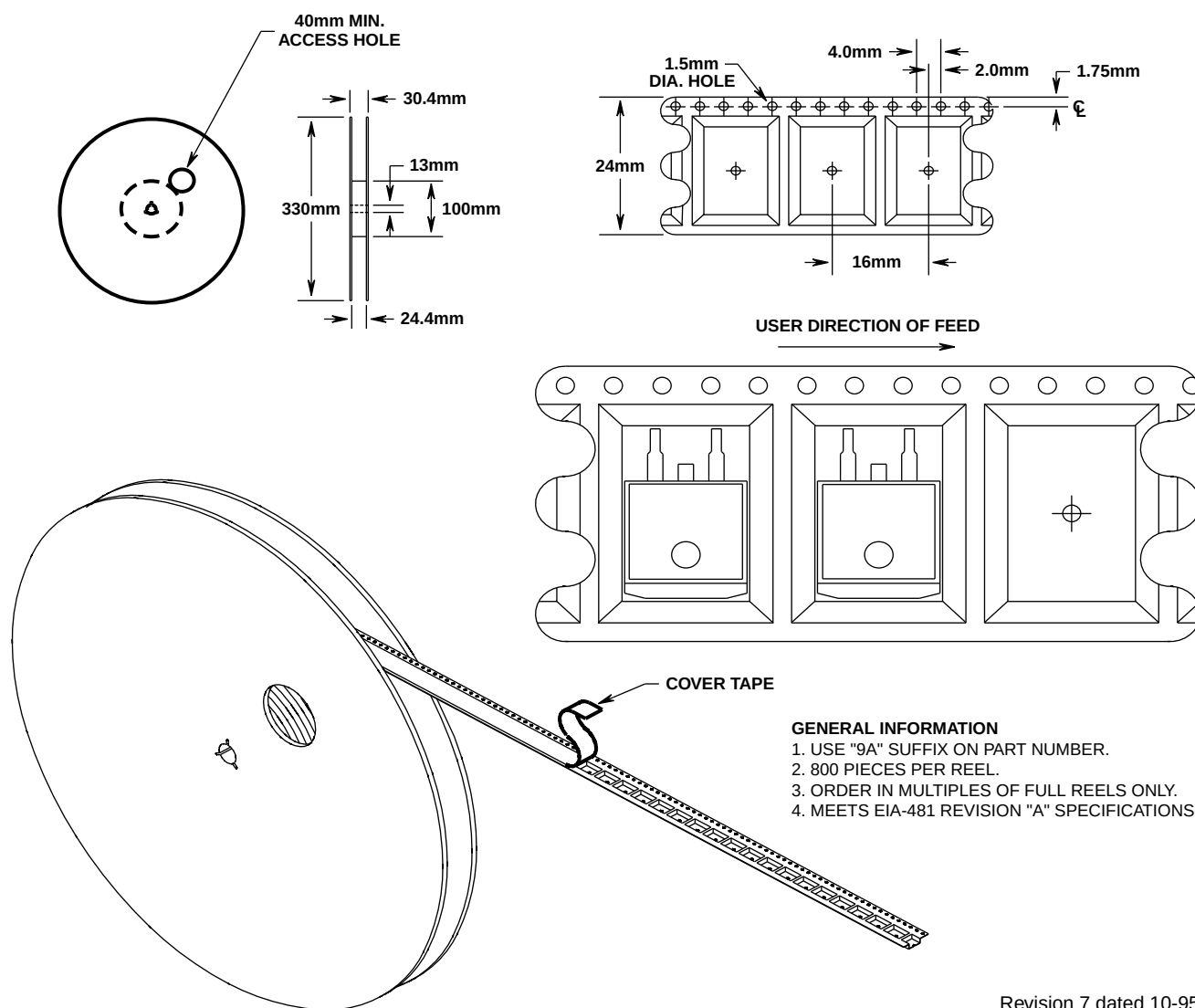
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A ₁	0.048	0.052	1.22	1.32	4, 5
b	0.030	0.034	0.77	0.86	4, 5
b ₁	0.045	0.055	1.15	1.39	4, 5
b ₂	0.310	-	7.88	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		7
e ₁	0.200 BSC		5.08 BSC		7
H ₁	0.045	0.055	1.15	1.39	-
J ₁	0.095	0.105	2.42	2.66	-
L	0.175	0.195	4.45	4.95	-
L ₁	0.090	0.110	2.29	2.79	4, 6
L ₂	0.050	0.070	1.27	1.77	3
L ₃	0.315	-	8.01	-	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-263AB outline dated 2-92.
2. L₃ and b₂ dimensions established a minimum mounting surface for terminal 4.
3. Solder finish uncontrolled in this area.
4. Dimension (without solder).
5. Add typically 0.002 inches (0.05mm) for solder plating.
6. L₁ is the terminal length for soldering.
7. Position of lead to be measured 0.120 inches (3.05mm) from bottom of dimension D.
8. Controlling dimension: Inch.
9. Revision 7 dated 10-95.

TO-263AB

24mm TAPE AND REEL



GENERAL INFORMATION

1. USE "9A" SUFFIX ON PART NUMBER.
2. 800 PIECES PER REEL.
3. ORDER IN MULTIPLES OF FULL REELS ONLY.
4. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

Revision 7 dated 10-95

All Harris Semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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Sales Office Headquarters

For general information regarding Harris Semiconductor and its products, call **1-800-4-HARRIS**

UNITED STATES
Harris Semiconductor
P. O. Box 883, Mail Stop 53-210
Melbourne, FL 32902
TEL: 1-800-442-7747
(407) 729-4984
FAX: (407) 729-5321

EUROPE
Harris Semiconductor
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Harris Semiconductor PTE Ltd.
No. 1 Tannery Road
Cencon 1, #09-01
Singapore 1334
TEL: (65) 748-4200
FAX: (65) 748-0400

