

FEATURES

- Max. transparent propagation delay of 900ps
- Min. Master Reset and Enable pulse widths of 100ps
- IEE min. of -98mA
- Industry standard 100K ECL levels
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75kΩ input pull-down resistors
- More than 40% faster than Fairchild
- Approximately 30% lower power than Fairchild
- Function and pinout compatible with Fairchild F100K
- Available in 28-pin PLCC package

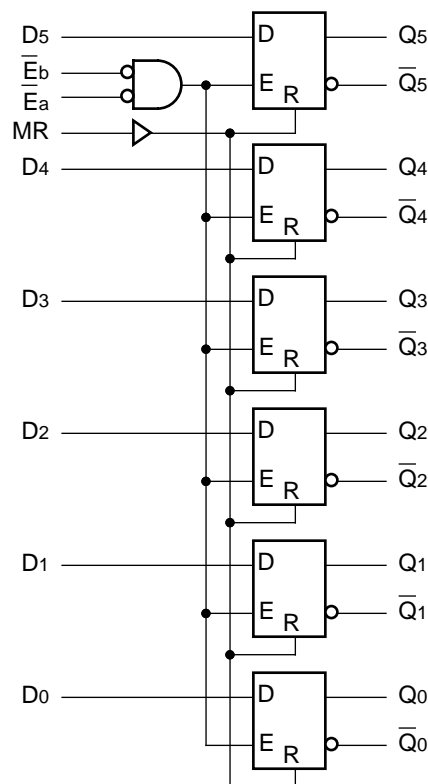
DESCRIPTION

The SY100S350 offers six high-speed D-Latches with both true and complement outputs, and is performance compatible for use with high-performance ECL systems. When both enable signals (\bar{E}_a and \bar{E}_b) are at a logic LOW, the latches are transparent and the input signals(D₀–D₅) appear at the outputs (Q₀–Q₅) after a propagation delay. If either or both of the enable signals are at a logic HIGH, then the latches store the last valid data present on its inputs before \bar{E}_a or \bar{E}_b went to a logic HIGH. The Master Reset (MR) overrides all other input signals and takes the outputs to a logic LOW state. All inputs have 75kΩ pull-down resistors.

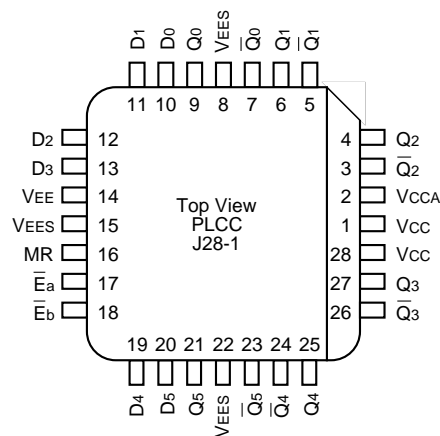
PIN NAMES

| Pin | Function |
|---------------------------------|-----------------------------------|
| D ₀ — D ₅ | Data Inputs |
| \bar{E}_a , \bar{E}_b | Common Enable Inputs (Active LOW) |
| MR | Asynchronous Master Reset Input |
| Q ₀ — Q ₅ | Data Outputs |
| \bar{Q}_0 — \bar{Q}_5 | Complementary Data Outputs |
| VEES | VEE Substrate |
| VCCA | VCCO for ECL Outputs |

BLOCK DIAGRAM



PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
|---------------------------------|--------------|-----------------|---|-------------|
| SY100S350JC | J28-1 | Commercial | SY100S350JC | Sn-Pb |
| SY100S350JCTR ⁽¹⁾ | J28-1 | Commercial | SY100S350JC | Sn-Pb |
| SY100S350JZ ⁽²⁾ | J28-1 | Commercial | SY100S350JZ with Pb-Free bar-line indicator | Matte-Sn |
| SY100S350JZTR ^(1, 2) | J28-1 | Commercial | SY100S350JZ with Pb-Free bar-line indicator | Matte-Sn |

- Notes:
- 1. Tape and Reel.
 - 2. Pb-Free package is recommended for new designs.

TRUTH TABLE⁽¹⁾

Each Latch

| Inputs | | | | Outputs | | Operating Mode |
|----------------|-------------|-------------|----|------------------------|------------------------|----------------|
| D _n | \bar{E}_a | \bar{E}_b | MR | Q _n | \bar{Q}_n | |
| H | L | L | L | H | L | Latch |
| L | L | L | L | L | H | |
| X | X | H | L | Latched ⁽²⁾ | Latched ⁽²⁾ | |
| X | H | X | L | Latched ⁽²⁾ | Latched ⁽²⁾ | |
| X | X | X | H | L | H | Asynchronous |

- NOTES:
- 1. H = HIGH State
L = LOW State
X = Don't Care
 - 2. Retains data that is present before \bar{E} positive transition.

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

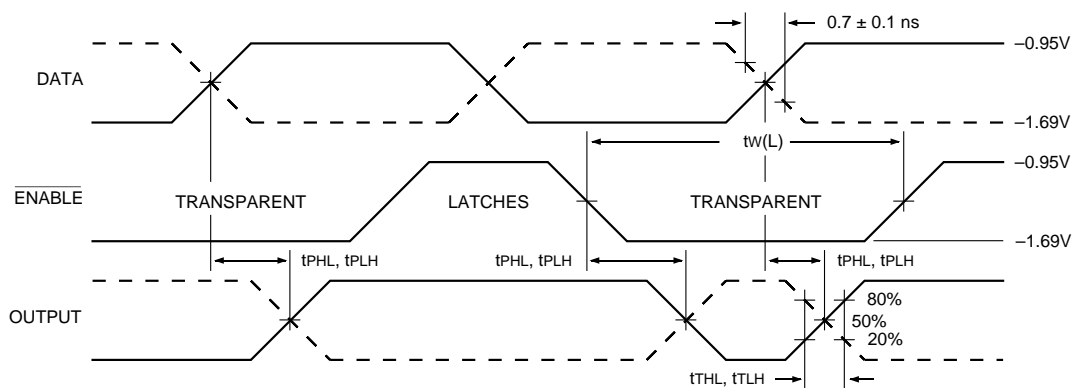
| Symbol | Parameter | Min. | Typ. | Max. | Unit | Condition |
|----------|------------------------|------|------|------|---------|--------------------------|
| I_{IH} | Input HIGH Current | — | — | 250 | μA | $V_{IN} = V_{IH} (Max.)$ |
| | MR | — | — | 250 | | |
| | D_n | — | — | 250 | | |
| | \bar{E}_a, \bar{E}_b | — | — | 250 | | |
| I_{EE} | Power Supply Current | -98 | -78 | -49 | mA | Inputs Open |

AC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$

| Symbol | Parameter | $T_A = 0^\circ C$ | | $T_A = +25^\circ C$ | | $T_A = +85^\circ C$ | | Unit | Condition |
|------------------------|---|-------------------|------|---------------------|------|---------------------|------|------|-----------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| t_{PLH} t_{PHL} | Propagation Delay D_n to Output | 300 | 900 | 300 | 900 | 300 | 900 | ps | |
| t_{PLH} t_{PHL} | Propagation Delay E_a, E_b to Output | 300 | 1000 | 300 | 1000 | 300 | 1000 | ps | |
| t_{PLH} t_{PHL} | Propagation Delay MR to Output | 300 | 1200 | 300 | 1200 | 300 | 1200 | ps | |
| t_{TLH} t_{THL} | Transition Time 20% to 80%, 80% to 20% | 300 | 900 | 300 | 900 | 300 | 900 | ps | |
| t_s | Set-up Time, D_n to E_n | 500 | — | 500 | — | 500 | — | ps | |
| t_h | Hold Time, D_n to E_n | 500 | — | 500 | — | 500 | — | ps | |
| t_r | Release Time, MR to E_n | 1000 | — | 1000 | — | 1000 | — | ps | |
| $t_{PW} (L)$ | Pulse Width, E_a, E_b | 1000 | — | 1000 | — | 1000 | — | ps | |
| $t_{PW} (H)$ | Pulse Width, MR | 1000 | — | 1000 | — | 1000 | — | ps | |

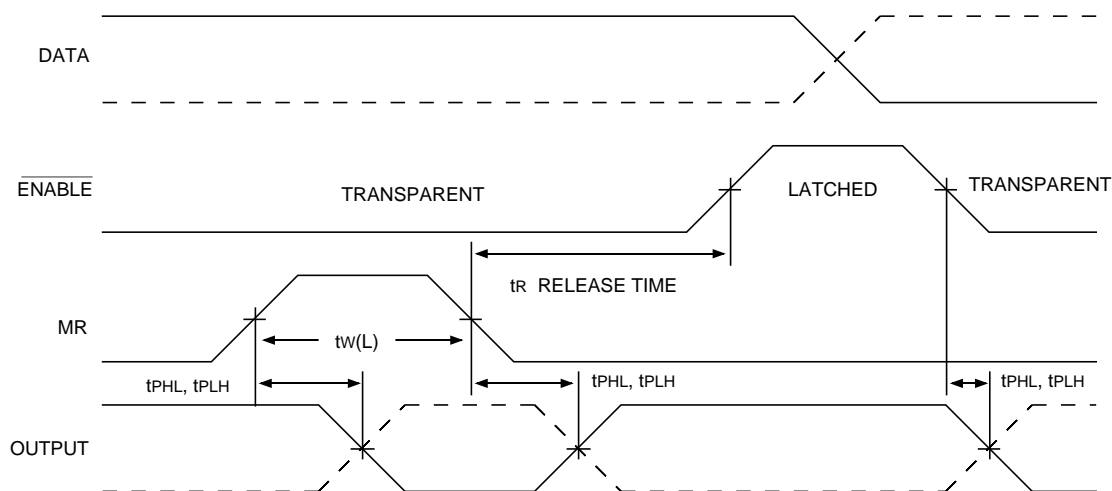
TIMING DIAGRAMS



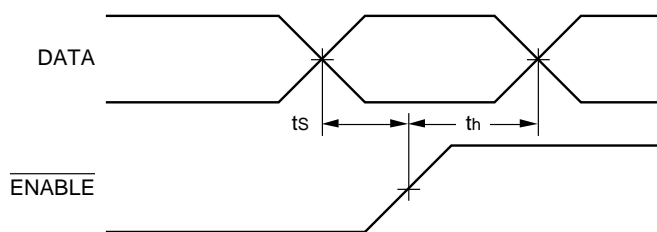
Enable Timing

Note:

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$



Reset Timing



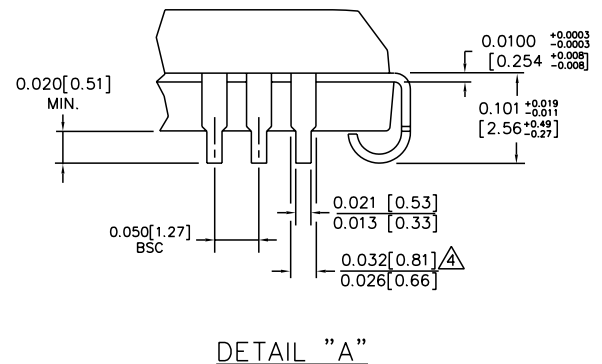
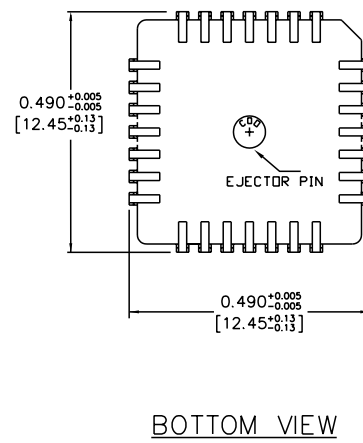
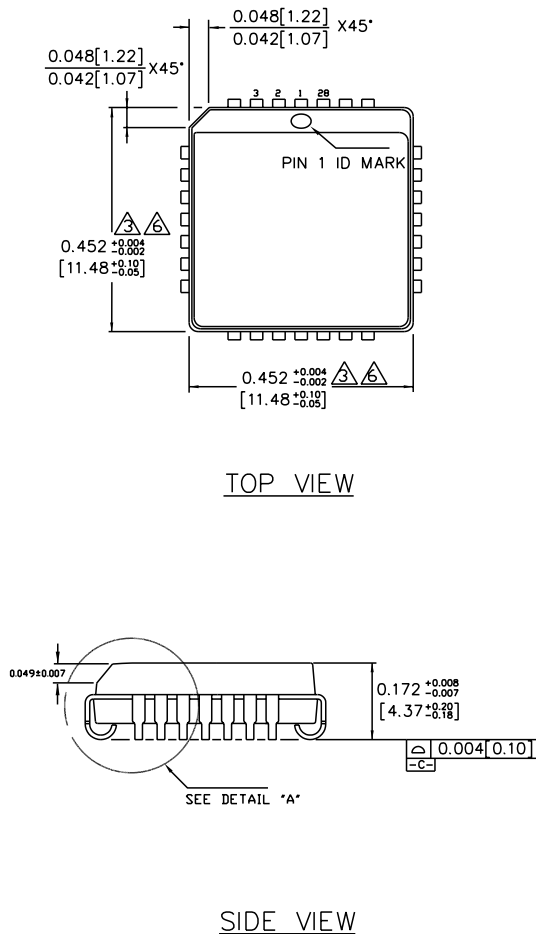
Data Set-up and Hold Times

Notes:

t_s is the minimum time before the transition of the clock that information must be present at the data input.

t_h is the minimum time after the transition of the clock that information must remain unchanged at the data input.

28-PIN PLCC (J28-1)



NOTES:

1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

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MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB <http://www.micrel.com>

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