MN4046B / MN4046BS

Phase-Locked Loops

■ Description

This MN4046B/S are phase-locked loop circuits composed of two phase comparators, VCO, source follower and zener diode.
The two comparators have common signal inputs $SIGN_{IN}$ and $COMP_{IN}$.
$SIGN_{IN}$ should be used by directly connecting to large voltage signals or by connecting small voltage signal through serial capacitors.
Small voltage signals are adjusted to the linear area of the amplifier by the self-bias circuit.
Phase comparator 1 is an Exclusive-OR gate which outputs digital error signal $PC1_{OUT}$, and shifts phase by 90° with the central frequency between $SIGN_{IN}$ signal and $COMP_{IN}$ signal (50% duty cycle)
Phase comparator 2 outputs digital error signals PC_{OUT} and PCP_{OUT} and phase shifts between $SIGN_{IN}$ and $COMP_{IN}$ (duty cycle is arbitrary) is 0°.
The frequency of signal VCO_{OUT} obtained by the linear VCO is defined by the voltage of input VCO_{IN} and the constant of the resistor and capacitor connected to R_1, R_2, C_{1A} and C_{1B}.
When VOC_{IN} signal is necessary and there is no space for loading, source follower output SF_{OUT} together with an external resistor is used. When inhibit input INH is "1" level, stand-by power dissipation can be minimized because the VCO and source follower are disabled.
A zener diode should be used to adjust the power supply source.
The MN4046B/S can be widely used for modulation and demodulation of FM and FSK, composition and discrimination of frequencies, tone decoding, synchronization and adjustment of data, and conversion of voltage and frequencies.

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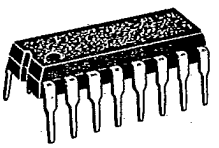

16-Pin • Plastic DIL Package

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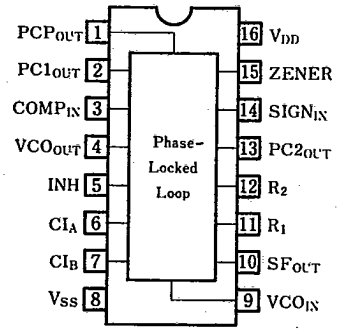
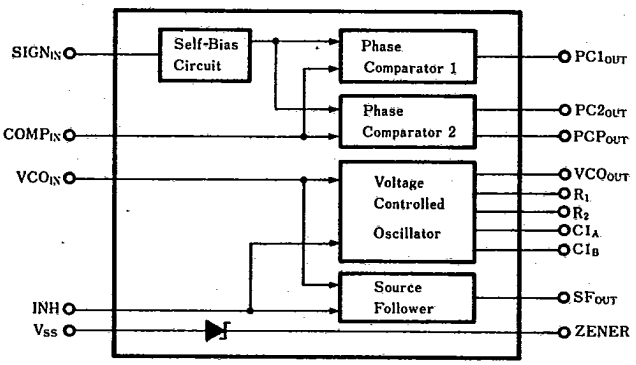
16-Pin • Panaflat Package (SO-16D)

Pin Configuration



■ Block Diagram



■ Maximum Ratings (Ta=25℃)

Item		Symbol	Ratings	Unit
Supply Voltage		V_{DD}	−0.5～+18	V
Input Voltage		V_I	−0.5～V_{DD}+0.5*	V
Output Voltage		V_O	−0.5～V_{DD}+0.5*	V
Peak Input · Output Current		$\pm I_I$	max. 10	mA
Power Dissipation (per package)	Ta=−40～+60℃	P_D	max. 400	mW
	Ta=+60～+85℃		Decrease up to 200mW rating at 8mW/°C	
Power Dissipation (per output terminal)		P_D	max. 100	mW
Operating Ambient Temperature		Topr	−40～+85	℃
Storage Temperature		Tstg	−65～+150	℃

* V_{DD} + 0.5V should be under 18V

■ DC Characteristics (V_{SS}=0V)

Item	V_{DD} (V)	Symbol	Conditions		Ta=−40℃ min.	Ta=−40℃ max.	Ta=25℃ min.	Ta=25℃ max.	Ta=85℃ min.	Ta=85℃ max.	Unit
Quiescent Power Supply Current	5	I_{DD}	INH = H, $SIGN_{IN}$ = H		—	20	—	20	—	150	μA
	10				—	40	—	40	—	300	
	15				—	80	—	80	—	600	
Output Voltage Low Level	5	V_{OL}	V_I=V_{SS} or V_{DD} $\lvert I_O\rvert$<1μA		—	0.05	—	0.05	—	0.05	V
	10				—	0.05	—	0.05	—	0.05	
	15				—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	V_I=V_{SS} or V_{DD} $\lvert I_O\rvert$<1μA		4.95	—	4.95	—	4.95	—	V
	10				9.95	—	9.95	—	9.95	—	
	15				14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{IL}	$\lvert I_O\rvert$<1μA	V_O=0.5V or 4.5V	—	1.5	—	1.5	—	1.5	V
	10			V_O=1V or 9V	—	3	—	3	—	3	
	15			V_O=1.5V or 13.5V	—	4	—	4	—	4	
Input Voltage High Level	5	V_{IH}	$\lvert I_O\rvert$<1μA	V_O=0.5V or 4.5V	3.5	—	3.5	—	3.5	—	V
	10			V_O=1V or 9V	7	—	7	—	7	—	
	15			V_O=1.5V or 13.5V	11	—	11	—	11	—	
Output Current Low Level	5	I_{OL}	V_O=0.4V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=0.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=1.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=4.6V, V_I=0 or 5V		0.52	—	0.44	—	0.36	—	mA
	10		V_O=9.5V, V_I=0 or 10V		1.3	—	1.1	—	0.9	—	
	15		V_O=13.5V, V_I=0 or 15V		3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{OH}$	V_O=2.5V, V_I=0 or 5V		1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_I$	V_I=0 or 15V		—	0.3	—	0.3	—	1	μA
Input Capacitance		C_I			—	—	—	7.5	—	—	pF

Electrical Characteristics

• Switching Characteristics ($Ta=25℃$, $V_{SS}=0V$, $C_L=50pF$)

Item	V_{DD} (V)	Symbol	Condition	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}		—	60	180	ns
	10			—	30	90	
	15			—	20	60	
Output Fall Time	5	t_{THL}		—	60	180	ns
	10			—	30	90	
	15			—	20	60	

• Phase · Comparator

Item		V_{DD} (V)	Symbol	Condition	min.	typ.	max.	Unit
Input Resistance	$SIGN_{IN}$	5	R_{IN}		—	750	—	kΩ
		10			—	220	—	
		15			—	140	—	
	$COMP_{IN}$	15			—	—	—	
Minimum Input Sensitivity		5	V_{IN}	AC Couple-$SIGN_{IN}$	—	150	—	mV_{P-P}
		10		$R_1=10k\Omega$, $R_2=\infty$	—	150	—	
		15		$C_1=100pF$	—	200	—	
DC Couple-$SIGN_{IN}$: $COMP_{IN}$ Low Level		5	V_{IL}		—	—	1.5	V
		10			—	—	3	
		15			—	—	4	
DC Couple-$SIGN_{IN}$: $COMP_{IN}$ High Level		5	V_{IH}		3.5	—	—	V
		10			7	—	—	
		15			11	—	—	

• Voltage Control Oscillator

Item	V_{DD} (V)	Symbol	Condition		min.	typ.	max.	Unit
Maximum Frequency	5	fmax	$VCO_{IN}=V_{DD}$		0.5	1	—	MHz
	10		$R_1=10k\Omega$, $R_2=\infty$		1	2	—	
	15		$C_1=50pF$		1.3	2.7	—	
Temperature-Frequency Stability	5		$R_2=\infty$		—	0.12	—	%/℃
	10				—	0.04	—	
	15				—	0.015	—	
Linearity	5		$R_2=\infty$	$VCO_{IN}=2.50V\pm0.30V$, $R_1>10k\Omega$	—	0.50	—	%
	10			$VCO_{IN}=5.00V\pm2.50V$, $R_1>400k\Omega$	—	0.25	—	
	15			$VCO_{IN}=7.50V\pm5.00V$, $R_1=1M\Omega$	—	0.25	—	
Output Duty Cycle	5 ~ 15	δ			—	50	—	%
Input Resistance (VCO_{IN})	5 ~ 15	R_{IN}			—	10^6	—	MΩ

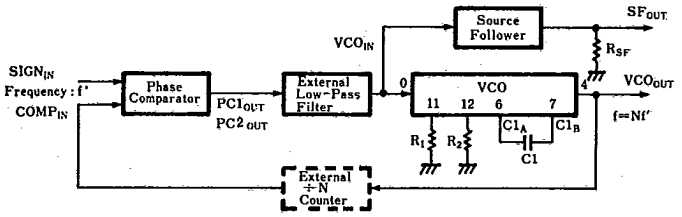
• Source · Follower

Item	V_{DD} (V)	Symbol	Condition	min.	typ.	max.	Unit
Offset Voltage	5		$VCO_{IN}-SF_{OUT}$, $R_{SF}=50k\Omega$	—	1.5	—	V
	10			—	1.7	—	
	15			—	1.8	—	
Linearity	5		$VCO_{IN}=2.50V\pm0.30V$, $R_{SF}>50k\Omega$	—	0.3	—	%
	10		$VCO_{IN}=5.00V\pm2.50V$, $R_{SF}>50k\Omega$	—	1.0	—	
	15		$VCO_{IN}=7.50V\pm5.00V$, $R_{SF}>50k\Omega$	—	1.3	—	

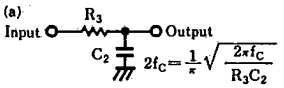
● **Zener Diode**

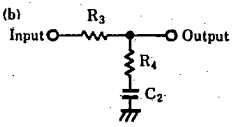
Item	V_{DD} (V)	Symbol	Condition	min.	typ.	max.	Unit
Zener Voltage		V_Z	$I_Z = 50\mu A$	—	7.3	—	V
Action Resistance		R_Z	$I_Z = 1$ mA	—	25	—	Ω

(Fig. 1) General PLL Connections

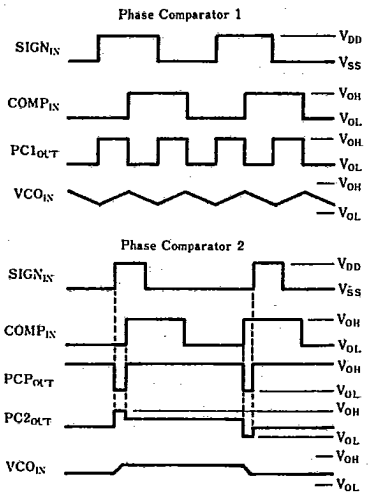


Typical Low-Pass Filters





Cut-off Frequency



(Fig. 2) Phase · Comparator Mode Diagrams