STi5267

Advanced SD STB decoder
with integrated DVB-T/DVB-C demodulator

Data brief

Features

- Combined DVB-T/-C receiver
  - Compatible with low to high IF tuners
  - DVB-T demodulation
  - DVB-C demodulation
  - DVB-CI compliant output
  - I²C serial bus interface

- Advanced standard-definition video decoding (H264/VC-1/MPEG2/AVS)

- Advanced multi-channel audio decoding (MPEG 1, 2, MP 3, DD/DD+, AAC/AAC+, and WMA9/WMA9pro)

- Linux, Windows CE, and OS21 compatible ST40 applications CPU (450 MHz)

- 16-bit DDR1/DDR2 compatible local memory interface

- Multi-stream, DVR capable transport stream processing

- Extensive connectivity (dual USB 2.0 hosts, e-SATA (optional), Ethernet MAC/MII/RMII, and PCI)

- Advanced security and DRM support including SVP, MS-DRM, and DTCP-IP

Description

The STi5267 uses state-of-the-art process technology to provide a fully featured SD AVC, DVB-C, and DVB-T demodulator/decoder IC.

It is a highly integrated system-on-chip, suitable for STB markets across cable, terrestrial, and terrestrial/IP hybrid networks worldwide.

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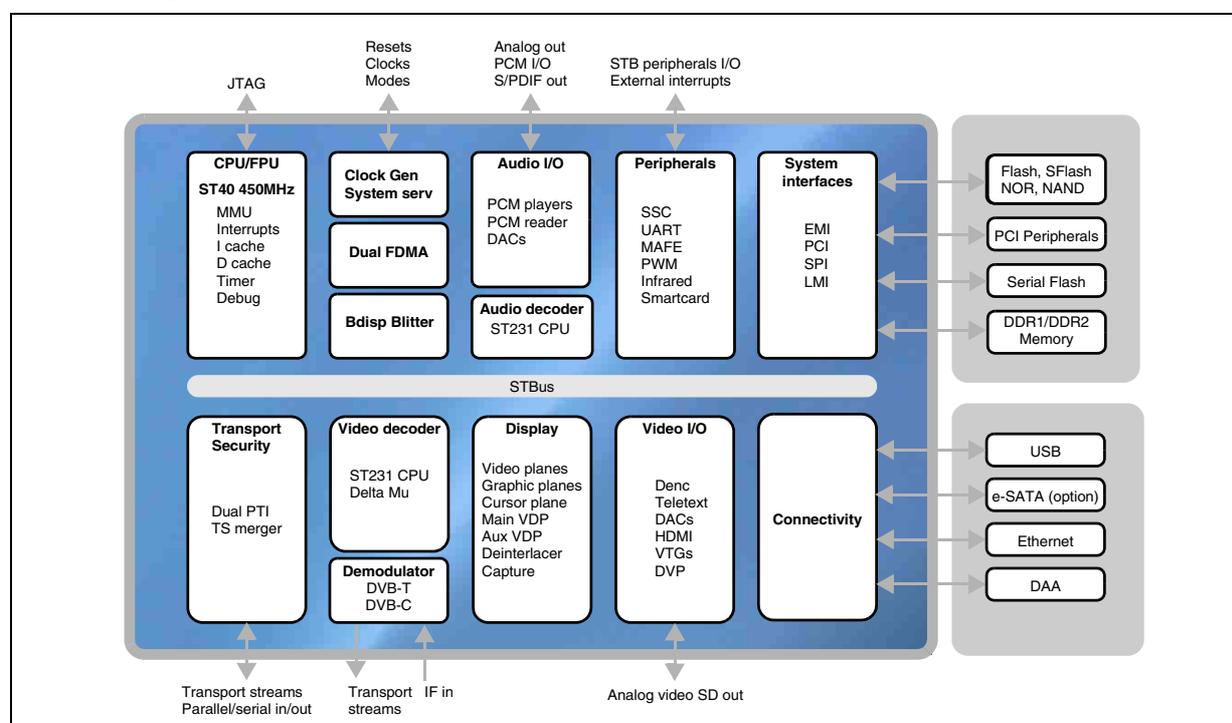
1   Introduction

The STi5267 is targeted at the latest Operator and CE manufacturer requirements for STBs that use advanced SD decoding (H264/VC-1/MPEG2), and which conform to DVB, ISMA, ATIS-IIF, SCTE, ATSC, ARIB, CEA, ITU, OpenCable and MSTV specifications.

The STi5267 provides a solution for operators to specify a range of low-cost, high performance SD STBs including low-cost zappers, IP clients, interactive STBs, DVR standalone and DVR server/home network-capable STBs, and with content delivery possible using broadcast or broadband networks, or both (hybrid STBs). The STi5267 keeps pace with the latest conditional access, DRM and trusted platform requirements of major operators worldwide by incorporating the latest generation of advanced security features.

The STi5267 offers current users of ST's growing family of advanced decoding ICs enhancements in performance and features, while reducing cost and time-to-market for the next generation deployments.

Features	Benefits
Combines a configurable DVB-C/DVB-T demodulator with STB decoding and display functions	This highly integrated SoC helps to reduce board area and manufacturing cost, allowing low cost and small size STBs to be designed for either DVB-C or DVB-T networks
ST40-300 applications CPU @450MHz, 32K I cache, 32K D cache	Up to 800DMIPs superscalar performance from a single CPU core, using standard tools and operating systems (Linux, OS21)
STMicroelectronics' DELTA video decoding system with ST231 processor	Decoding of advanced high definition standards for MPEG2, H264, VC-1 broadcast, with the performance and flexibility for web-based content decoding such as Flash, DivX, MJPEG and Real
Dual USB 2.0 hosts, optional e-SATA, Ethernet MAC with MII/RMII and TMII, PCI	Extensive high speed connectivity for the widest range of STB peripherals, such as Flash drives, external HDDs, home network controllers (for example MoCA, Wi-Fi), DOCSIS modem and so on
Low power process, design and architecture	Best in class, low power standby mode, to meet emerging energy standards for STBs. Dynamic configuration of power to individual sub-systems enables power-efficient active standby modes
Advanced 2D graphics and display subsystem which also supports 3D user interface effects and 1080p60 display output	Allows visually appealing user interfaces and video rich navigation to be offered to consumers, while high quality progressive output can be watched on the latest high definition displays

1.1 STi5267 features summary

The STi5267 has the following main features:

1.1.1 COFDM demodulation

● General features:
  – Compatible with low to high IF tuners
  – Wide-range carrier tracking loop for large offsets recovery
  – Dual ADC for IQ baseband interface
  – ADC for RF signal strength indicator
  – Dual SD digital split AGC for RF and IF/BB gain control
  – Flexible clock management uses external reference from 4 to 30 MHz
● Channel impairments management:
  – Nordig Unified (v2.0) compliant
  – DTG 5.0 and Digitenne compliant
  – Outstanding performance in various channel configurations: dynamic fading, urban environment
  – Built-in channel reception quality indicators
  – Out-of-guard interval echoes compatible
  – Impulsive noise rejection capable
  – Outstanding adjacent and co-channel rejection capability with integrated and flexible digital channel filtering
  – High-performance digital carrier, timing and symbol recovery loops
● Decoding capabilities:
  – ETSI EN-300744 v1.5.1 compatible
  – 2-K and 8-K FFT length
  – 6, 7 and 8 MHz channel bandwidths
  – 1/4, 1/8, 1/16, 1/32 guard-interval length
  – QPSK - 16QAM - 64QAM modulations
  – Hierarchical modulation capability
  – TPS decoding
  – Puncture rates are 1/2, 2/3, 3/4, 5/6, 7/8
  – Outer Reed-Solomon decoder as per DVB-T standard
  – Energy dispersal descrambler

1.1.2 QAM demodulation

● Decodes ITU-T J.83-Annexes A/C and DVB-C bit streams
● High-performance integrated ADC for direct IF architecture in all QAM modes
● Supports 16, 32, 64, 128 and 256 point constellations
● Variable symbol rates
● Front derotator for better low symbol rate performance and relaxed tuner constraints
● Integrated matched filtering
● Robust integrated adaptive pre- and post- high multi-tap equalizer
● On-chip FEC A/C with ability to bypass individual blocks
● Built-in clock management for operation from a flexible 4 MHz to 30 MHz external reference
● Fast signal acquisition
● ADC for RF signal strength indicator

1.1.3 Interfaces

● I²C serial bus interface:
● Fast, up to 400 kHz slave interface
● Four possible slave addresses
● Flexible and DVB-CI compliant TS output

1.1.4 Processor core

The STi5267 integrates a 450 MHz ST40-300 processor core that features a 32-bit superscalar RISC CPU and IEEE-754 compliant floating point unit (FPU). The ST40-300 includes two-way, set-associative caches and an interrupt controller with 15 user interrupt sources and an interrupt expansion port.

1.1.5 External memory interface (EMI)

The EMI is a general-purpose interface for attaching Flash memory and peripherals. The EMI features are:
● Five banks
● Addressing up to at least 64 Mbytes of NOR Flash
● External bus master support through BUSREQ/BUSGNT signals
● Slave Mode EMI support
● Single level cell (SLC) NAND Flash and boot from SLC NAND Flash
● Serial Flash support
● PCI interface, host and device selected on boot
● ATAPI PIO mode 4
● DVB-CI+

1.1.6 Local memory interface (LMI)

The STi5267 integrates one 16-bit DDR2-DDR1 interface. The interface can run up to 400 MHz when configured in DDR2 mode or up to 250 MHz when in DDR1 mode.
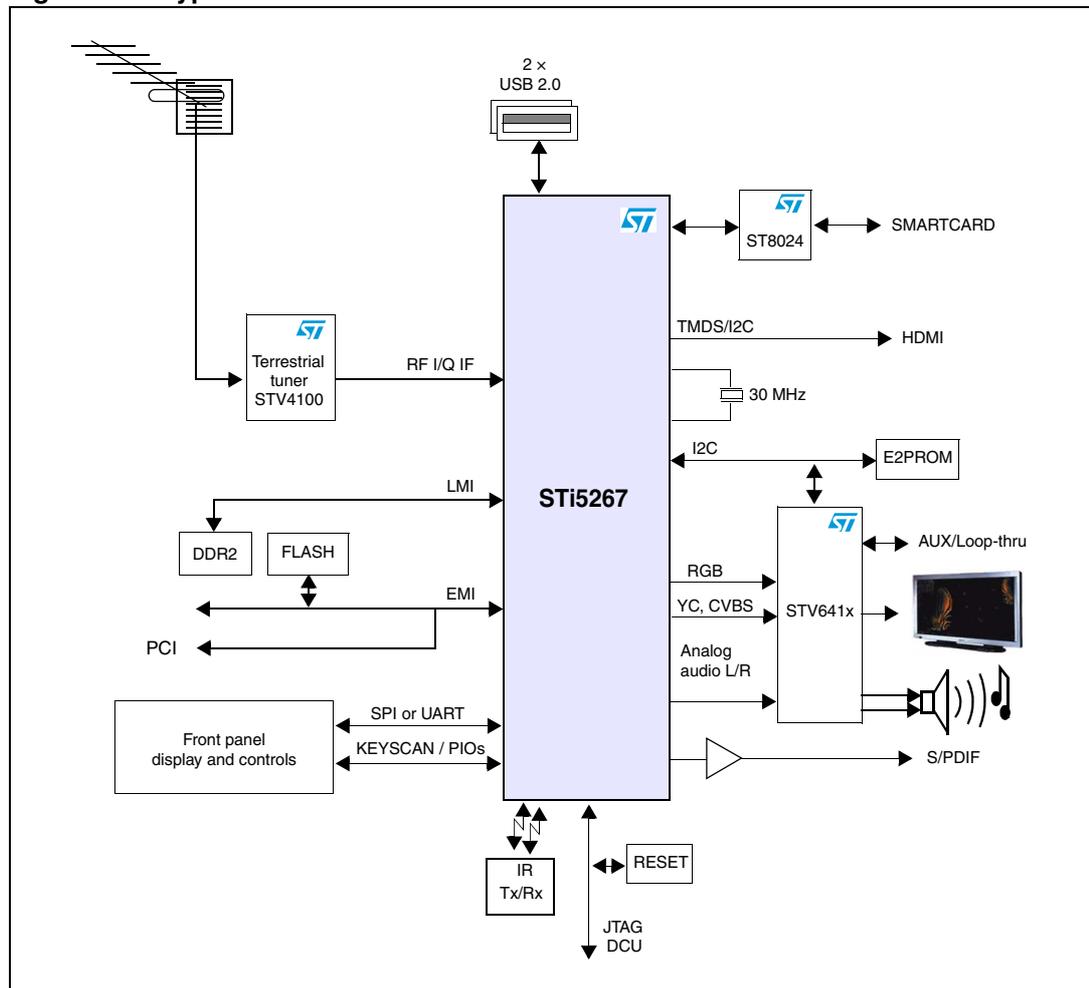
The LMI supports 16-bit configurations, including:

● 1 × 512 Mbits (×16) devices resulting in 64 Mbytes memory space
● 1 × 1 Gbits (×16) devices resulting in 128 Mbytes memory space
● 1 × 2 Gbits (×16) devices resulting in 256 Mbytes memory space
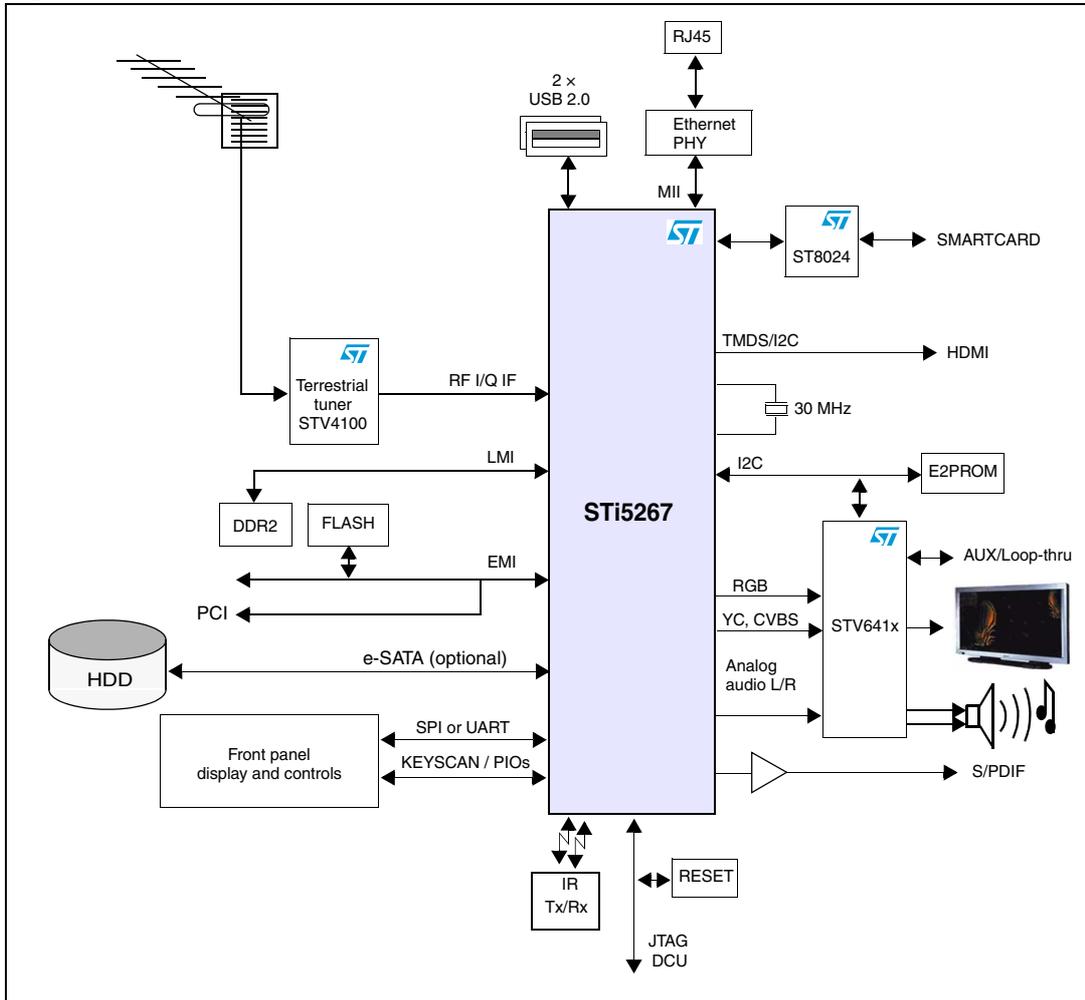
2 Target applications

2.1 Terrestrial STB
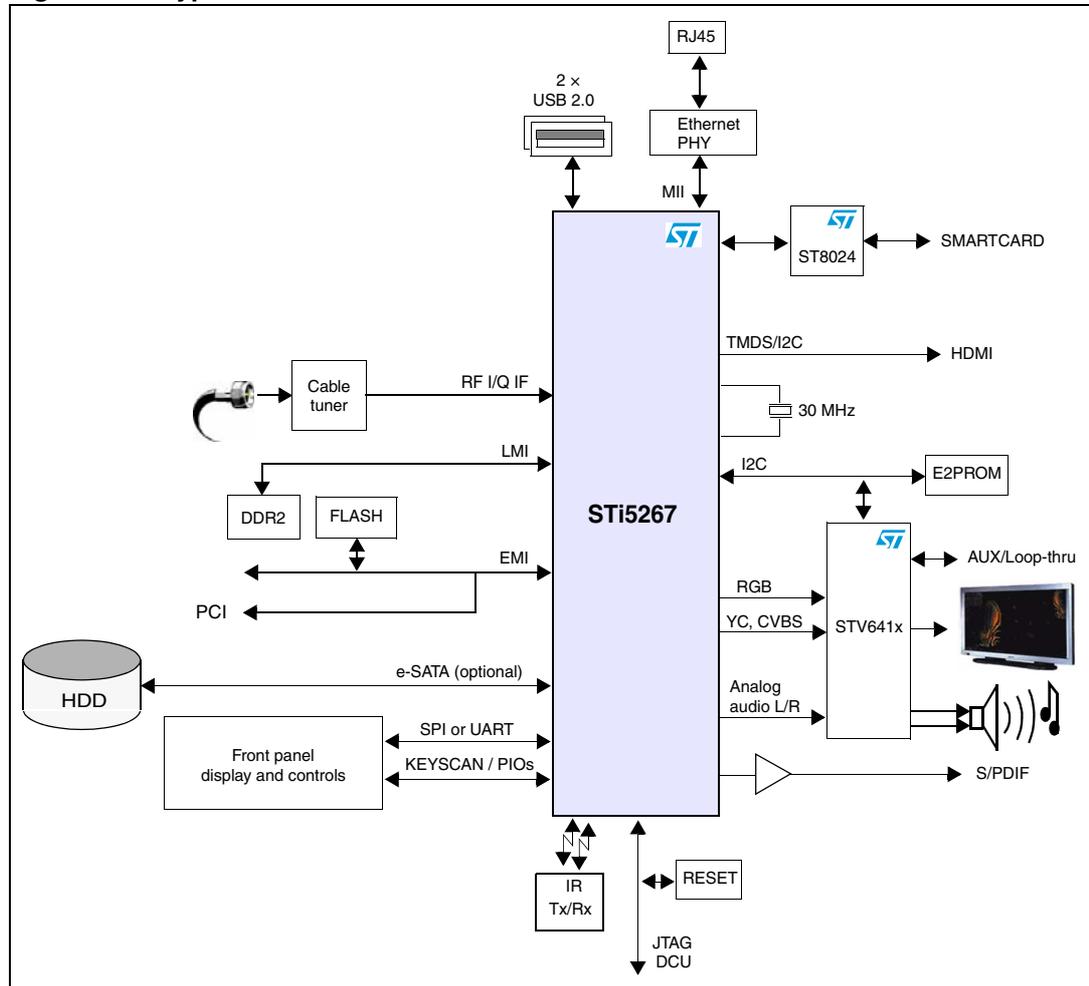
Figure 1.   Typical terrestrial STB

2.2 Hybrid IP/terrestrial STB

Figure 2. Typical hybrid IP/terrestrial STB

2.3 Cable applications

Figure 3. Typical DVR cable STB

3 Ordering information

Table 1. Ordering information

Order code	Packaging	Description
STi5267ZUC	FPBGA 27 mm × 27 mm	Development version, all options

4 Revision history

Table 2. Document revision history

Date	Revision	Changes
07-Jan-2010	1	Initial release.

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