



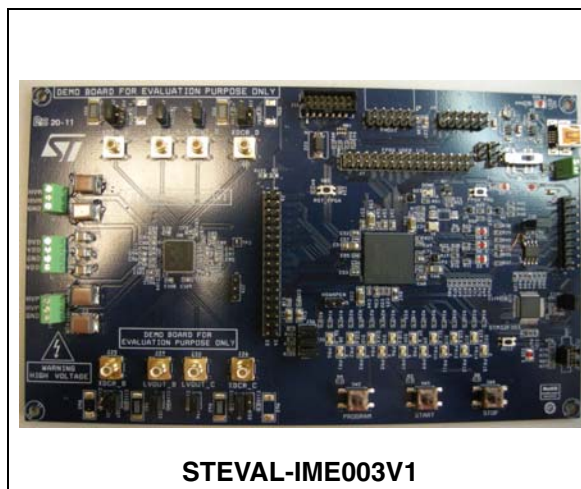
STEVAL-IME003V1

STEVAL-IME003V1 demonstration board based on the STHV748 high voltage pulser

Data brief

Features

- 4-channel outputs: high voltage and low voltage BNC connectors
- Load simulator using signal equivalent circuits
- Possibility to set up own load simulator
- 16 preset waveforms
- USB connector to connect STM32 with PC and supply power to it
- 4 MB serial Flash memory to host FPGA code and waveforms
- Memory expansion connector to add external serial Flash
- Connectors to supply high voltage and low voltage to the STHV748 output stage
- LEDs to monitor the power management stage
- Human machine interface to select, start and stop the generation of the preset waveforms
- 25 LEDs to monitor board behavior
- RoHS compliant



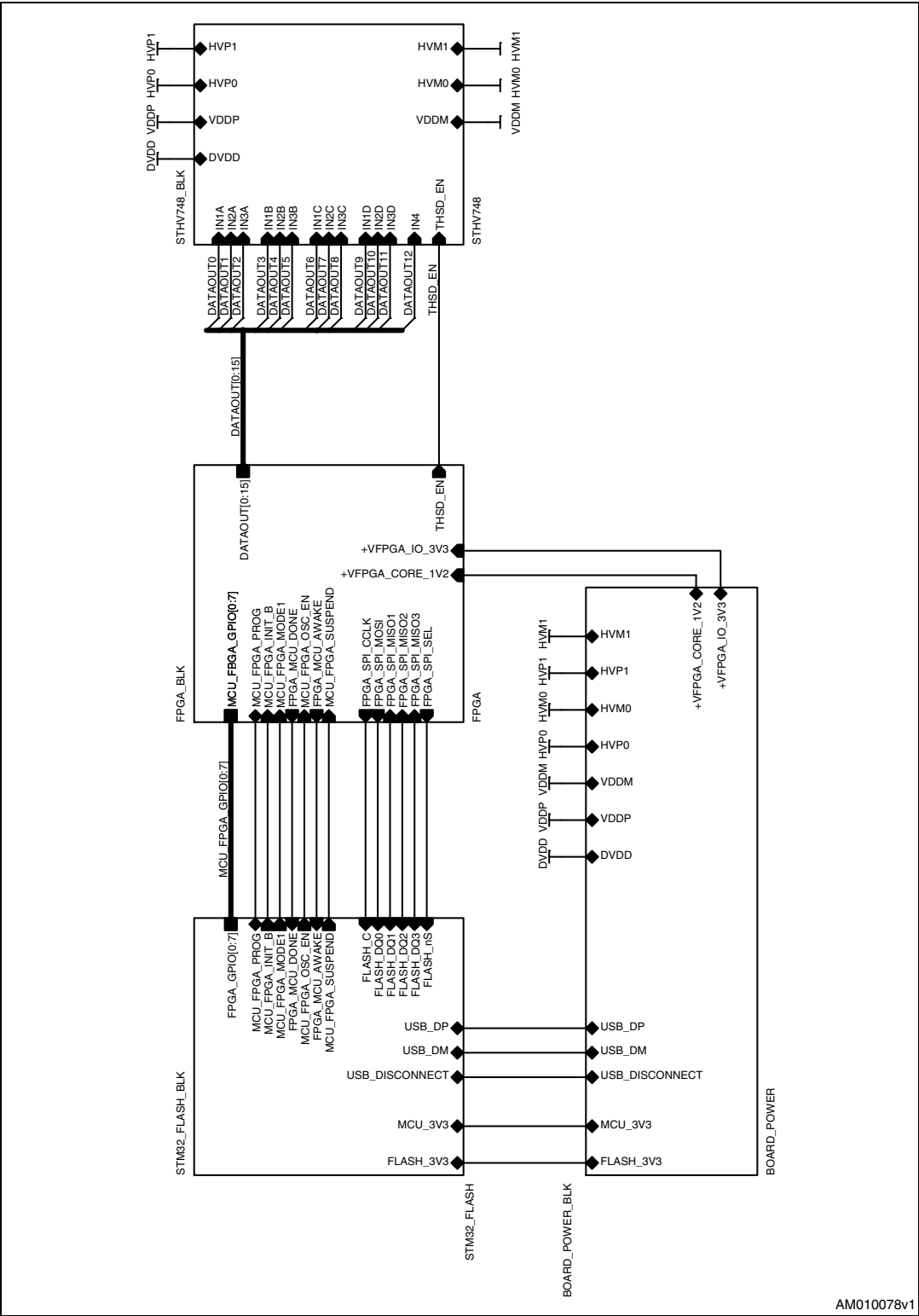
Description

The STEVAL-IME003V1 demonstration board is designed around the STHV748 4-channel high voltage pulser, a state-of-the-art device designed for ultrasound imaging applications.

The output waveforms can be displayed directly on an oscilloscope by connecting the scope probe to the relative BNCs. 16 preset waveforms are available to test the HV pulser under varying conditions.

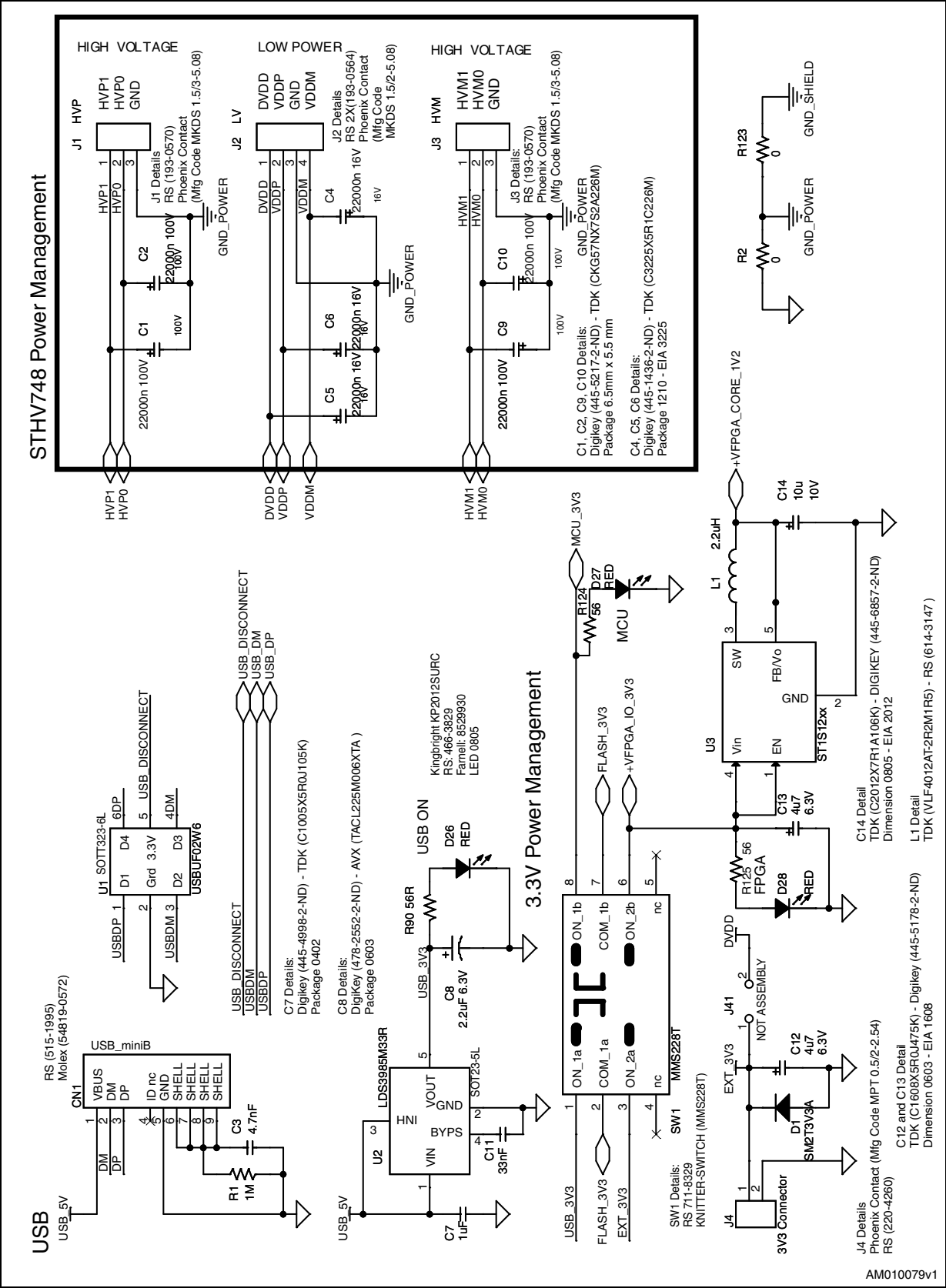
1 Schematic diagrams

Figure 1. STEVAL-IME003V1 hierarchical blocks



AM010078v1

Figure 2. STEVAL-IME003V1 FPGA bank 0 configuration



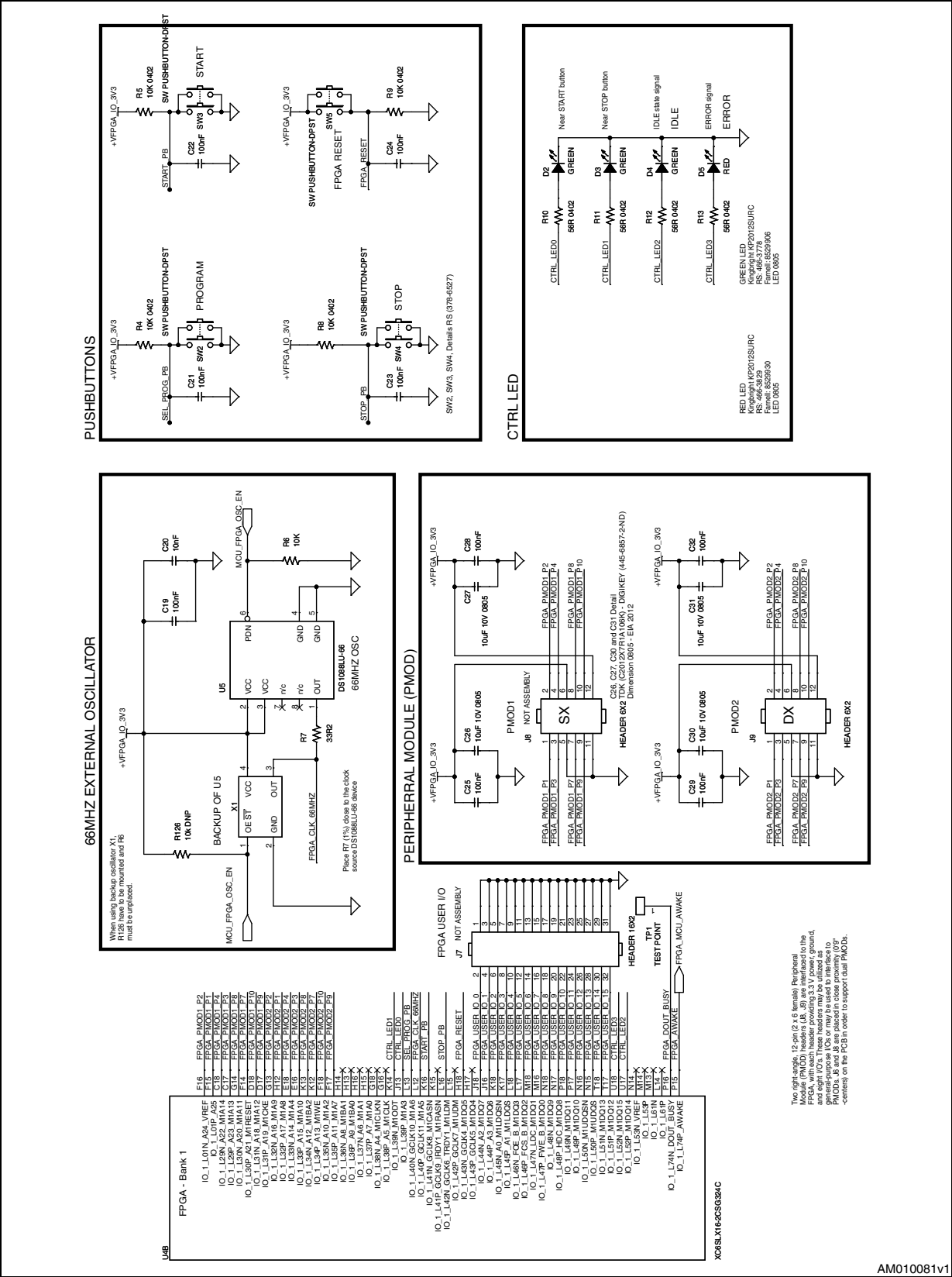
U4A

FPGA - Bank 0

IO_0_L10N_VREF
IO_0_L10P_VREF
IO_0_L02P_A2
IO_0_L02P_A3
IO_0_L03N_A2
IO_0_L03N_A3
IO_0_L04P_A4
IO_0_L04P_A5
IO_0_L06N_A5
IO_0_L06N_A6
IO_0_L07N_A7
IO_0_L07N_A8
IO_0_L08N_VREF
IO_0_L08P_VREF
IO_0_L08P_A6
IO_0_L08P_A7
IO_0_L10N_A7
IO_0_L10N_A8
IO_0_L11N_A8
IO_0_L11N_A9
IO_0_L12P_A9
IO_0_L12P_A10
IO_0_L13N_A10
IO_0_L13N_A11
IO_0_L34P_GCLK18
IO_0_L34P_GCLK19
IO_0_L35N_GCLK16
IO_0_L35N_GCLK17
IO_0_L36N_GCLK14
IO_0_L36P_GCLK15
IO_0_L37N_GCLK12
IO_0_L37N_GCLK13
IO_0_L38N_VREF
IO_0_L38P_VREF
IO_0_L38P_A11
IO_0_L38P_A12
IO_0_L39N_B11
IO_0_L39N_B12
IO_0_L40P_A12
IO_0_L41N_B12
IO_0_L41N_B13
IO_0_L42P_A13
IO_0_L42P_A14
IO_0_L47N_A13
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IO_0_L50P_A13
IO_0_L50P_A14
IO_0_L51N_A14
IO_0_L51N_A15
IO_0_L10N_VREF
IO_0_L02P_A13
IO_0_L03N_A13
IO_0_L04P_A15
IO_0_L04P_A16
IO_0_L06N_A16
IO_0_L06N_A17
IO_0_L06P_A17
IO_0_L06P_A18

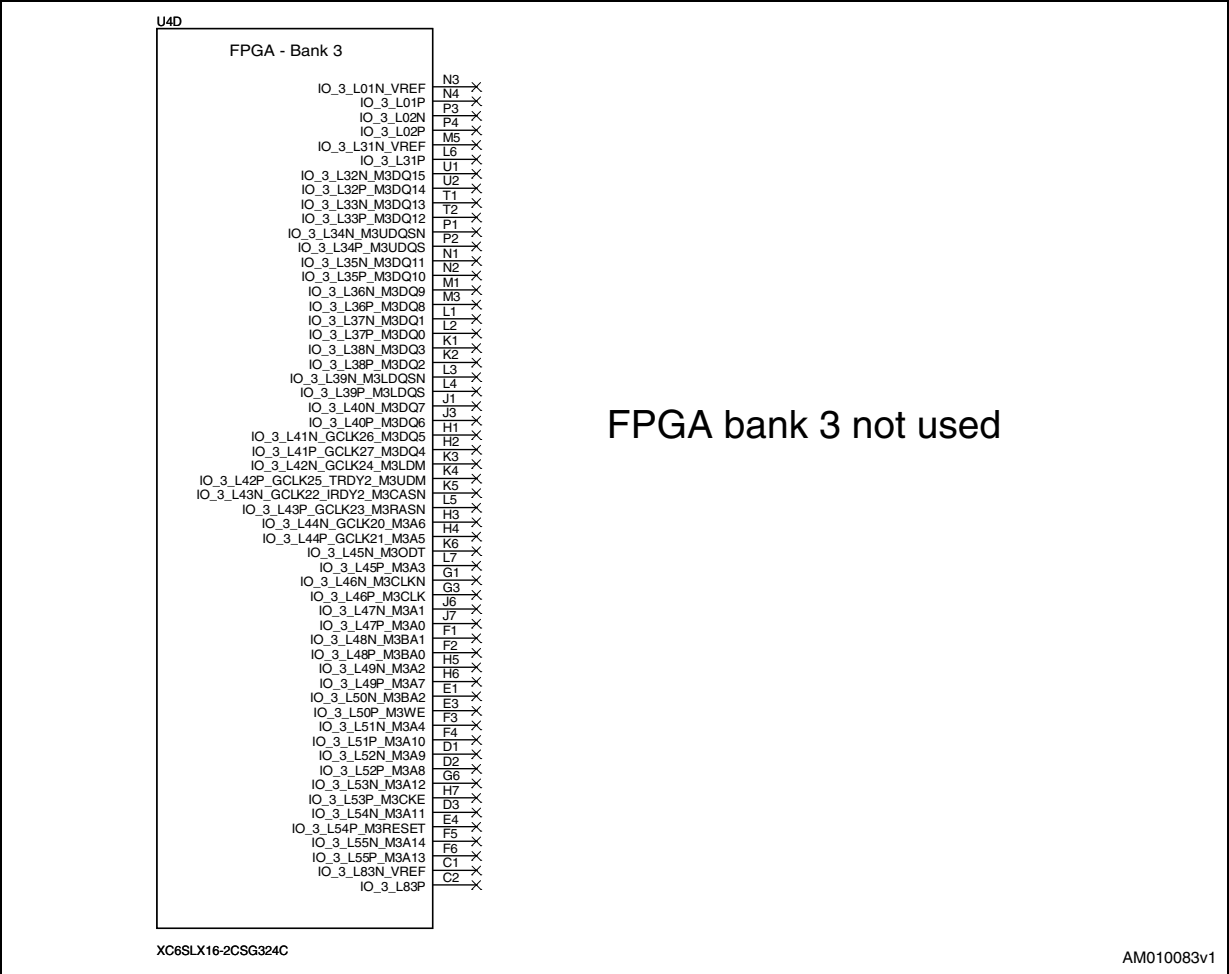
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Figure 4. STEVAL-IME003V1 FPGA bank 2 configuration



[illegible]

Figure 6. STEVAL-IME003V1 FPGA bank 3 configuration

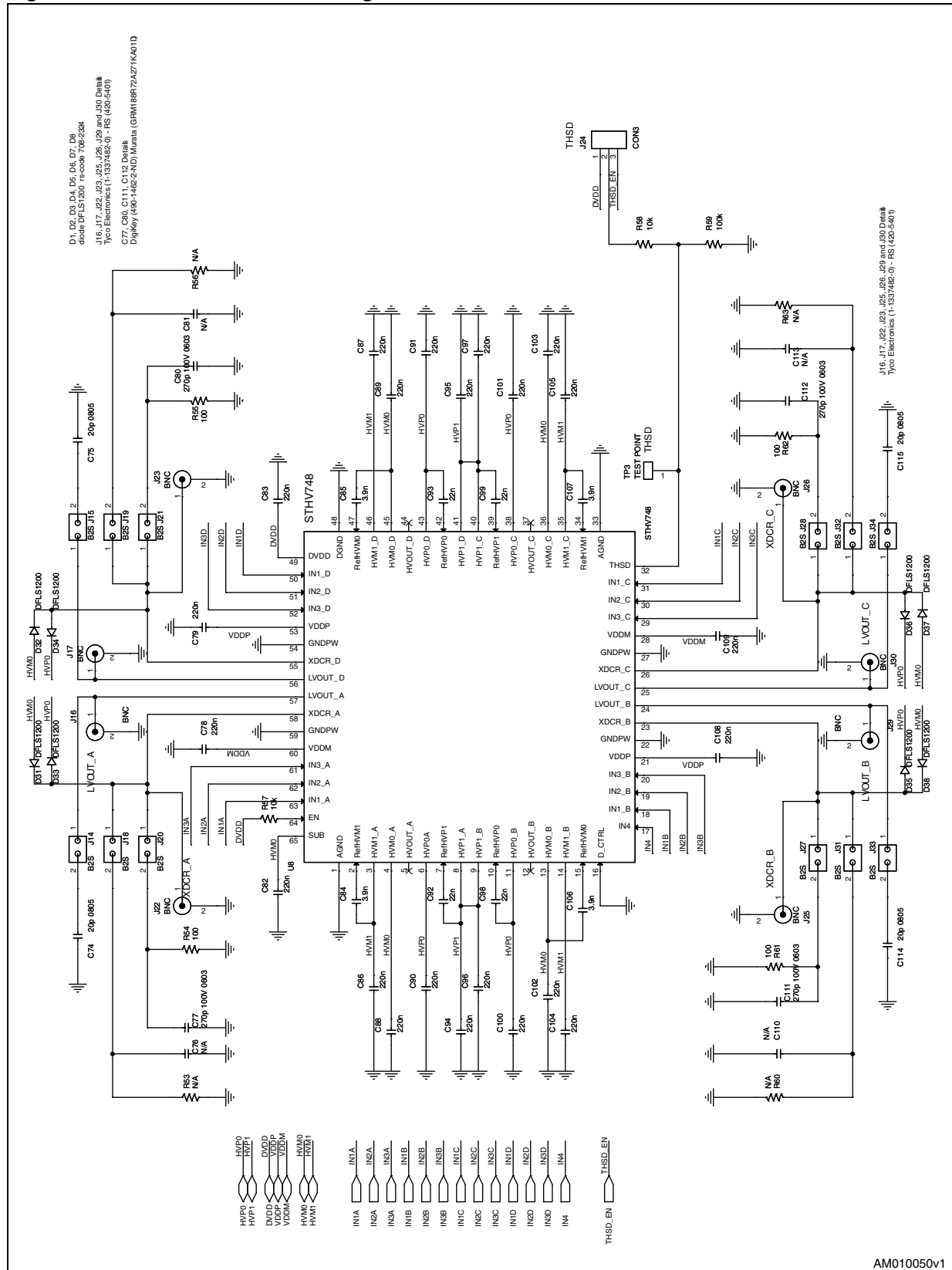


The schematic diagram illustrates the electrical connections for the Xilinx Zynq-7010 evaluation board, organized into four main functional blocks:

- FPGA JTAG:** This section shows the JTAG interface. It includes a 4-pin header (J1) connected to a 4-wire resistor array (R1) and a 4-wire resistor array (R2). The JTAG signals are connected to the JTAG pins of the Zynq-7010 (J1, J2, J3, J4).
- SUSPEND & CMPCS_B:** This section shows the suspend and power management logic. It includes a 74V133CTR (U6) configured as a monostable multivibrator, triggered by a 10K 0402 resistor (R4) connected to the FPGA suspend pin. The output of U6 is connected to the CMPCS_B pin of the Zynq-7010.
- PROGRAM_B:** This section shows the programming logic. It includes a 74V133CTR (U7) configured as a monostable multivibrator, triggered by a 10K 0402 resistor (R5) connected to the FPGA programming pin. The output of U7 is connected to the PROGRAM_B pin of the Zynq-7010.
- Power & Configuration:** This section shows the power and configuration logic. It includes a 74V133CTR (U8) configured as a monostable multivibrator, triggered by a 10K 0402 resistor (R6) connected to the FPGA power pin. The output of U8 is connected to the VCCAUX pin of the Zynq-7010.

The diagram also shows the connection of the Zynq-7010 to the external components, including the 4-wire resistor array (R1), the 4-wire resistor array (R2), the 74V133CTR (U6), the 74V133CTR (U7), the 74V133CTR (U8), and the 10K 0402 resistors (R4, R5, R6).

Figure 8. STEVAL-IME003V1 configuration of the STHV748



Use USB for reconfigurable power for SPI flash devices.
USB must be open when using external SPI flash devices on connecto J10. Default value closed.

SPI FLASH

FLASH_3V3

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2 Revision history

Table 1. Document revision history

| Date | Revision | Changes |
|-------------|-----------------|------------------|
| 11-Aug-2011 | 1 | Initial release. |

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