Data Sheet | November 20, 2006 | FN3281.10

Monolithic, Quad SPST, CMOS Analog Switches

The DG441 and DG442 monolithic CMOS analog switches are drop-in replacements for the popular DG201A and DG202 series devices. They include four independent single pole single throw (SPST) analog switches, TTL and CMOS compatible digital inputs, and a voltage reference for logic thresholds.

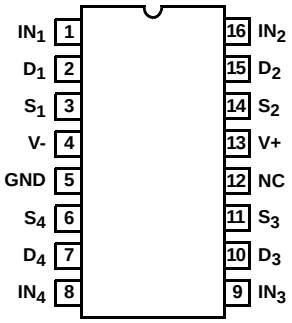
These switches feature lower analog ON resistance (<85Ω) and faster switch time (t_{ON} <250ns) compared to the DG201A and DG202. Charge injection has been reduced, simplifying sample and hold applications.

The improvements in the DG441 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling $40V_{P-P}$ signals. Power supplies may be single ended from +5V to +34V, symmetrical supplies from ±5V to ±22V or asymmetrical supplies limited to a maximum differential voltage of 44V with a V+ max of 34V or a V- max of -25V.

The four switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±5V analog input range. The switches in the DG441 and DG442 are identical, differing only in the polarity of the selection logic.

Pinout

DG441, DG442
(16 LD PDIP, SOIC, TSSOP)
TOP VIEW



Features

- ON Resistance (Max) 85Ω
- Low Power Consumption (P_D) . . . . . <1.6mW
- Fast Switching Action
  - t_{ON} (Max) 250ns
  - t_{OFF} (Max, DG441) 120ns
- Low Charge Injection
- Upgrade from DG201A, DG202
- TTL, CMOS Compatible
- Single or Split Supply Operation
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Audio Switching
- Battery Operated Systems
- Data Acquisition
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Automatic Test Equipment

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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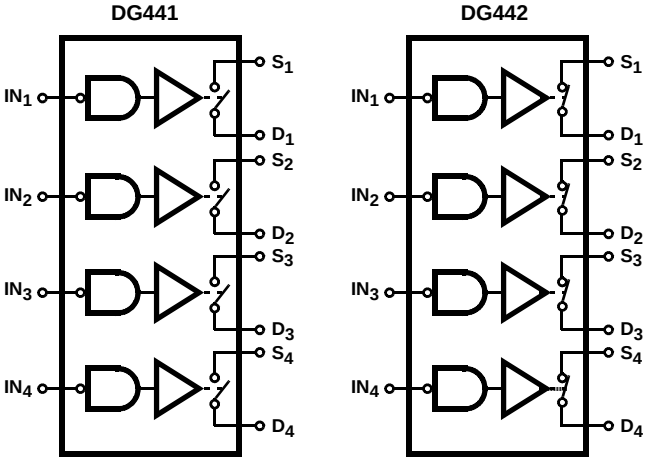
Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
DG441DJ	DG441DJ	-40 to +85	16 Ld PDIP	E16.3
DG441DJZ (Note)	DG441DJZ	-40 to +85	16 Ld PDIP* (Pb-free)	E16.3
DG441DY	DG441DY	-40 to +85	16 Ld SOIC	M16.15
DG441DY-T	DG441DY	16 Ld SOIC Tape and Reel		M16.15
DG441DYZ (Note)	DG441DYZ	-40 to +85	16 Ld SOIC (Pb-free)	M16.15
DG441DYZ-T (Note)	DG441DYZ	16 Ld SOIC Tape and Reel (Pb-free)		M16.15
DG441DYZA (Note)	DG441DYZ	-40 to +85	16 Ld SOIC (Pb-free)	M16.15
DG441DYZA-T (Note)	DG441DYZ	16 Ld SOIC Tape and Reel (Pb-free)		M16.15
DG441DVZ (Note)	DG441DVZ	-40 to +85	16 Ld TSSOP (Pb-free)	M16.173
DG441DVZ-T (Note)	DG441DVZ	-40 to +85	16 Ld TSSOP Tape and Reel (Pb-free)	M16.173
DG442DJ	DG442DJ	-40 to +85	16 Ld PDIP	E16.3
DG442DJZ (Note)	DG442DJZ	-40 to +85	16 Ld PDIP* (Pb-free)	E16.3
DG442DY	DG442DY	-40 to +85	16 Ld SOIC	M16.15
DG442DY-T	DG442DY	16 Ld SOIC Tape and Reel		M16.15
DG442DYZ (Note)	DG442DYZ	-40 to +85	16 Ld SOIC (Pb-free)	M16.15
DG442DYZ-T (Note)	DG442DYZ	16 Ld SOIC Tape and Reel (Pb-free)		M16.15
DG442DVZ (Note)	DG442DVZ	-40 to +85	16 Ld TSSOP (Pb-free)	M16.173
DG442DVZ-T (Note)	DG442DVZ	16 Ld TSSOP Tape and Reel (Pb-free)		M16.173

***Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.**

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Functional Diagrams

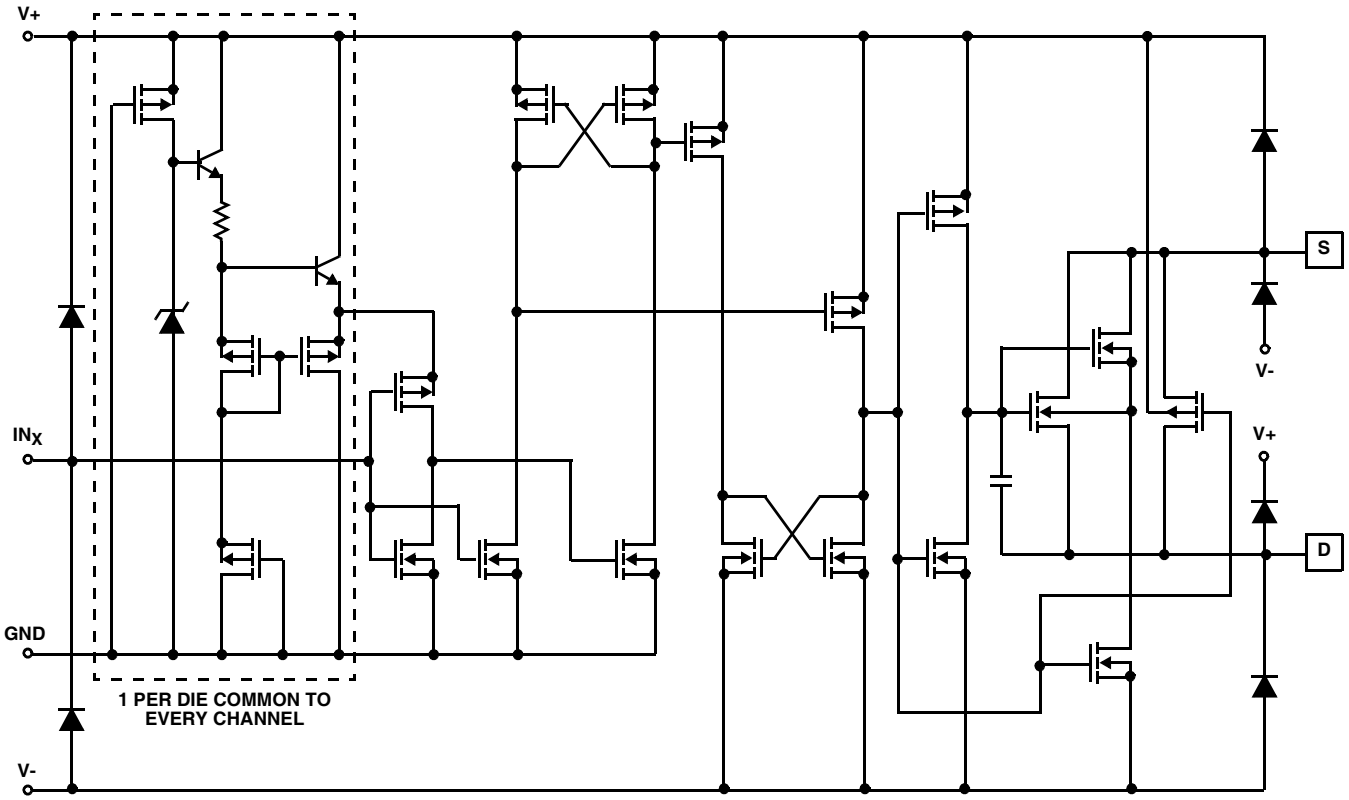


SWITCHES SHOWN FOR LOGIC "1" INPUT

TRUTH TABLE

LOGIC	V_{IN}	DG441	DG442
0	≤0.8V	ON	OFF
1	≥2.4V	OFF	ON

Schematic Diagram (One Channel)



Pin Descriptions

PIN	SYMBOL	DESCRIPTION
1	IN_1	Logic Control for Switch 1
2	D_1	Drain (Output) Terminal for Switch 1
3	S_1	Source (Input) Terminal for Switch 1
4	V-	Negative Power Supply Terminal
5	GND	Ground Terminal (Logic Common)
6	S_4	Source (Input) Terminal for Switch 4
7	D_4	Drain (Output) Terminal for Switch 4
8	IN_4	Logic Control for Switch 4
9	IN_3	Logic Control for Switch 3
10	D_3	Drain (Output) Terminal for Switch 3
11	S_3	Source (Input) Terminal for Switch 3
12	NC	No Internal Connection
13	V+	Positive Power Supply Terminal (Substrate)
14	S_2	Source (Input) Terminal for Switch 2
15	D_2	Drain (Output) Terminal for Switch 2
16	IN_2	Logic Control for Switch 2

Absolute Maximum Ratings

V+ to V- 44.0V
GND to V-. . . . . -25V
GND to V+ . . . . . +34V
Digital Inputs, V_S, V_D (Note 1)
. . . . . (V-) -2V to (V+) + 2V or 30mA, Whichever Occurs First
Continuous Current (Any Terminal) 30mA
Peak Current, S or D (Pulsed 1ms, 10% Duty Cycle Max) . . 100mA

Operating Conditions

Temperature Range . . . . . -40°C to +85°C
Signal Voltage Range . . . . . ±20V (Max)
Input Low Voltage . . . . . 0.8V (Max)
Input High Voltage . . . . . 2.4V (Min)
Input Rise and Fall Time . . . . . ≤20ns

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
PDIP Package*	90
SOIC Package	115
TSSOP Package	150

Maximum Junction Temperature (Plastic Packages) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C
(SOIC and TSSOP- Lead Tips Only)

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Signals on S_X, D_X or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

(Dual Supply) Test Conditions: V+ = +15V, V- = -15V, V_{IN} = 2.4V, 0.8V, $V_{ANALOG} = V_S, V_D$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN	(NOTE 3) TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	R_L = 1kΩ, C_L = 35pF, V_S = ±10V, (Figure 1)	+25	-	150	250	ns
Turn-OFF Time, t_{OFF}						
DG441		+25	-	90	120	ns
DG442			-	110	210	ns
Charge Injection, Q (Figure 2)	C_L = 1nF, V_G = 0V, R_G = 0Ω	+25	-	-1	-	pC
OFF Isolation (Figure 4)	R_L = 50Ω, C_L = 5pF, f = 1MHz	+25	-	60	-	dB
Crosstalk (Channel-to-Channel) (Figure 3)		+25	-	-100	-	dB
Source OFF Capacitance, $C_{S(OFF)}$	f = 1MHz, V_{ANALOG} = 0 (Figure 5)	+25	-	4	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$		+25	-	4	-	pF
Channel ON Capacitance, $C_{D(ON)} + C_{S(ON)}$		+25	-	16	-	pF
DIGITAL INPUT CHARACTERISTICS						
Input Current V_{IN} Low, I_{IL}	V_{IN} Under Test = 0.8V, All Others = 2.4V	Full	-0.5	-0.00001	0.5	µA
Input Current V_{IN} High, I_{IH}	V_{IN} Under Test = 2.4V, All Others = 0.8V	Full	-0.5	0.00001	0.5	µA
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	-15	-	15	V
Drain-Source ON Resistance, $r_{DS(ON)}$	I_S = ∓10mA, V_D = ±8.5V, V+ = 13.5V, V- = -13.5V	+25	-	50	85	Ω
		+85	-	-	100	Ω
Source OFF Leakage Current, $I_{S(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	+25	-0.5	0.01	0.5	nA
		+85	-5	-	5	nA
Drain OFF Leakage Current, $I_{D(OFF)}$		+25	-0.5	0.01	0.5	nA
		+85	-5	-	5	nA
Channel ON Leakage Current, $I_{D(ON)} + I_{S(ON)}$	V+ = 16.5V, V- = -16.5V, $V_S = V_D$ = ±15.5V	+25	-0.5	0.08	0.5	nA
		+85	-10	-	10	nA

Electrical Specifications (Dual Supply) Test Conditions: V+ = +15V, V- = -15V, V_{IN} = 2.4V, 0.8V, V_{ANALOG} = V_S, V_D, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN	(NOTE 3) TYP	MAX	UNITS
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	Full	-	15	100	µA
Negative Supply Current, I-		+25	-1	-0.0001	-	µA
		Full	-5	-	-	µA
Ground Current, I_{GND}		Full	-100	-15	-	µA

Electrical Specifications (Single Supply) Test Conditions: V+ = 12V, V- = 0V, V_{IN} = 2.4V, 0.8V, Unless Otherwise Specified

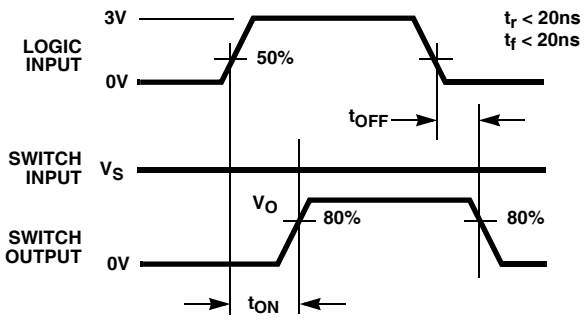
PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN	(NOTE 3) TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	R_L = 1kΩ, C_L = 35pF, V_S = 8V, (Figure 1)	+25	-	300	450	ns
Turn-OFF Time, t_{OFF}		+25	-	60	200	ns
Charge Injection, Q (Figure 2)	C_L = 1nF, V_G = 6V, R_G = 0Ω	+25	-	2	-	pC
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	12	V
Drain-Source ON Resistance, $r_{DS(ON)}$	I_S = 10mA, V_D = 3V, 8V V+ = 10.8V	+25	-	100	160	Ω
		Full	-	-	200	Ω
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 13.2V, V- = 0V, V_{IN} = 0V or 5V	Full	-	15	100	µA
Negative Supply Current, I-		+25	-1	-0.0001	-	µA
		Full	-100	-0.0001	-	µA
Ground Current, I_{GND}		Full	-100	-15	-	µA

NOTES:

3. Typical values are for DESIGN AID ONLY, not guaranteed nor production tested.

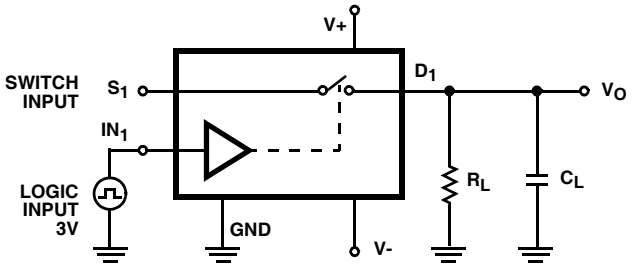
Test Circuits and Waveforms

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



NOTE: Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS



Repeat test for Channels 2, 3 and 4.
For load conditions, see Specifications. C_L includes fixture and stray capacitance.

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

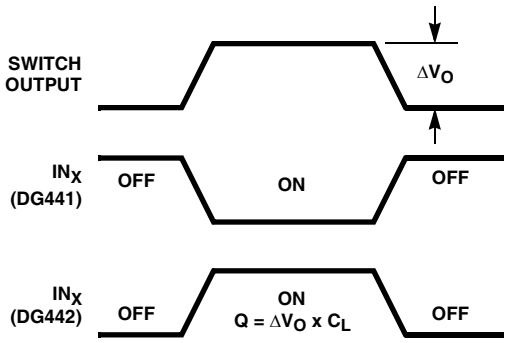


FIGURE 2A. MEASUREMENT POINTS

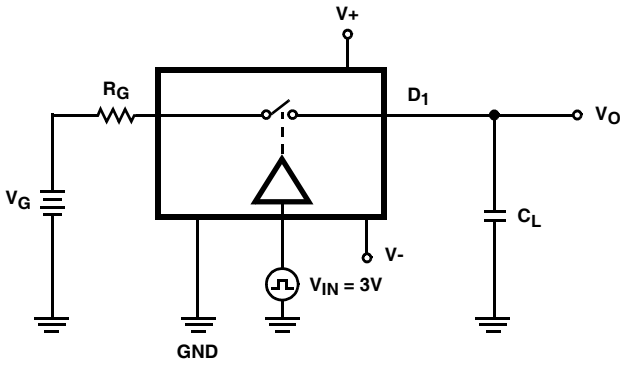


FIGURE 2B. TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

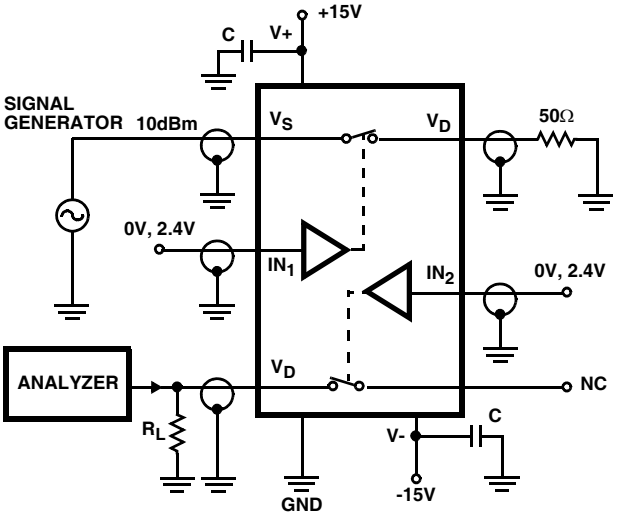


FIGURE 3. CROSSTALK TEST CIRCUIT

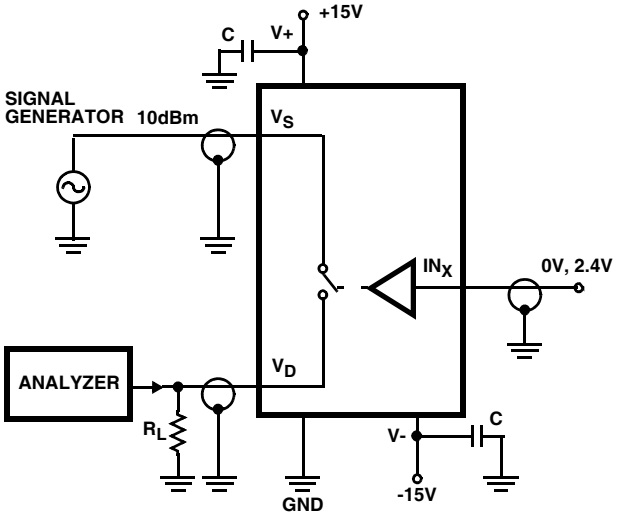


FIGURE 4. OFF ISOLATION TEST CIRCUIT

Test Circuits and Waveforms (Continued)

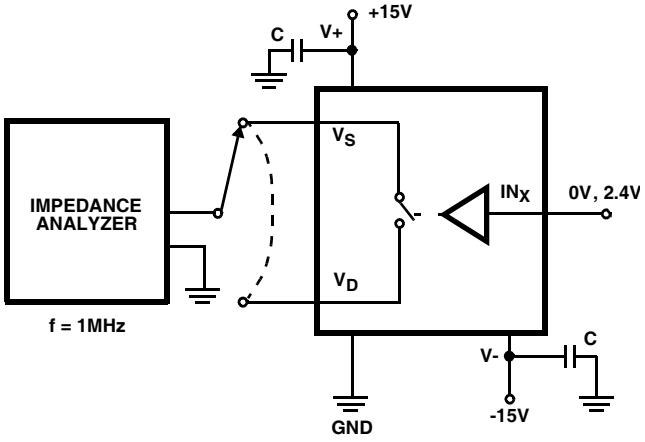
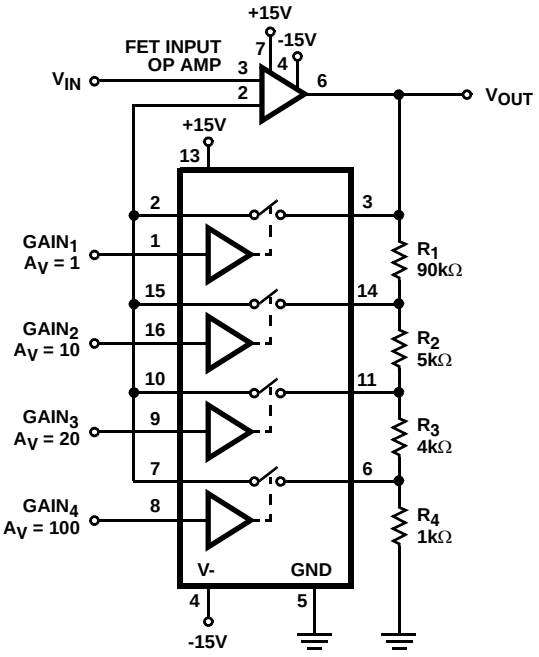


FIGURE 5. SOURCE/DRAIN CAPACITANCES TEST CIRCUIT

Application Information

GAIN ERROR IS DETERMINED ONLY BY THE RESISTOR TOLERANCE.
OP AMP OFFSET AND CMRR WILL LIMIT ACCURACY OF CIRCUIT.



$$\frac{V_{OUT}}{V_{IN}} = \frac{R_1 + R_2 + R_3 + R_4}{R_4} = 100 \text{ with } SW_4 \text{ closed}$$

FIGURE 6. PRECISION WEIGHTED RESISTOR PROGRAMMABLE GAIN AMPLIFIER

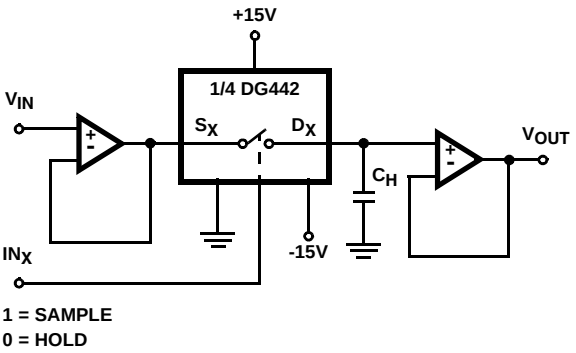


FIGURE 7. OPEN LOOP SAMPLE AND HOLD

Typical Performance Curves

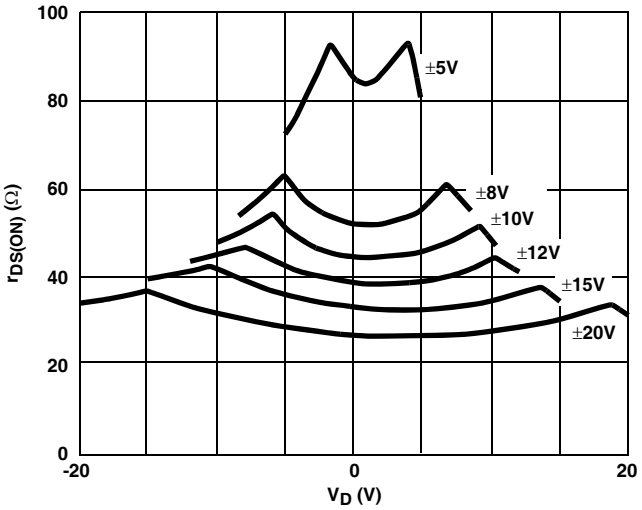


FIGURE 8. $r_{DS(ON)}$ vs V_D AND POWER SUPPLY VOLTAGE

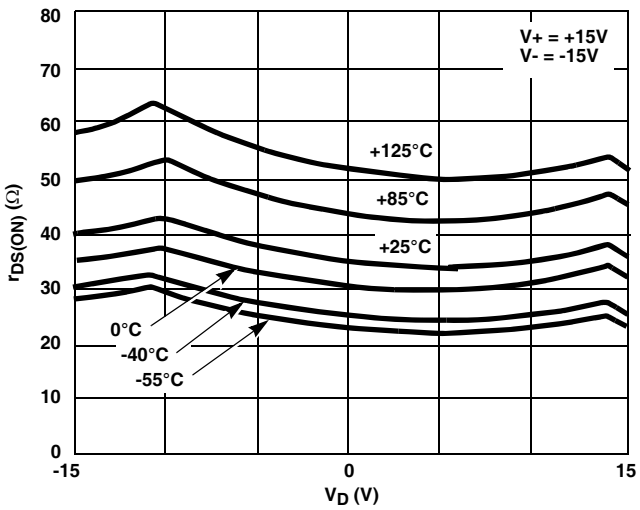


FIGURE 9. $r_{DS(ON)}$ vs V_D AND TEMPERATURE

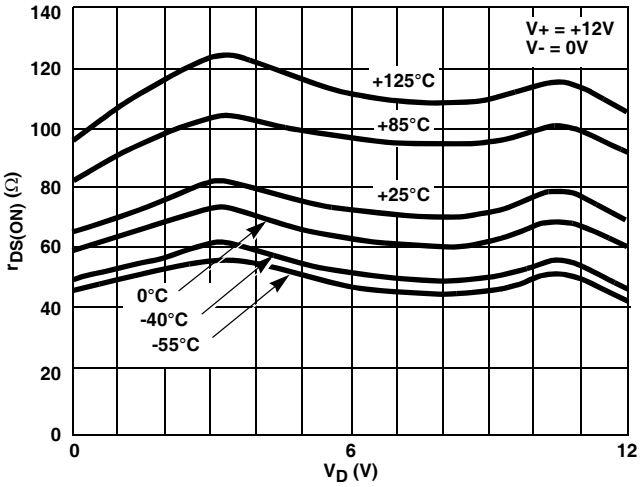


FIGURE 10. $r_{DS(ON)}$ vs V_D AND TEMPERATURE (SINGLE 12V SUPPLY)

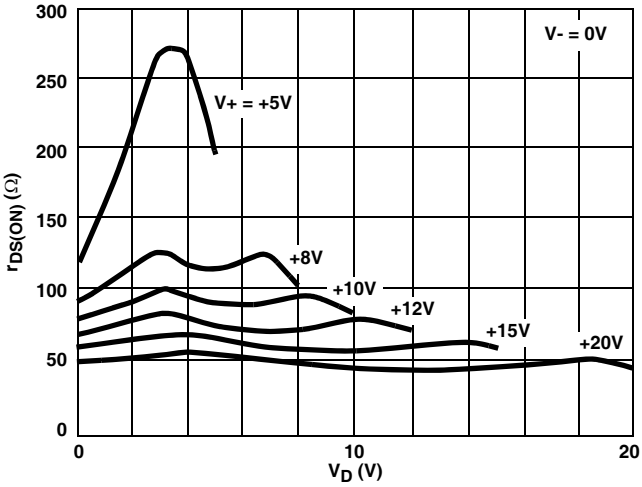


FIGURE 11. $r_{DS(ON)}$ vs V_D AND SINGLE SUPPLY VOLTAGE

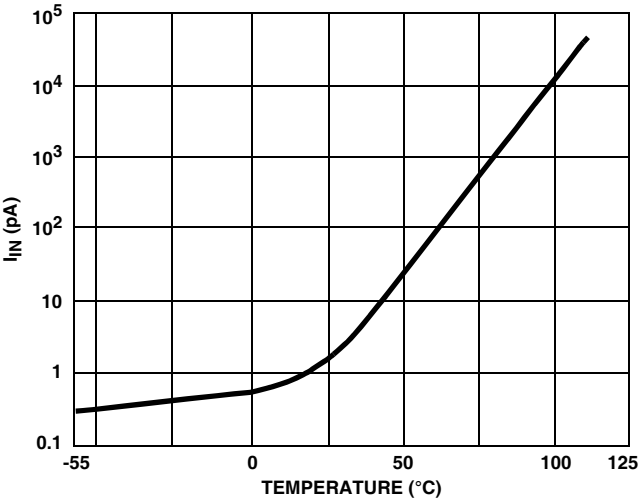


FIGURE 12. INPUT CURRENT vs TEMPERATURE

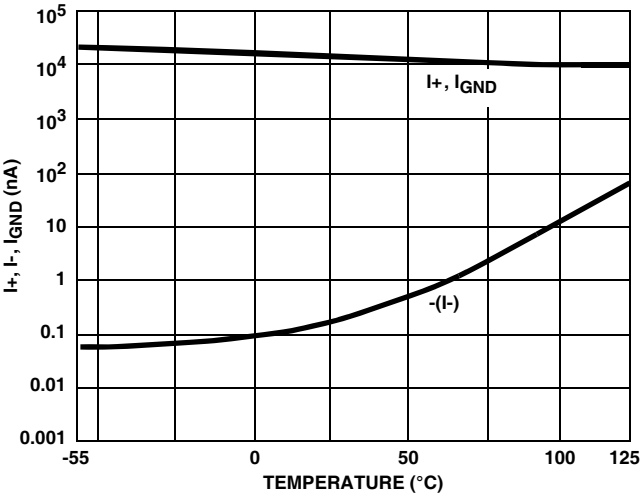


FIGURE 13. SUPPLY CURRENT vs TEMPERATURE

Typical Performance Curves (Continued)

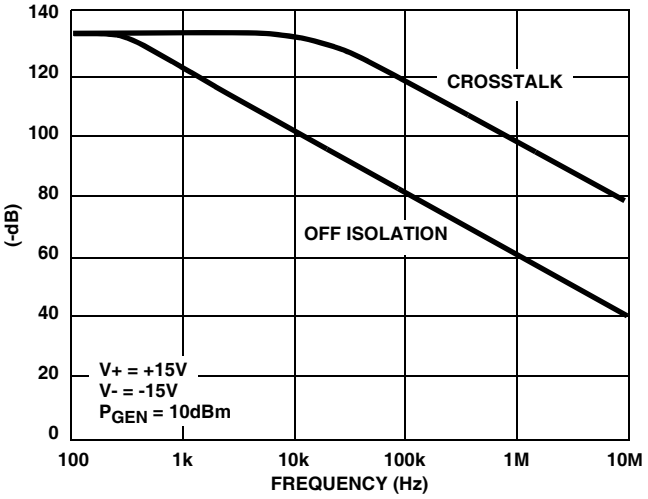


FIGURE 14. CROSSTALK AND OFF ISOLATION vs FREQUENCY

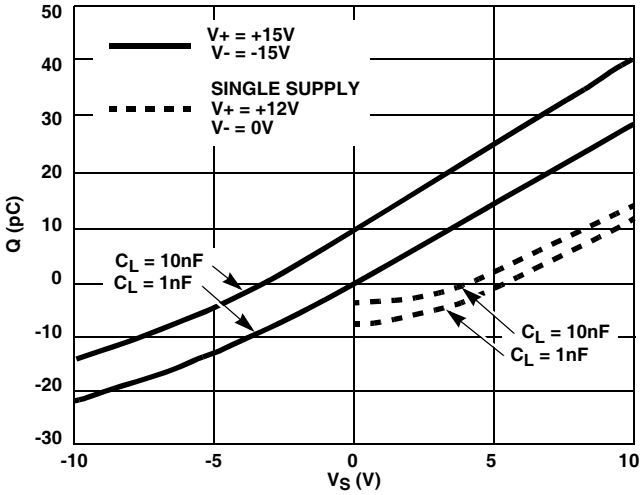


FIGURE 15. CHARGE INJECTION vs SOURCE VOLTAGE

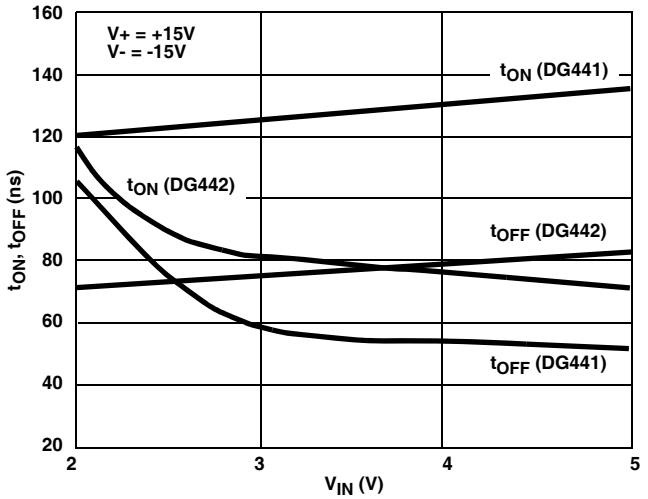


FIGURE 16. SWITCHING TIMES vs INPUT VOLTAGE

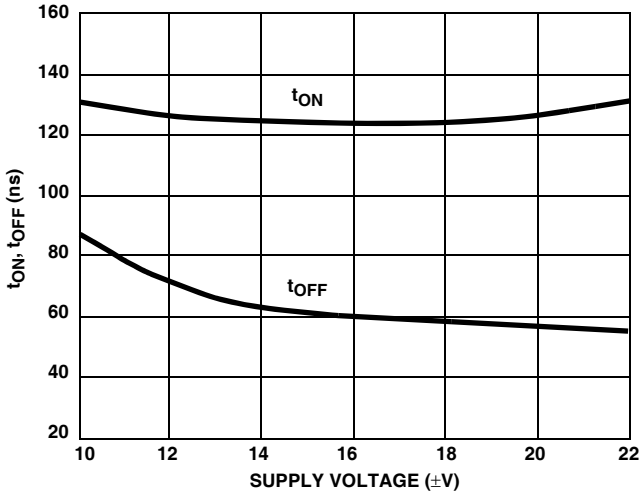


FIGURE 17. SWITCHING TIME vs POWER SUPPLY VOLTAGE (DG441)

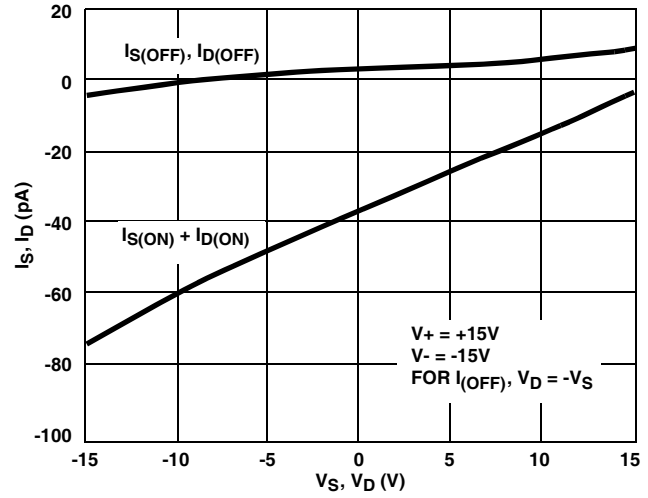


FIGURE 18. LEAKAGE CURRENT vs ANALOG VOLTAGE

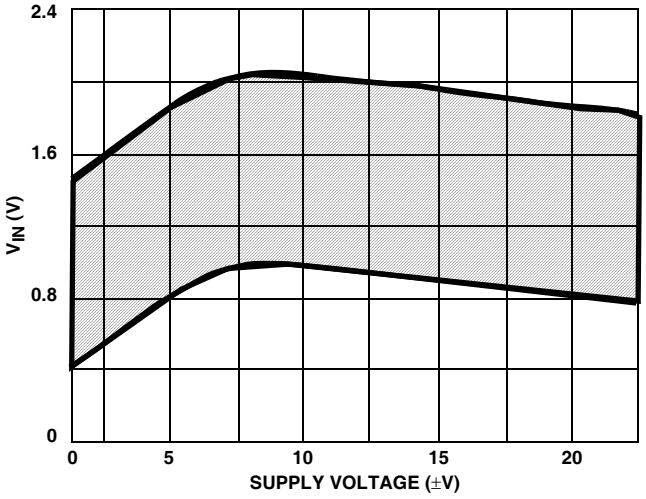


FIGURE 19. SWITCHING THRESHOLD vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

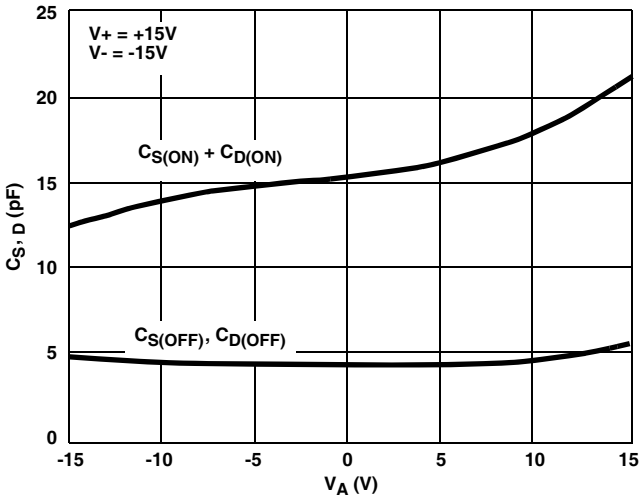


FIGURE 20. SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE

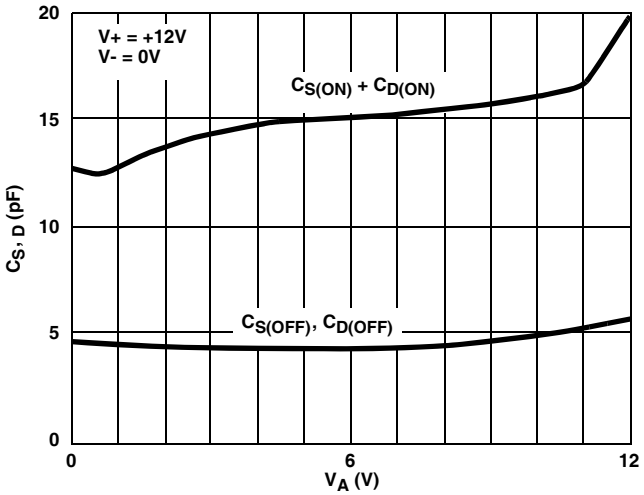


FIGURE 21. SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE (SINGLE 12V SUPPLY)

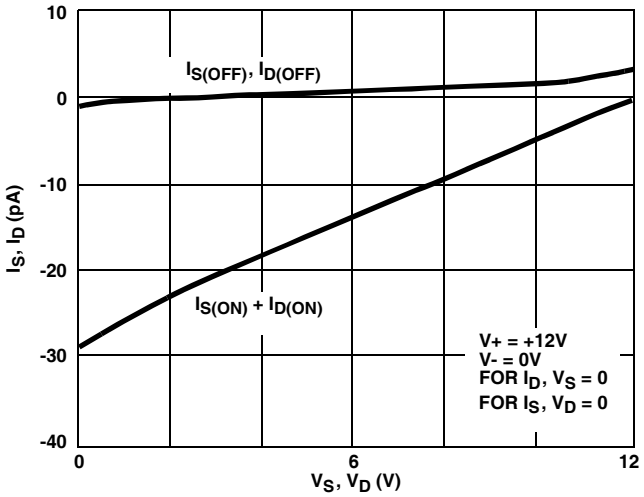


FIGURE 22. SOURCE/DRAIN LEAKAGE CURRENTS (SINGLE 12V SUPPLY)

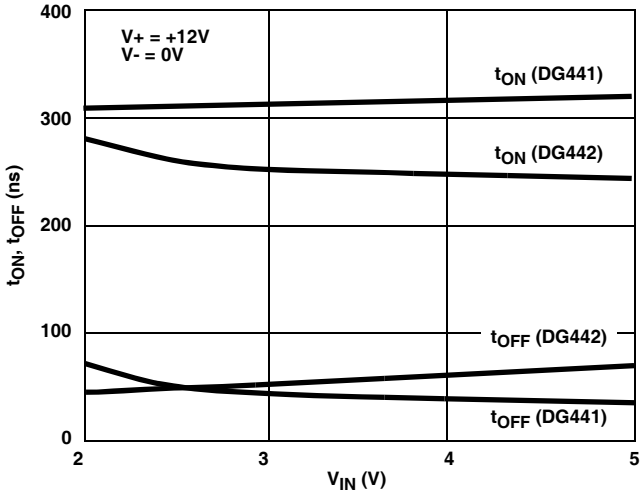


FIGURE 23. SWITCHING TIME vs INPUT VOLTAGE (SINGLE 12V SUPPLY)

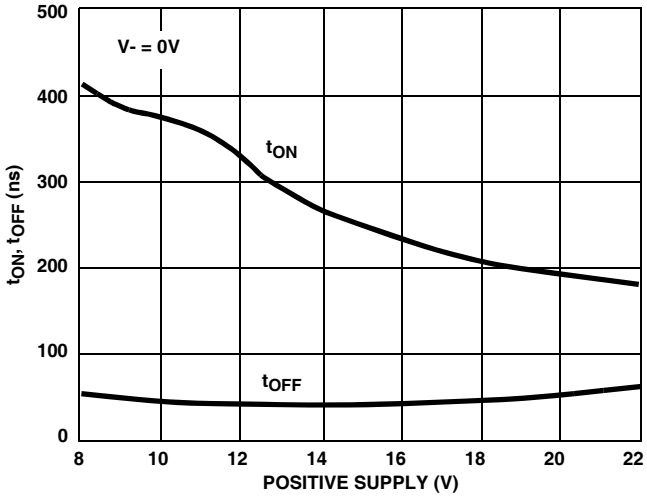


FIGURE 24. SWITCHING TIME vs SINGLE SUPPLY VOLTAGE (DG441)

Die Characteristics

DIE DIMENSIONS:

2160µm x 1760µm x 485µm

METALLIZATION:

Type: SiAl
Thickness: 12kÅ ±1kÅ

PASSIVATION:

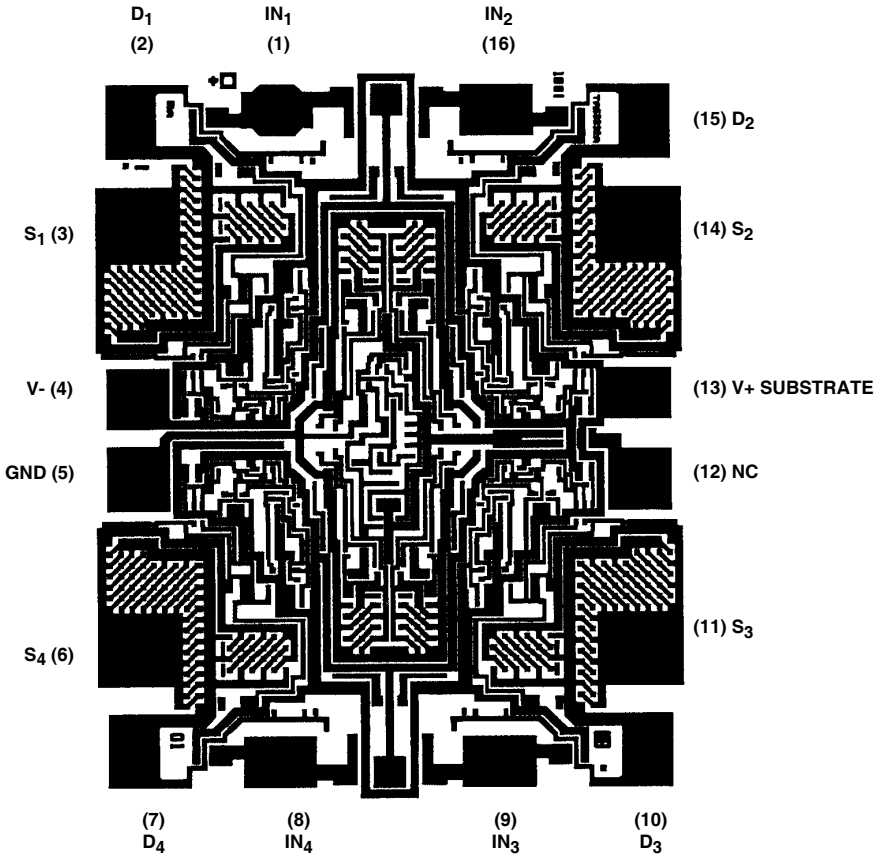
Type: Nitride
Thickness: 8kÅ ±1kÅ

WORST CASE CURRENT DENSITY:

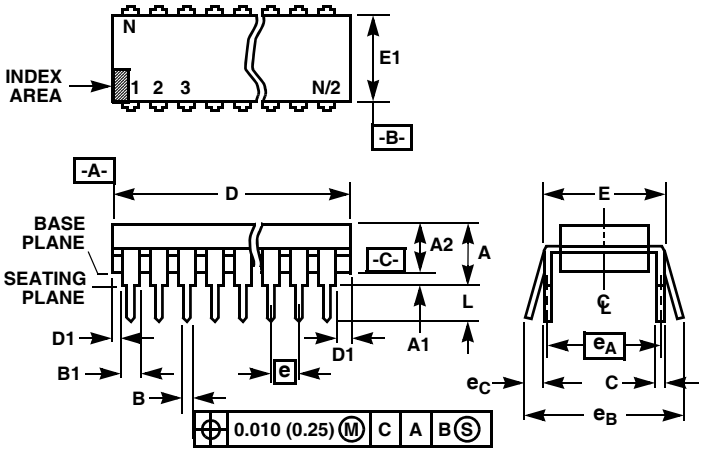
9.1×10^4 A/cm^2

Metallization Mask Layout

DG441, DG442



Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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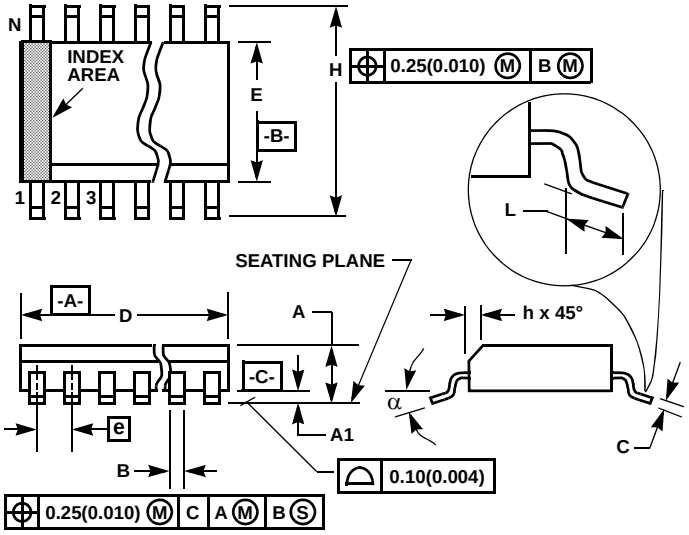
Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

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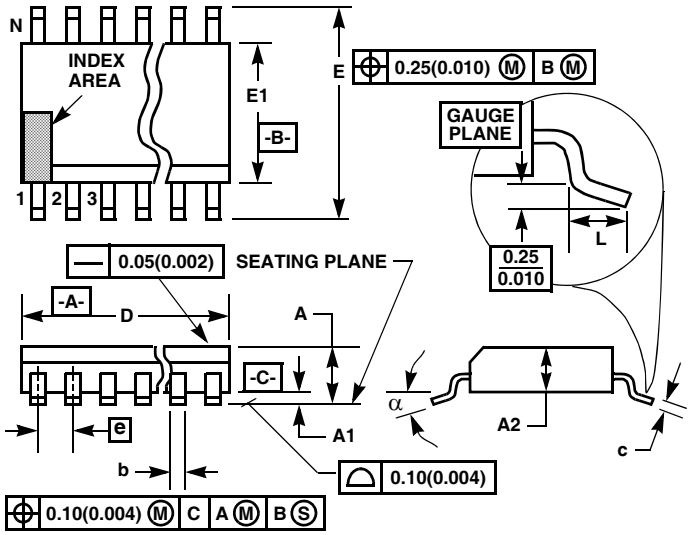
Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AB, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

M16.173

16 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.043	-	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.033	0.037	0.85	0.95	-
b	0.0075	0.012	0.19	0.30	9
c	0.0035	0.008	0.09	0.20	-
D	0.193	0.201	4.90	5.10	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.020	0.028	0.50	0.70	6
N	16		16		7
α	0^o	8^o	0^o	8^o	-

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