

SIPMOS® Power-Transistor

Feature

- P-channel
- Enhancement mode
- Logic Level
- 175°C operating temperature
- Avalanche rated
- dv/dt rated
- Pb-free lead plating; RoHS compliant
- ° Qualified according to AEC Q101

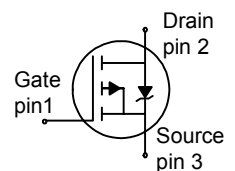
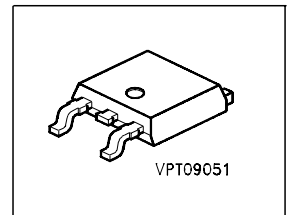


Type	Package	Lead free
SPD09P06PL G	PG-TO252-3	Yes

Product Summary

V_{DS}	-60	V
$R_{DS(on)}$	0.25	Ω
I_D	-9.7	A

PG-TO252-3



Maximum Ratings, at $T_j = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Value	Unit
Continuous drain current	I_D	-9.7	A
$T_C=25^\circ\text{C}$		-6.8	
$T_C=100^\circ\text{C}$			
Pulsed drain current	$I_{D \text{ puls}}$	-38.8	
$T_C=25^\circ\text{C}$			
Avalanche energy, single pulse	E_{AS}	70	mJ
$I_D=-9.7 \text{ A}$, $V_{DD}=-25\text{V}$, $R_{GS}=25\Omega$			
Avalanche energy, periodic limited by T_{jmax}	E_{AR}	4.2	
Reverse diode dv/dt	dv/dt	6	kV/ μs
$I_S=-9.7\text{A}$, $V_{DS}=-48$, $di/dt=200\text{A}/\mu\text{s}$, $T_{jmax}=175^\circ\text{C}$			
Gate source voltage	V_{GS}	± 20	V
Power dissipation	P_{tot}	42	W
$T_C=25^\circ\text{C}$			
Operating and storage temperature	T_j, T_{stg}	-55... +175	$^\circ\text{C}$
IEC climatic category; DIN IEC 68-1		55/175/56	

Thermal Characteristics

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Characteristics					
Thermal resistance, junction - case	R_{thJC}	-	-	3.6	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}	-	-	100	
SMD version, device on PCB:	R_{thJA}				
@ min. footprint		-	-	75	
@ 6 cm ² cooling area ¹⁾		-	-	50	

Electrical Characteristics, at $T_j = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static Characteristics					
Drain-source breakdown voltage $V_{GS}=0V, I_D=-250\mu A$	$V_{(BR)DSS}$	-60	-	-	V
Gate threshold voltage, $V_{GS} = V_{DS}$ $I_D=-250\mu A$	$V_{GS(th)}$	-1	-1.5	-2	
Zero gate voltage drain current $V_{DS}=-60V, V_{GS}=0V, T_j=25^{\circ}C$ $V_{DS}=-60V, V_{GS}=0V, T_j=150^{\circ}C$	I_{DSS}	- -	-0.1 -10	-1 -100	μA
Gate-source leakage current $V_{GS}=-20V, V_{DS}=0V$	I_{GSS}	-	-10	-100	
Drain-source on-state resistance $V_{GS}=-4.5V, I_D=-5.4A$	$R_{DS(on)}$	-	0.3	0.4	Ω
Drain-source on-state resistance $V_{GS}=-10V, I_D=-6.8A$	$R_{DS(on)}$	-	0.2	0.25	

¹Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical without blown air.

Electrical Characteristics, at $T_j = 25\text{ }^{\circ}\text{C}$, unless otherwise specified

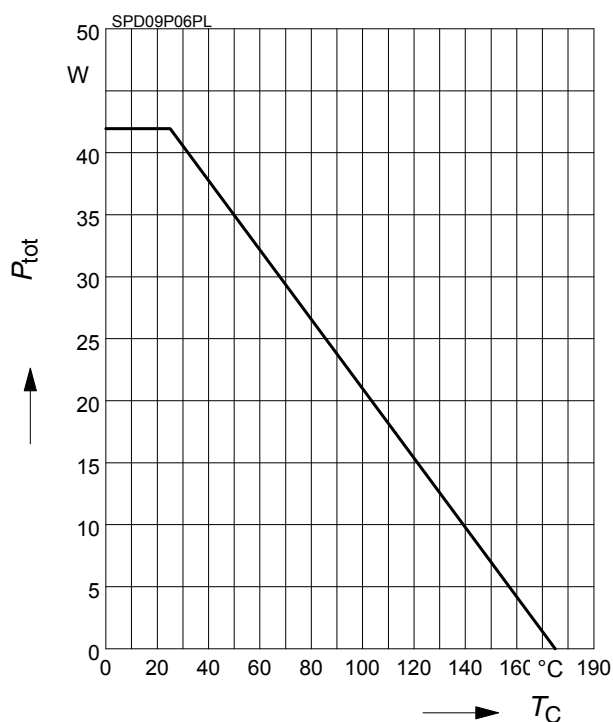
Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic Characteristics						
Transconductance	g_{fs}	$V_{DS} \geq 2 \cdot I_D \cdot R_{DS(ON)max}$, $I_D = -5.4$	1.8	3.5	-	S
Input capacitance	C_{iss}	$V_{GS} = 0V$, $V_{DS} = -25V$, $f = 1MHz$	-	360	450	pF
Output capacitance	C_{oss}		-	103	130	
Reverse transfer capacitance	C_{rss}		-	40	50	
Turn-on delay time	$t_{d(ON)}$	$V_{DD} = -30V$, $V_{GS} = -4.5V$, $I_D = -5.4$, $R_G = 6\Omega$	-	11	17	ns
Rise time	t_r	$V_{DD} = -30V$, $V_{GS} = -4.5V$, $I_D = -5.4A$, $R_G = 6\Omega$	-	168	252	
Turn-off delay time	$t_{d(OFF)}$		-	49	74	
Fall time	t_f		-	89	134	

Gate Charge Characteristics

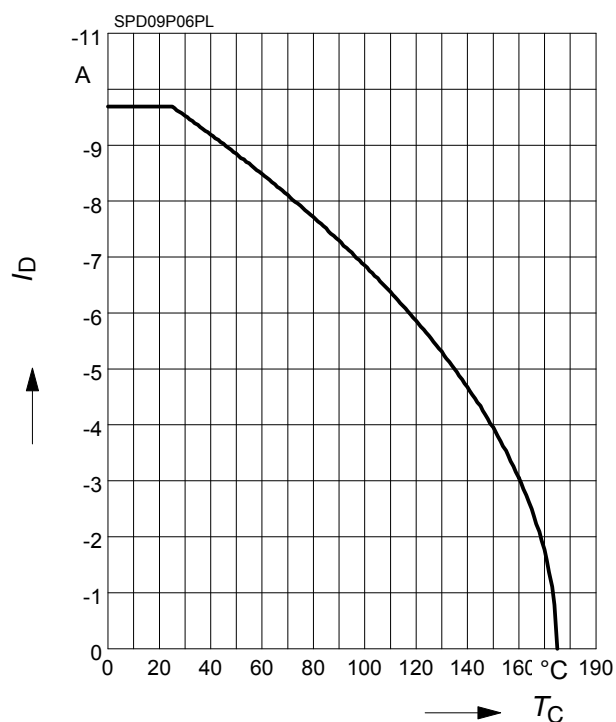
Gate to source charge	Q_{gs}	$V_{DD} = -48V$, $I_D = -9.7A$	-	1.3	2	nC
Gate to drain charge	Q_{gd}		-	5.1	7.5	
Gate charge total	Q_g	$V_{DD} = -48V$, $I_D = -9.7A$, $V_{GS} = 0$ to $-10V$	-	14	21	
Gate plateau voltage	$V_{(plateau)}$	$V_{DD} = -48V$, $I_D = -9.7A$	-	-4.1	-	V

Reverse Diode

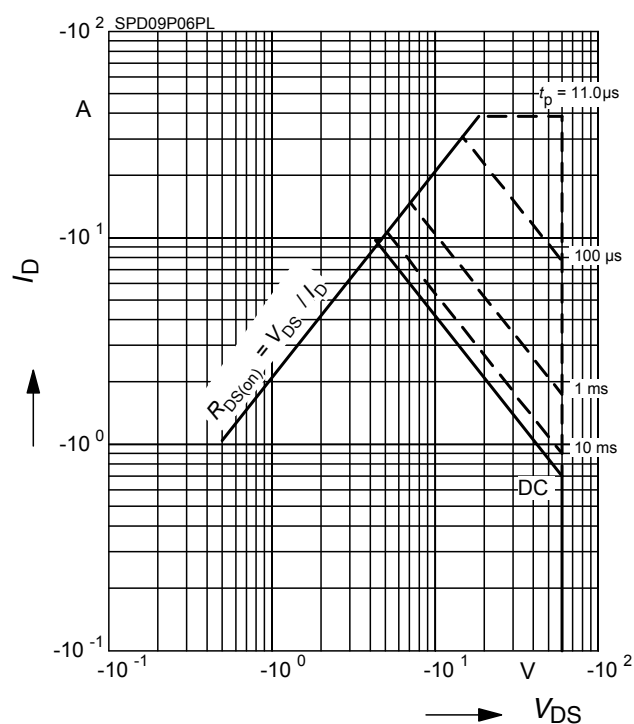
Inverse diode continuous forward current	I_S	$T_C = 25^{\circ}\text{C}$	-	-	-9.7	A
Inverse diode direct current, pulsed	I_{SM}		-	-	-38.8	
Inverse diode forward voltage	V_{SD}	$V_{GS} = 0V$, $I_F = -9.7A$	-	-1.1	-1.4	V
Reverse recovery time	t_{rr}	$V_R = -30V$, $I_F = I_S$	-	52	76	ns
Reverse recovery charge	Q_{rr}	$di_F/dt = 100A/\mu s$	-	64	96	nC

$$P_{\text{tot}} = f(T_C)$$

$$I_D = f(T_C)$$

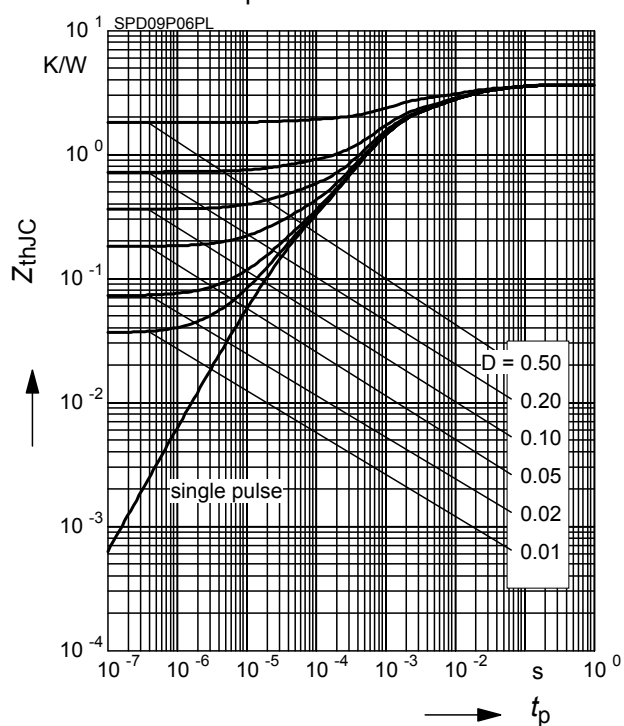
parameter: $V_{GS} \geq 10 \text{ V}$


$$I_D = f(V_{DS})$$

parameter : $D = 0$, $T_C = 25\text{ }^\circ\text{C}$


$$Z_{thJC} = f(t_p)$$

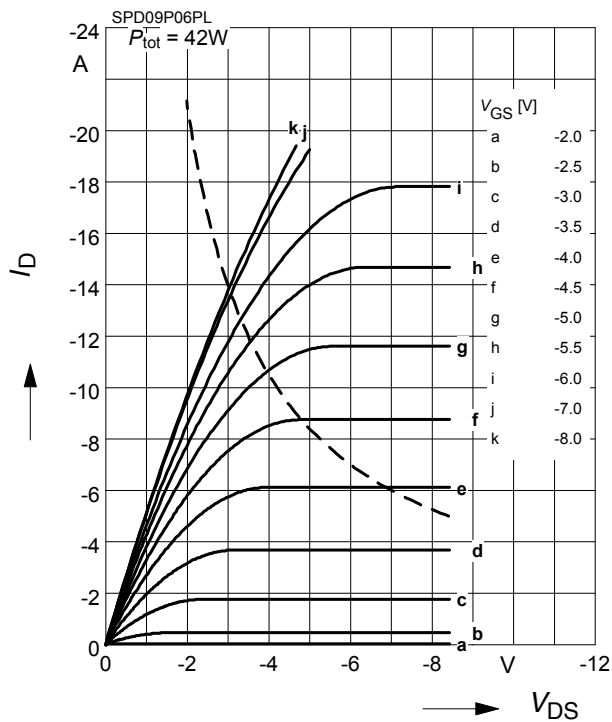
parameter : $D = t_p/T$



5 Typ. output characteristic

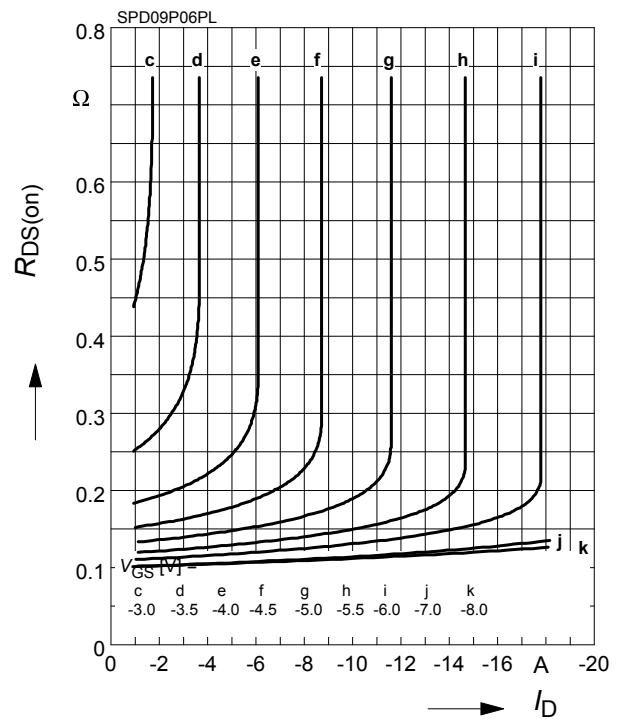
$$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$$

parameter: $t_p = 80 \mu\text{s}$


6 Typ. drain-source on resistance

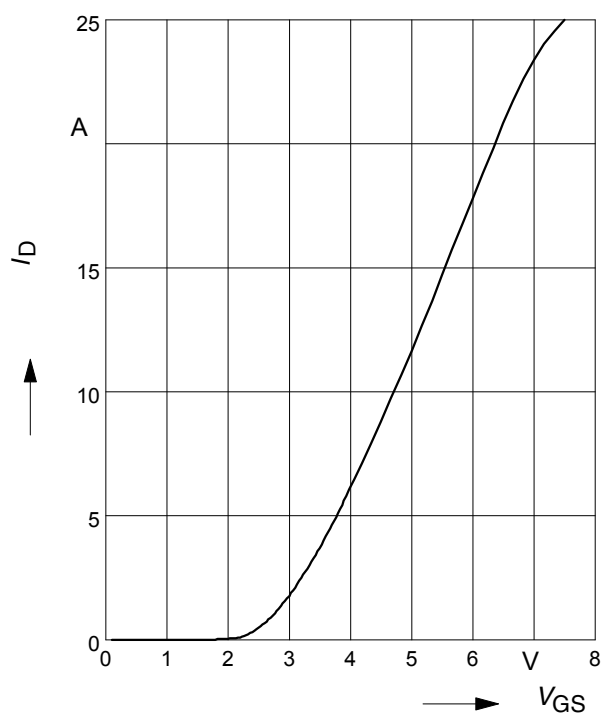
$$R_{DS(\text{on})} = f(I_D)$$

parameter: V_{GS}


7 Typ. transfer characteristics

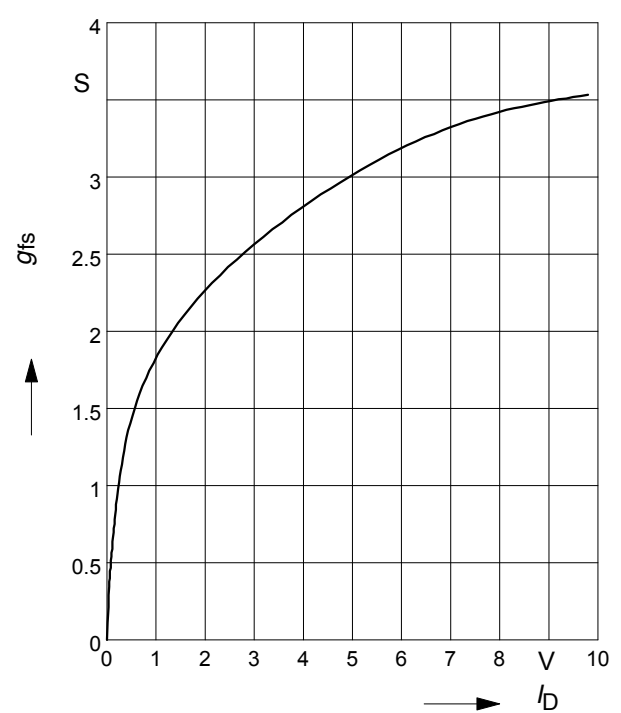
$$I_D = f(V_{GS}); V_{DS} \geq 2 \times I_D \times R_{DS(\text{on})\text{max}}$$

parameter: $t_p = 80 \mu\text{s}$


8 Typ. forward transconductance

$$g_{fs} = f(I_D); T_j = 25^\circ\text{C}$$

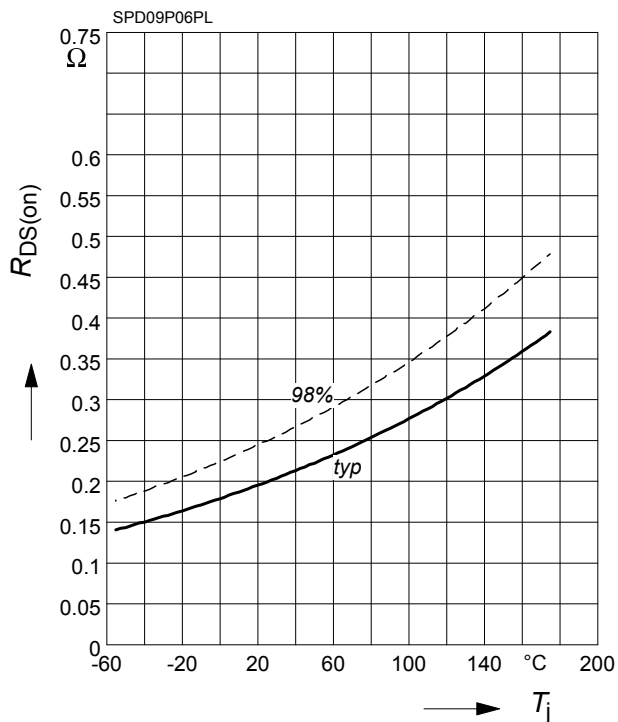
parameter: g_{fs}



9 Drain-source on-state resistance

$$R_{DS(on)} = f(T_j)$$

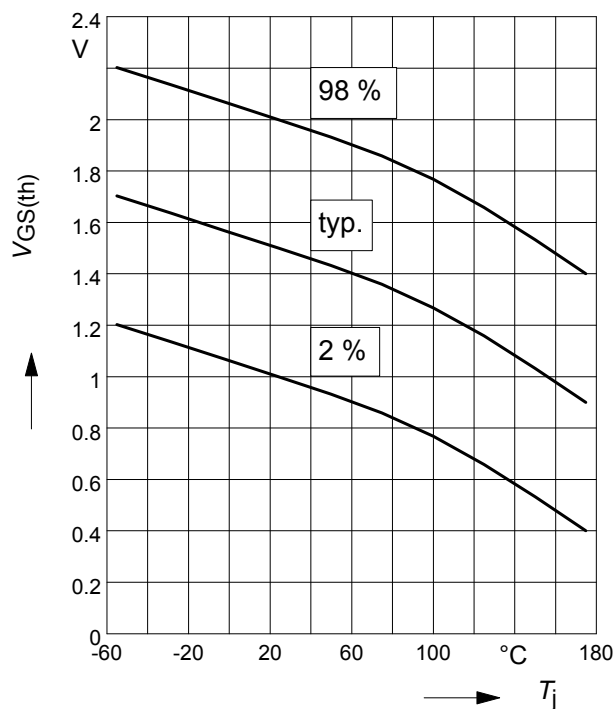
parameter: $I_D = -6.8 \text{ A}$, $V_{GS} = -10 \text{ V}$



10 Gate threshold voltage

$$V_{GS(th)} = f(T_j)$$

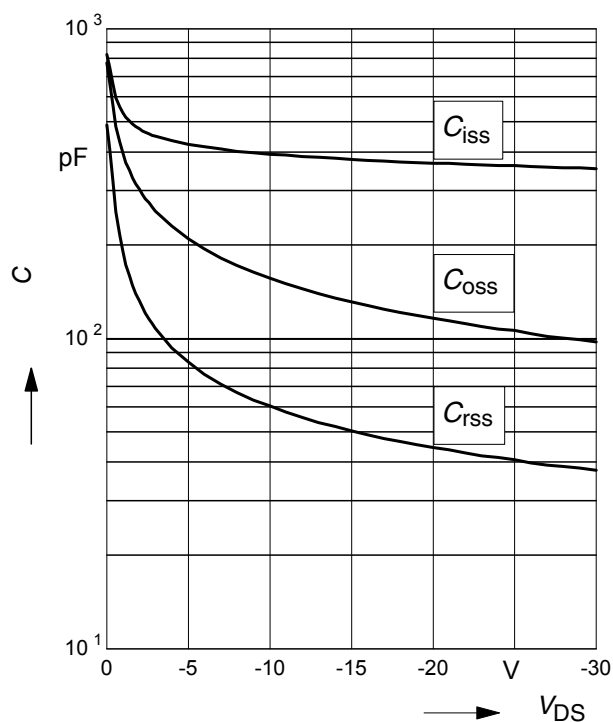
parameter: $V_{GS} = V_{DS}$, $I_D = -250 \mu\text{A}$



11 Typ. capacitances

$$C = f(V_{DS})$$

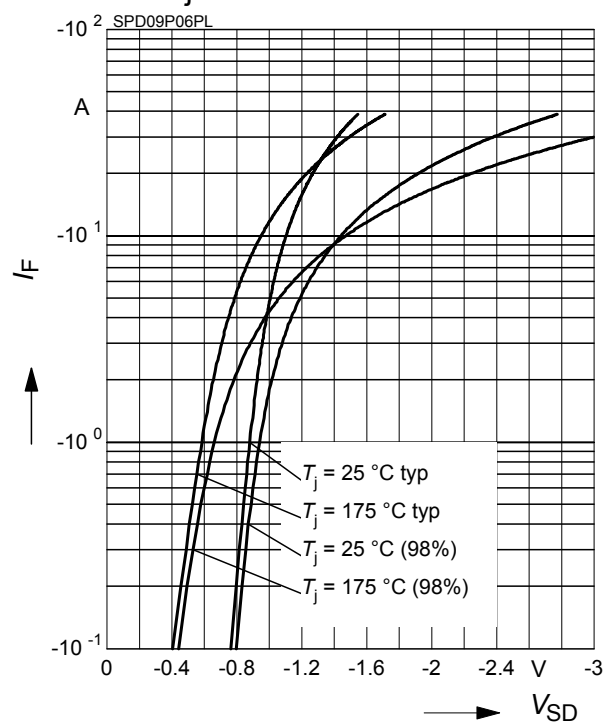
parameter: $V_{GS} = 0\text{V}$, $f = 1 \text{ MHz}$



12 Forward character. of reverse diode

$$I_F = f(V_{SD})$$

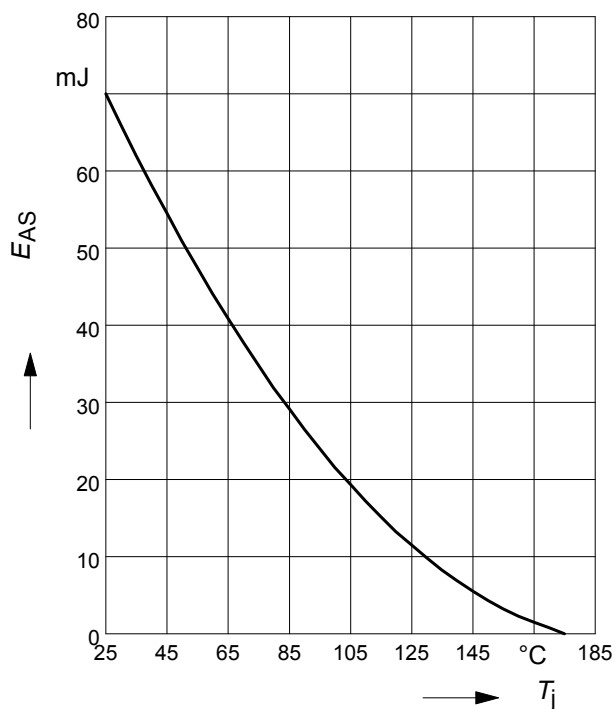
parameter: T_j , $t_p = 80 \mu\text{s}$



13 Typ. avalanche energy

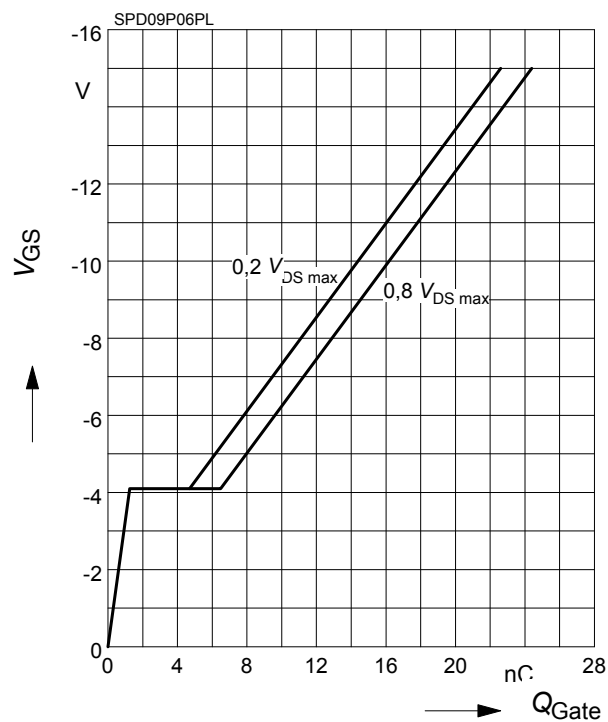
$$E_{AS} = f(T_j)$$

par.: $I_D = -9.7 \text{ A}$, $V_{DD} = -25 \text{ V}$, $R_{GS} = 25 \Omega$

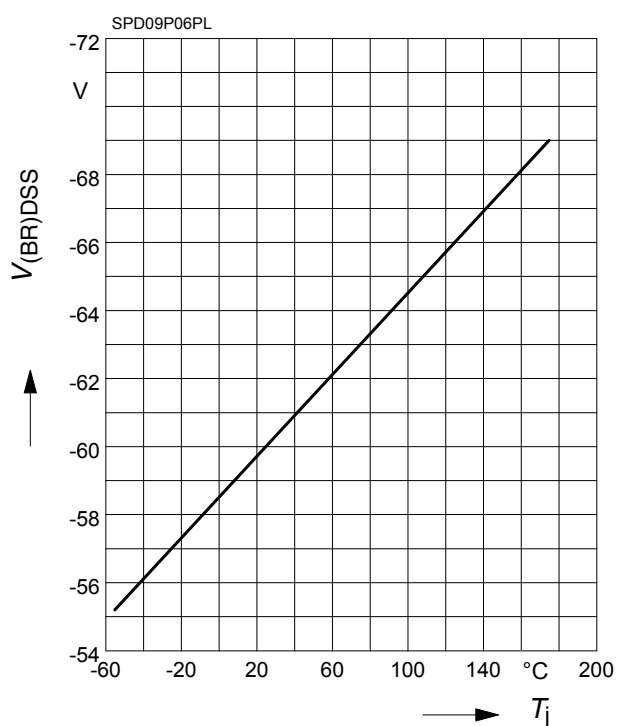

14 Typ. gate charge

$$V_{GS} = f(Q_{Gate})$$

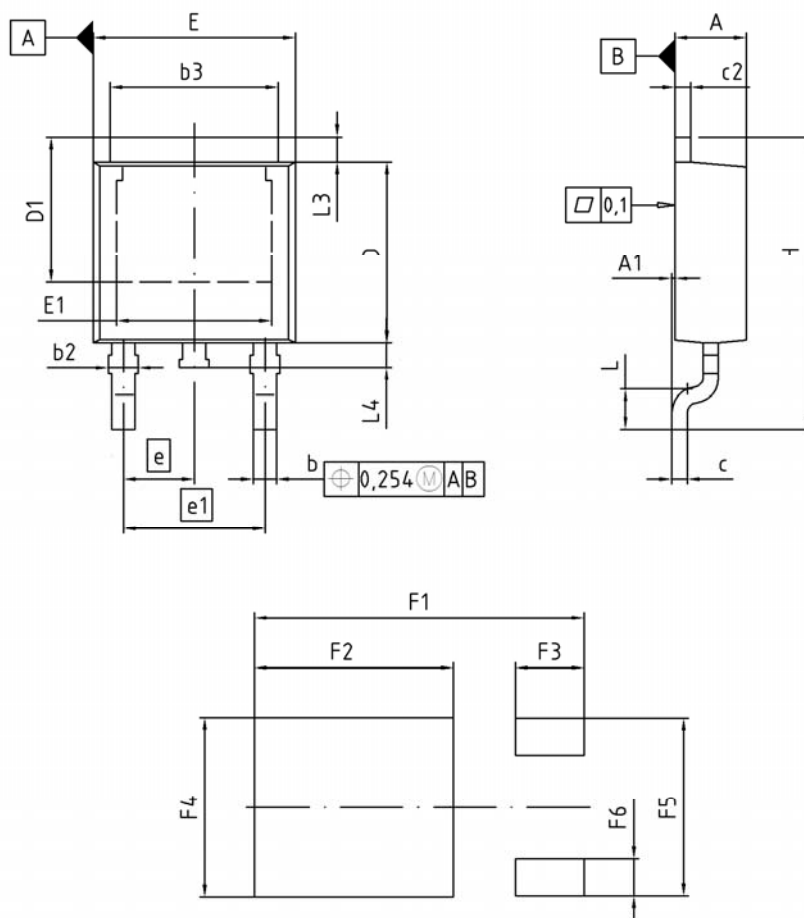
parameter: $I_D = -9.7 \text{ A}$ pulsed


15 Drain-source breakdown voltage

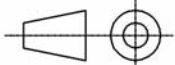
$$V_{(BR)DSS} = f(T_j)$$



Package outline: PG-TO252-3



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.16	2.41	0.085	0.095
A1	0.00	0.15	0.000	0.006
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b3	5.00	5.50	0.197	0.217
c	0.46	0.60	0.018	0.024
c2	0.46	0.98	0.018	0.039
D	5.97	6.22	0.235	0.245
D1	5.02	5.84	0.198	0.230
E	6.40	6.73	0.252	0.265
E1	4.70	5.21	0.185	0.205
e	2.29		0.090	
e1	4.57		0.180	
N	3		3	
H	9.40	10.48	0.370	0.413
L	1.18	1.70	0.046	0.067
L3	0.90	1.25	0.035	0.049
L4	0.51	1.00	0.020	0.039
F1	10.50	10.70	0.413	0.421
F2	6.30	6.50	0.248	0.256
F3	2.10	2.30	0.083	0.091
F4	5.70	5.90	0.224	0.232
F5	5.66	5.86	0.223	0.231
F6	1.10	1.30	0.043	0.051

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